3803 Group (Spec.H QzROM version)

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

REJ03B0166-0113
Rev.1.13
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DESCRIPTION

The 3803 group (Spec.H QzROM version) is the 8-bit microcomputer based on the 740 family core technology.
The 3803 group (Spec.H QzROM version) is designed for household products, office automation equipment, and controlling systems that require analog signal processing, including the serial interface functions, 8/16-bit timer, A/D converter and D/A converter.

FEATURES

- Basic machine-language instructions 71
- Minimum instruction execution time ..... 0.24 µs
  (at 16.8 MHz oscillation frequency)
- Memory size
  QzROM ..... 16 K to 48 K bytes
  RAM ..... 2048 bytes
- Programmable input/output ports 56
- Software pull-up resistors ..... Built-in
- Interrupts ..... 21 sources, 16 vectors
  (external 8, internal 12, software 1)
- Timers ..... 16-bit × 1
  8-bit × 4
  (with 8-bit prescaler)
- Serial interface ..... 8-bit × 2 (UART or Clock-synchronized)
  8-bit × 1 (Clock-synchronized)
- PWM ..... 8-bit × 1 (with 8-bit prescaler)
- A/D converter ..... 10-bit × 16 channels
  (8-bit reading enabled)
- D/A converter ..... 8-bit × 2 channels
- Watchdog timer ..... 16-bit × 1 channel
- LED direct drive port 8
- Clock generating circuit ..... Built-in 2 circuits
  (connect to external ceramic resonator or quartz-crystal oscillator)
- Power source voltage
  [In high-speed mode]
  At 16.8 MHz oscillation frequency ..... 4.5 to 5.5 V
  At 12.5 MHz oscillation frequency ..... 4.0 to 5.5 V
  At 8.4 MHz oscillation frequency ..... 2.7 to 5.5 V
  At 4.2 MHz oscillation frequency ..... 2.2 to 5.5 V
  At 2.1 MHz oscillation frequency ..... 2.0 to 5.5 V
  [In middle-speed mode]
  At 16.8 MHz oscillation frequency ..... 4.5 to 5.5 V
  At 12.5 MHz oscillation frequency ..... 2.7 to 5.5 V
  At 8.4 MHz oscillation frequency ..... 2.2 to 5.5 V
  At 6.3 MHz oscillation frequency ..... 1.8 to 5.5 V
  [In low-speed mode]
  At 32 kHz oscillation frequency ..... 1.8 to 5.5 V
- Power dissipation
  In high-speed mode ..... 40 mW (typ.)
  (at 16.8 MHz oscillation frequency, at 5 V power source voltage)
  In low-speed mode ..... 45 µW (typ.)
  (at 32 kHz oscillation frequency, at 3 V power source voltage)
- Operating temperature range ..... –20 to 85 °C
- Packages
  SP ..... PRDP0064BA-A (64P4B) <64-pin 750mil SDIP>
  HP ... PLQP0064KB-A (64P6Q-A)<64-pin 10 × 10mm LQFP>
  KP ... PLQP0064GA-A (64P6U-A)<64-pin 14 × 14mm LQFP>
  WG ..... PTLG0064JA-A (64F0G)<64-pin 6 × 6mm FLGA>

APPLICATION

Household products, Consumer electronics, etc.

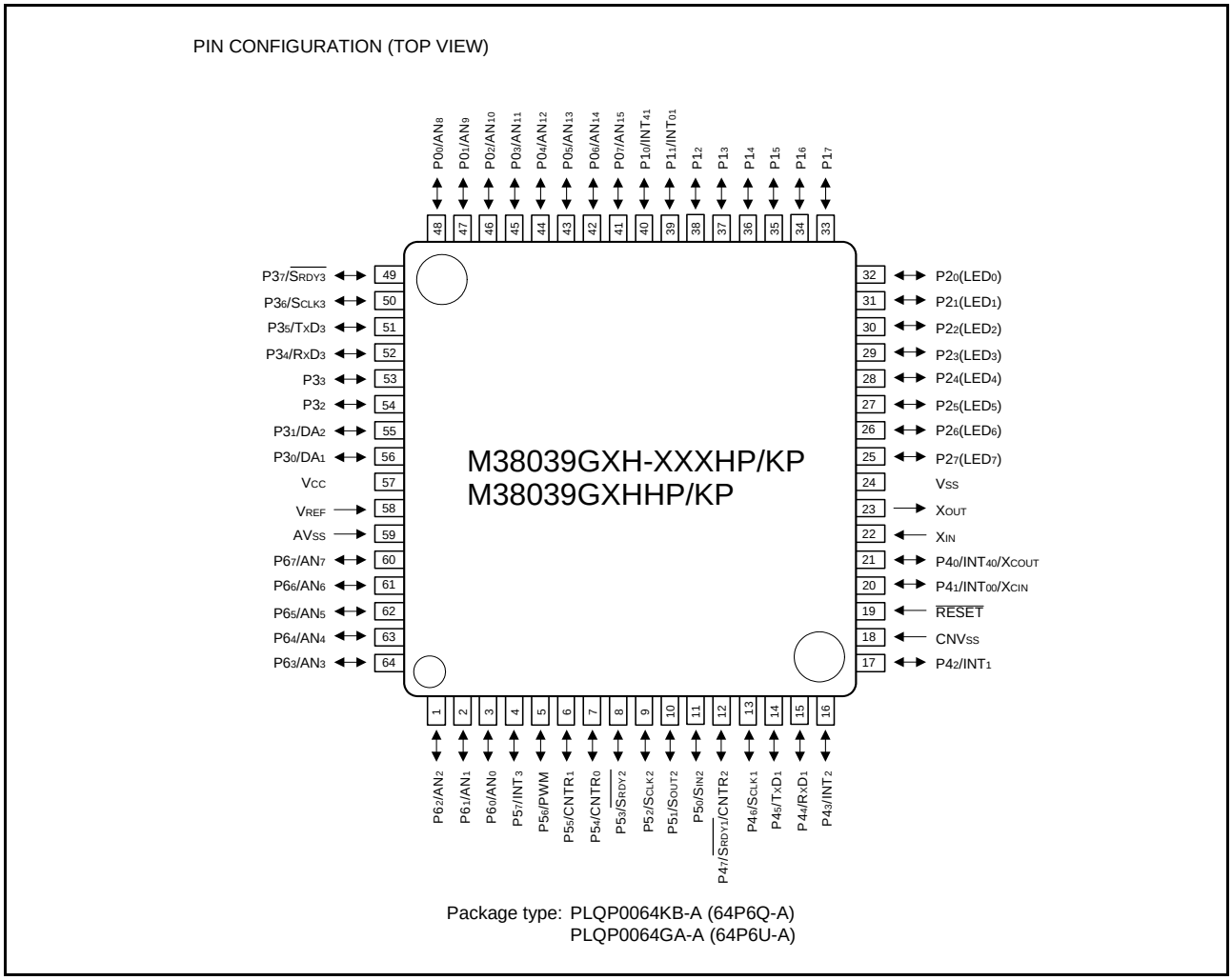


Fig 1. 3803 group (Spec.H QzROM version) pin configuration (PLQP0064KB-A/PLQP0064GA-A)

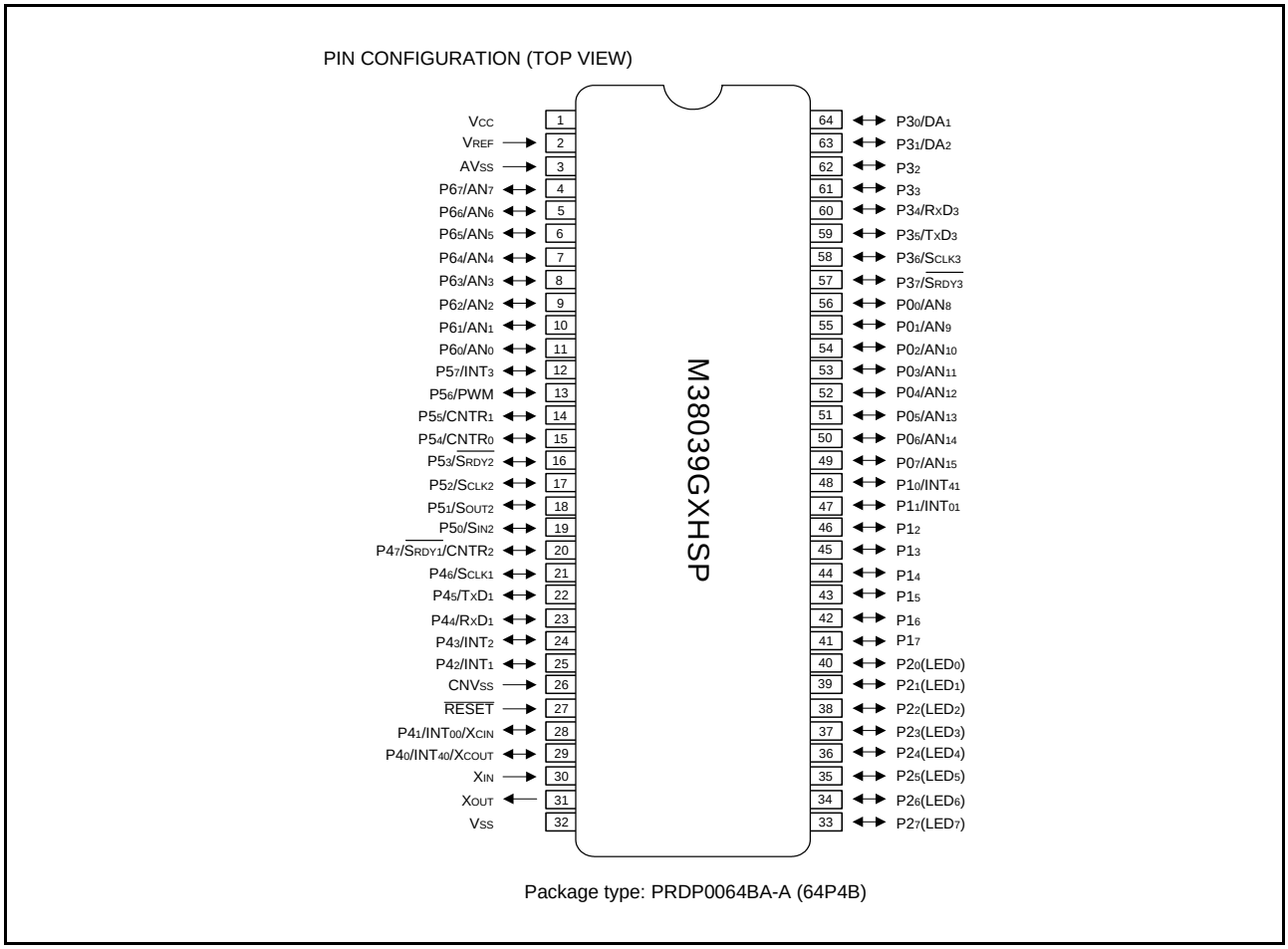
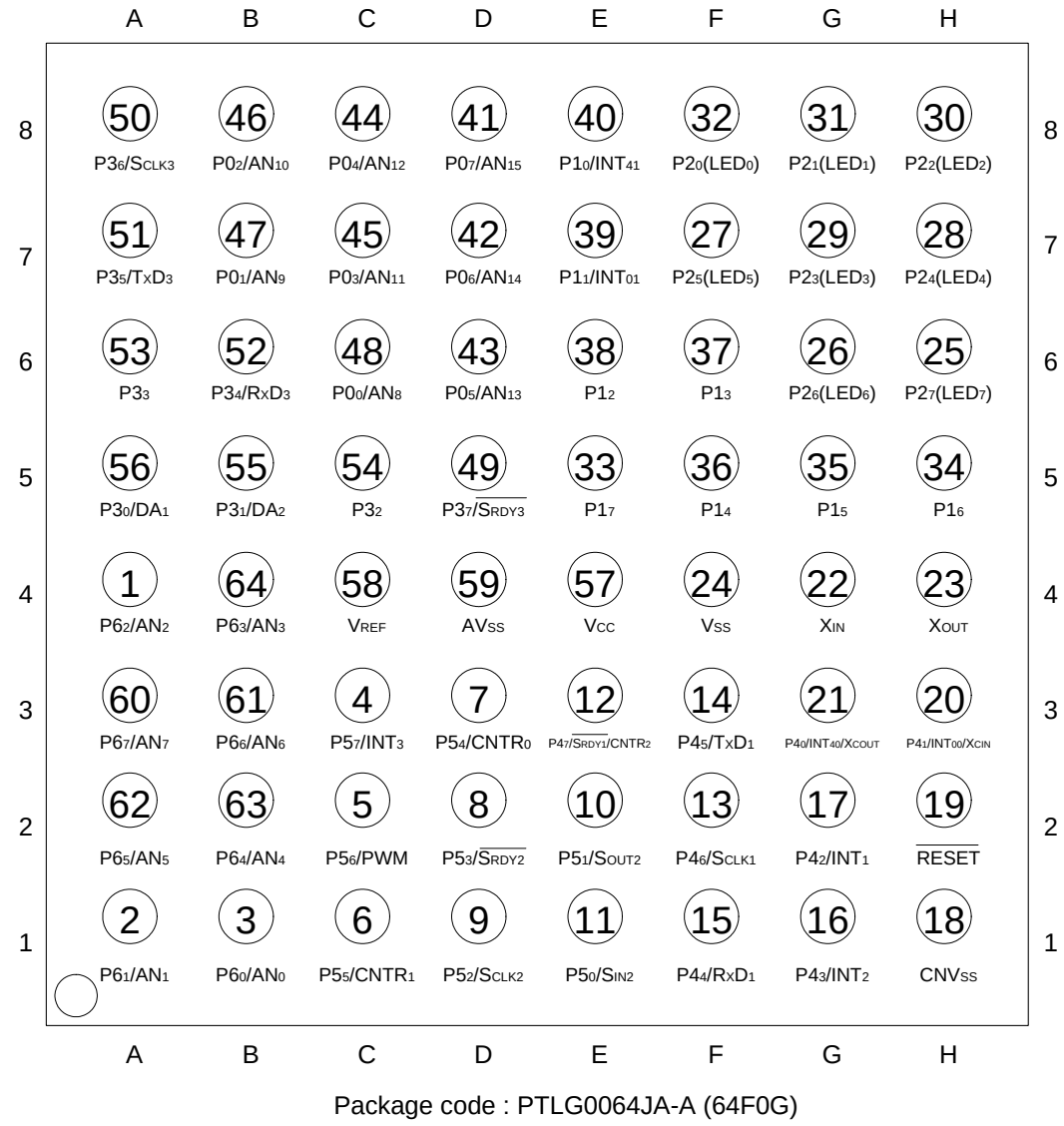


Fig 2. 3803 group (Spec.H QzROM version) pin configuration (PRDP0064BA-A)

PIN CONFIGURATION (TOP VIEW)



Package code : PTLG0064JA-A (64F0G)

Note : The numbers in circles corresponds with the number on the packages HP/KP.

Package (TOP VIEW)

Fig 3. Pin configuration (Top view) (PTLG0064JA-A (64F0G))

Table 1 Performance overview

Parameter				Function
Number of basic instructions				71
Minimum instruction execution time				0.24 μs (Oscillation frequency 16.8 MHz)
Oscillation frequency				16.8 MHz (Maximum)
Memory sizes			ROM	16 to 48 Kbytes
			RAM	2048 Kbytes
I/O port	P0, P1, P2, P3, P4, P5, P6			56 pins
Software pull-up resistors				Built-in
Interrupt				21 sources, 16 vectors (8 external, 12 internal, 1 software)
Timer				8-bit × 4 (with 8-bit prescaler) 16-bit × 1
Serial interface				8-bit × 2 (UART or Clock-synchronized) 8-bit × 1 (Clock-synchronized)
PWM				8-bit × 1 (with 8-bit prescaler)
A/D converter				10-bit × 16 channels (8-bit reading enabled)
D/A converter				8-bit × 2 channels
Watchdog timer				16-bit × 1
LED direct drive port				8 (average current: 10 mA, peak current: 20 mA, total current: 80 mA)
Clock generating circuits				Built-in 2 circuits (connect to external ceramic resonator or quartz-crystal oscillator)
Power source voltage	In high-speed mode	At 16.8 MHz		4.5 to 5.5 V
		At 12.5 MHz		4.0 to 5.5 V
		At 8.4 MHz		2.7 to 5.5 V
		At 4.2 MHz		2.2 to 5.5 V
		At 2.1 MHz		2.0 to 5.5 V
	In middle-speed mode	At 16.8 MHz		4.5 to 5.5 V
		At 12.5 MHz		2.7 to 5.5 V
		At 8.4 MHz		2.2 to 5.5 V
		At 6.3 MHz		1.8 to 5.5 V
	In low-speed mode	At 32 kHz		1.8 to 5.5 V
Power dissipation	In high-speed mode			Std. 40 mW (V_{CC}=5.0V, f(X_{IN})=16.8 MHz, Ta=25 °C)
	In low-speed mode			Std. 45 μW (V_{CC}=3.0V, f(X_{IN})=Stop, f(X_{CIN})=32kHz, Ta=25 °C)
Input/Output characteristics	Input/Output withstand voltage			V_{CC}
	Output current			10 mA
Operating temperature range				-20 to 85 °C
Device structure				CMOS silicon gate
Package				64-pin plastic molded SDIP/LQFP/FLGA

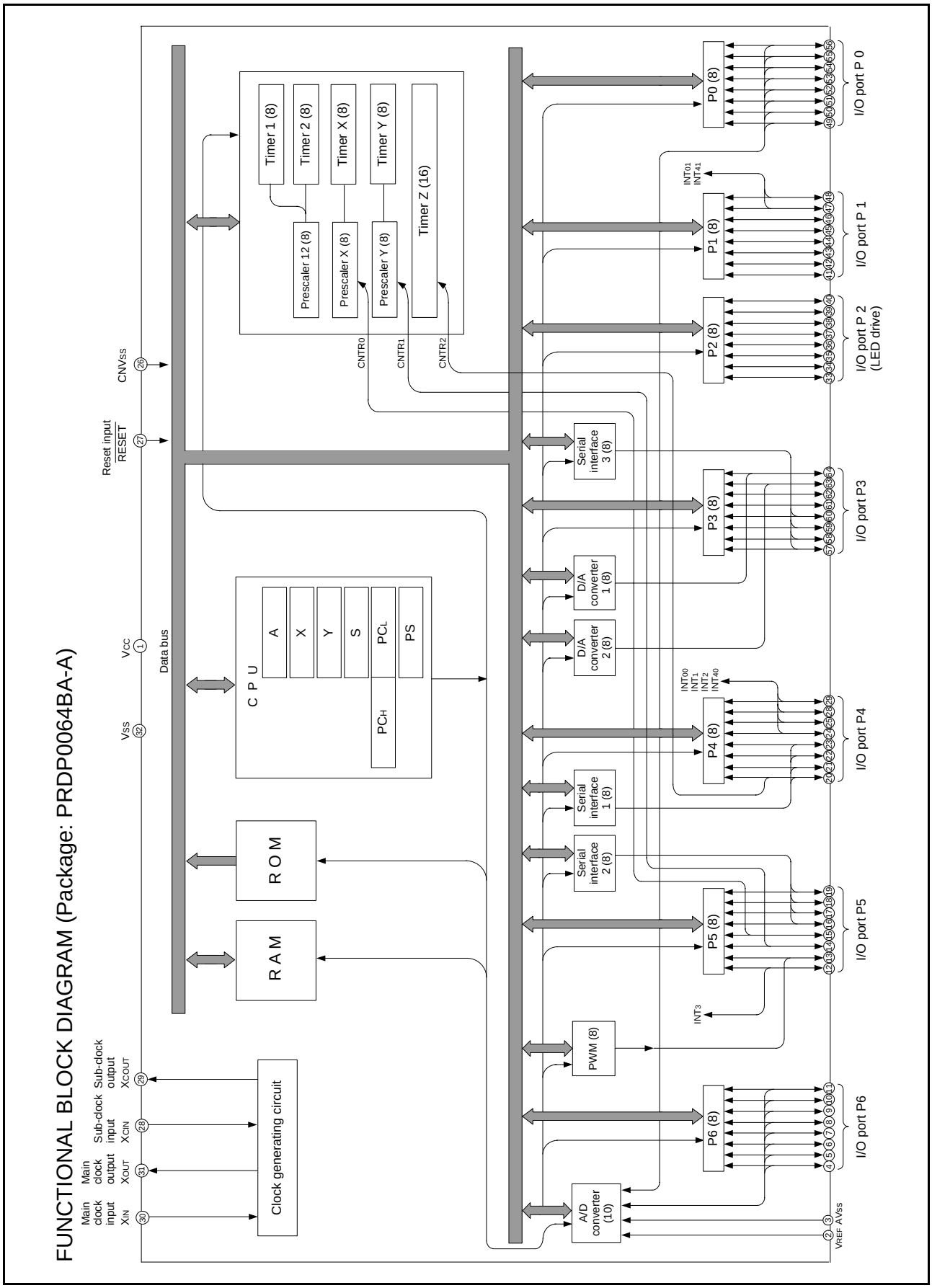


Fig 4. Functional block diagram

PIN DESCRIPTION

Table 2 Pin description

Pin	Name	Functions	Function except a port function
V_{CC}, V_{SS}	Power source	• Apply voltage of 1.8 V – 5.5 V to V_{CC}, and 0 V to V_{SS}.	
CNV_{SS}	CNV_{SS}	• This pin controls the operation mode of the chip and V_{PP} power source input pin in the QzROM writing mode. • Normally connected to V_{SS}.	
V_{REF}	Reference voltage	• Reference voltage input pin for A/D and D/A converters.	
AV_{SS}	Analog power source	• Analog power source input pin for A/D and D/A converters. • Connect to V_{SS}.	
$\overline{RESET}$	Reset input	• Reset input pin for active “L”.	
X_{IN}	Clock input	• Input and output pins for the clock generating circuit. • Connect a ceramic resonator or quartz-crystal oscillator between the X_{IN} and X_{OUT} pins to set the oscillation frequency. • When an external clock is used, connect the clock source to the X_{IN} pin and leave the X_{OUT} pin open.	
X_{OUT}	Clock output		
$P0_0/AN_8$– $P0_7/AN_{15}$	I/O port P0	• 8-bit CMOS I/O port. • I/O direction register allows each pin to be individually programmed as either input or output. • CMOS compatible input level. • CMOS 3-state output structure. • Pull-up control is enabled in a bit unit. • $P2_0$ – $P2_7$ (8 bits) are enabled to output large current for LED drive.	• A/D converter input pin
$P1_0/INT_{41}$ $P1_1/INT_{01}$	I/O port P1		• Interrupt input pin
$P1_2$–$P1_7$			
$P2_0$ (LED_0)– $P2_7$ (LED_7)	I/O port P2		
$P3_0/DA_1$ $P3_1/DA_2$	I/O port P3	• 8-bit CMOS I/O port. • I/O direction register allows each pin to be individually programmed as either input or output. • CMOS compatible input level. • $P3_0$, $P3_1$, $P3_4$ – $P3_7$ are CMOS 3-state output structure. • $P3_2$, $P3_3$ are N-channel open-drain output structure. • Pull-up control of $P3_0$, $P3_1$, $P3_4$ – $P3_7$ is enabled in a bit unit.	• D/A converter input pin
$P3_2$, $P3_3$			
$P3_4/RxD_3$ $P3_5/TxD_3$ $P3_6/SCLK_3$ $P3_7/\overline{SRDY_3}$			• Serial I/O3 function pin
$P4_0/INT_{40}/XCOUT$ $P4_1/INT_{00}/XCIN$	I/O port P4	• 8-bit CMOS I/O port. • I/O direction register allows each pin to be individually programmed as either input or output. • CMOS compatible input level. • CMOS 3-state output structure. • Pull-up control is enabled in a bit unit.	• Interrupt input pin • Sub-clock generating I/O pin (resonator connected)
$P4_2/INT_1$ $P4_3/INT_2$			• Interrupt input pin
$P4_4/RxD_1$ $P4_5/TxD_1$ $P4_6/SCLK_1$			• Serial I/O1 function pin
$P4_7/\overline{SRDY_1}/CNTR_2$			• Serial I/O1, timer Z function pin
$P5_0/SIN_2$ $P5_1/SOUT_2$ $P5_2/\overline{SCLK_2}$ $P5_3/\overline{SRDY_2}$	I/O port P5		• Serial I/O2 function pin
$P5_4/CNTR_0$			• Timer X function pin
$P5_5/CNTR_1$			• Timer Y function pin
$P5_6$/PWM			• PWM output pin
$P5_7/INT_3$			• Interrupt input pin
$P6_0/AN_0$– $P6_7/AN_7$	I/O port P6		• A/D converter input pin

PART NUMBERING

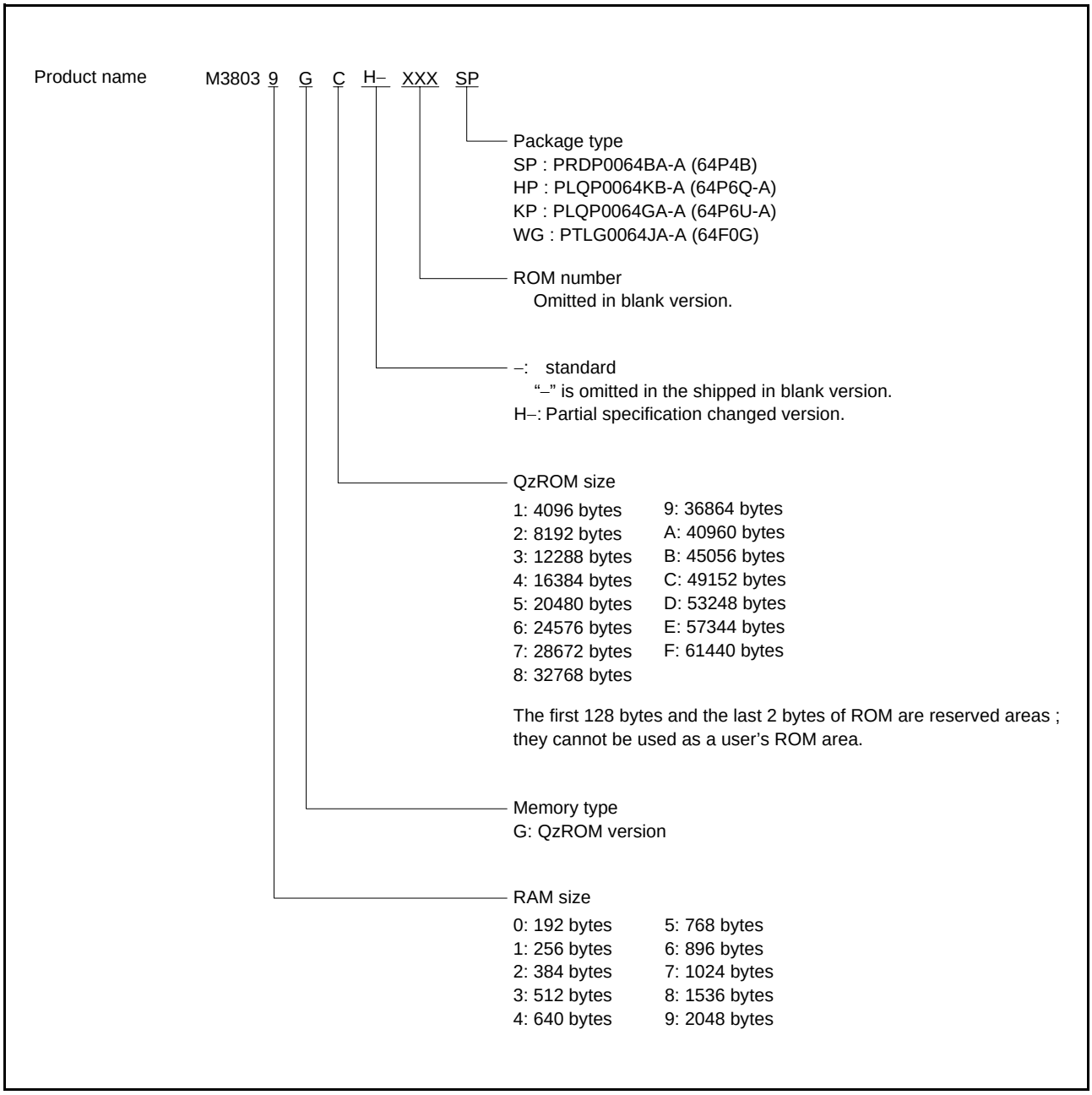


Fig 5. Part numbering

GROUP EXPANSION

Renesas Technology expands the 3803 group (Spec.H QzROM version) as follows.

Memory Type

Support for QzROM version.

Memory Size

- QzROM size ..... 16 K to 48 K bytes
- RAM size ..... 2048 bytes

Packages

- PRDP0064BA-A ..... 64-pin shrink plastic-molded SDIP
- PLQP0064KB-A .....0.5 mm-pitch plastic molded LQFP
- PLQP0064GA-A .....0.8 mm-pitch plastic molded LQFP
- PTLG0064JA-A.....0.65 mm-pitch plastic molded FLGA

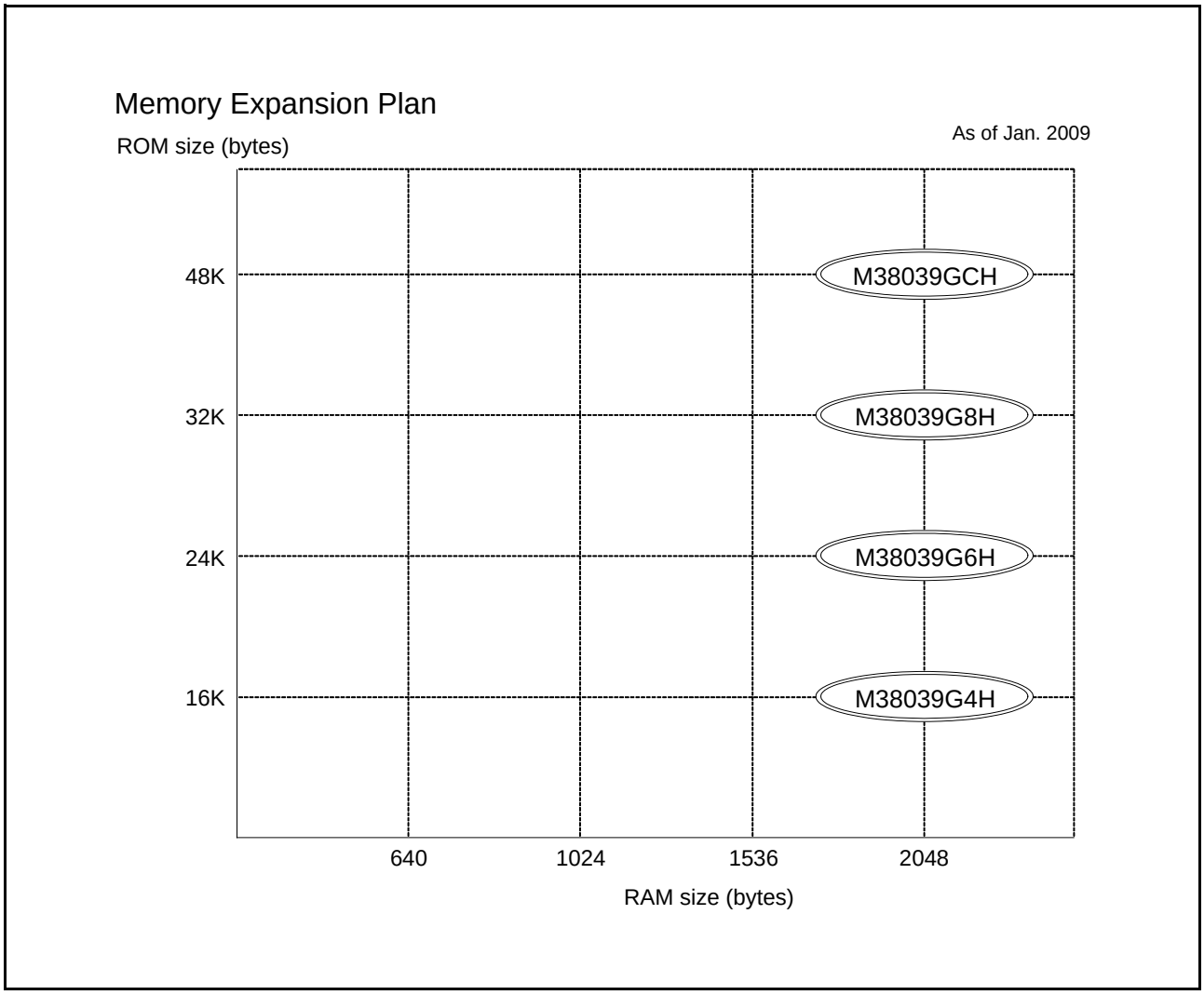


Fig 6. Memory expansion plan

Table 3 Support products

Product name	QzROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M38039G4H-XXXHP	16384 (16254) (3)	2048	PLQP0064KB-A (64P6Q-A)	QzROM version (Programmed shipment) (1)
M38039G4H-XXXKP			PLQP0064GA-A (64P6U-A)	
M38039G6H-XXXHP	24576 (24446) (3)		PLQP0064KB-A (64P6Q-A)	
M38039G6H-XXXKP			PLQP0064GA-A (64P6U-A)	
M38039G8H-XXXHP	32768 (32638) (3)		PLQP0064KB-A (64P6Q-A)	
M38039G8H-XXXKP			PLQP0064GA-A (64P6U-A)	
M38039GCH-XXXHP	49152 (49022) (3)		PLQP0064KB-A (64P6Q-A)	
M38039GCH-XXXKP			PLQP0064GA-A (64P6U-A)	
M38039GCH-XXXWG			PTLG0064JA-A (64F0G)	
M38039G4HSP	16384 (16254) (3)		PRDP0064BA-A (64F4B)	QzROM version (blank) (2)
M38039G4HHP			PLQP0064KB-A (64P6Q-A)	
M38039G4HKP			PLQP0064GA-A (64P6U-A)	
M38039G6HSP	24576 (24446) (3)		PRDP0064BA-A (64P4B)	
M38039G6HHP			PLQP0064KB-A (64P6Q-A)	
M38039G6HKP			PLQP0064GA-A (64P6U-A)	
M38039G8HSP	32768 (32638) (3)		PRDP0064BA-A (64P4B)	
M38039G8HHP			PLQP0064KB-A (64P6Q-A)	
M38039G8HKP			PLQP0064GA-A (64P6U-A)	
M38039GCHSP	49152 (49022) (3)		PRDP0064BA-A (64P4B)	
M38039GCHHP			PLQP0064KB-A (64P6Q-A)	
M38039GCHKP			PLQP0064GA-A (64P6U-A)	
M38039GCHWG			PTLG0064JA-A (64F0G)	

NOTES:
1. This means a shipment of which User ROM has been programmed.
2. The user ROM area of a blank product is blank.
3. ROM size includes the ID code protect area.

FUNCTIONAL DESCRIPTION

CENTRAL PROCESSING UNIT (CPU)

The 3803 group (Spec.H QzROM version) uses the standard 740 Family instruction set. Refer to the table of 740 Family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.
Machine-resident 740 Family instructions are as follows:
The FST and SLW instructions cannot be used.
The STP, WIT, MUL, and DIV instructions can be used.

[Accumulator (A)]

The accumulator is an 8-bit register. Data operations such as data transfer, etc. are executed mainly through the accumulator.

[Index Register X (X)]

The index register X is an 8-bit register. In the index addressing modes, the value of the OPERAND is added to the contents of register X and specifies the real address.

[Index Register Y (Y)]

The index register Y is an 8-bit register. In partial instruction, the value of the OPERAND is added to the contents of register Y and specifies the real address.

[Stack Pointer (S)]

The stack pointer is an 8-bit register used during subroutine calls and interrupts. This register indicates start address of stored area (stack) for storing registers during subroutine calls and interrupts.
The low-order 8 bits of the stack address are determined by the contents of the stack pointer. The high-order 8 bits of the stack address are determined by the stack page selection bit. If the stack page selection bit is “0”, the high-order 8 bits becomes “00_{16}”. If the stack page selection bit is “1”, the high-order 8 bits becomes “01_{16}”.
The operations of pushing register contents onto the stack and popping them from the stack are shown in Figure 8.
Store registers other than those described in Figure 7 with program when the user needs them during interrupts or subroutine calls (see Table 4).

[Program Counter (PC)]

The program counter is a 16-bit counter consisting of two 8-bit registers PC_H and PC_L. It is used to indicate the address of the next instruction to be executed.

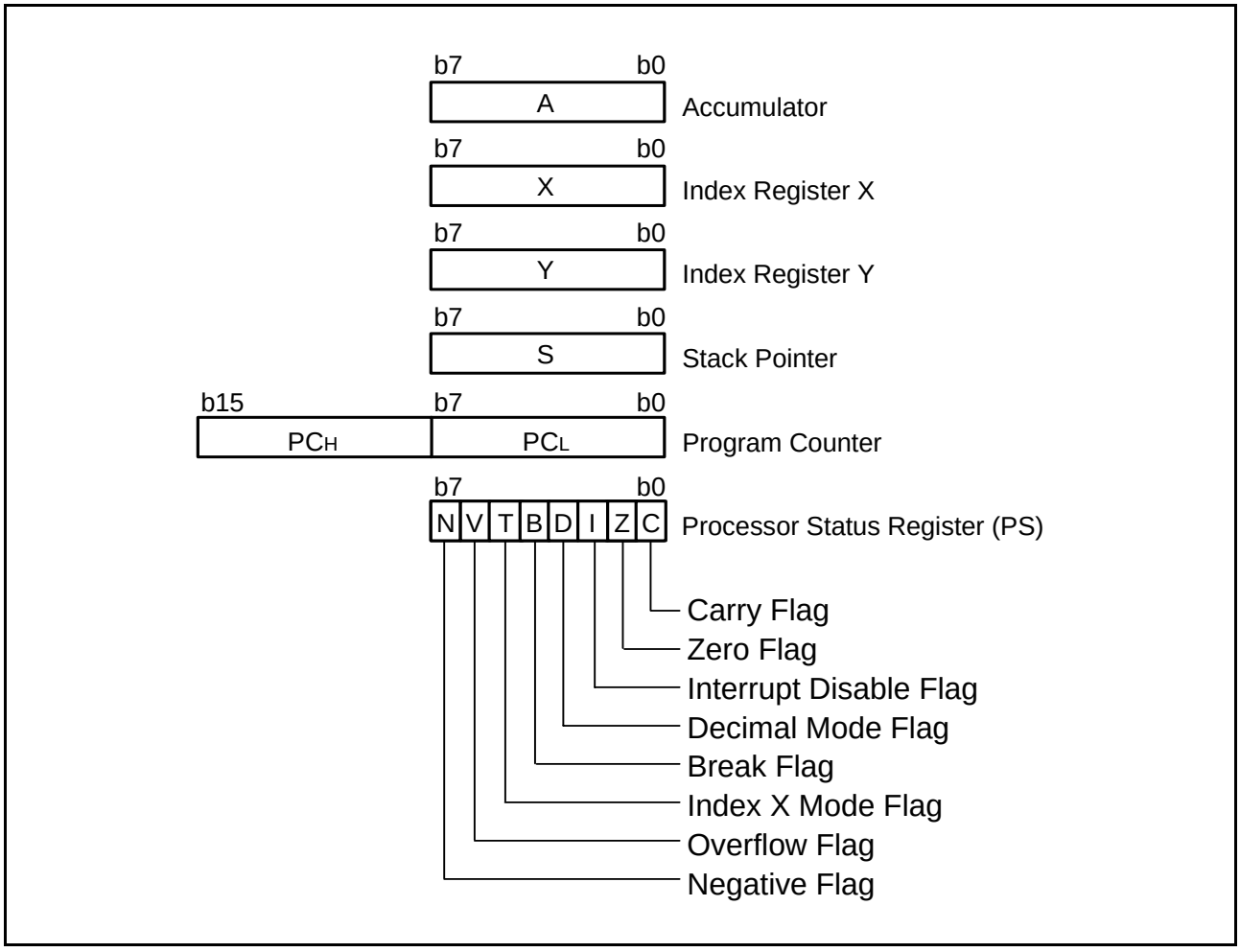


Fig 7. 740 Family CPU register structure

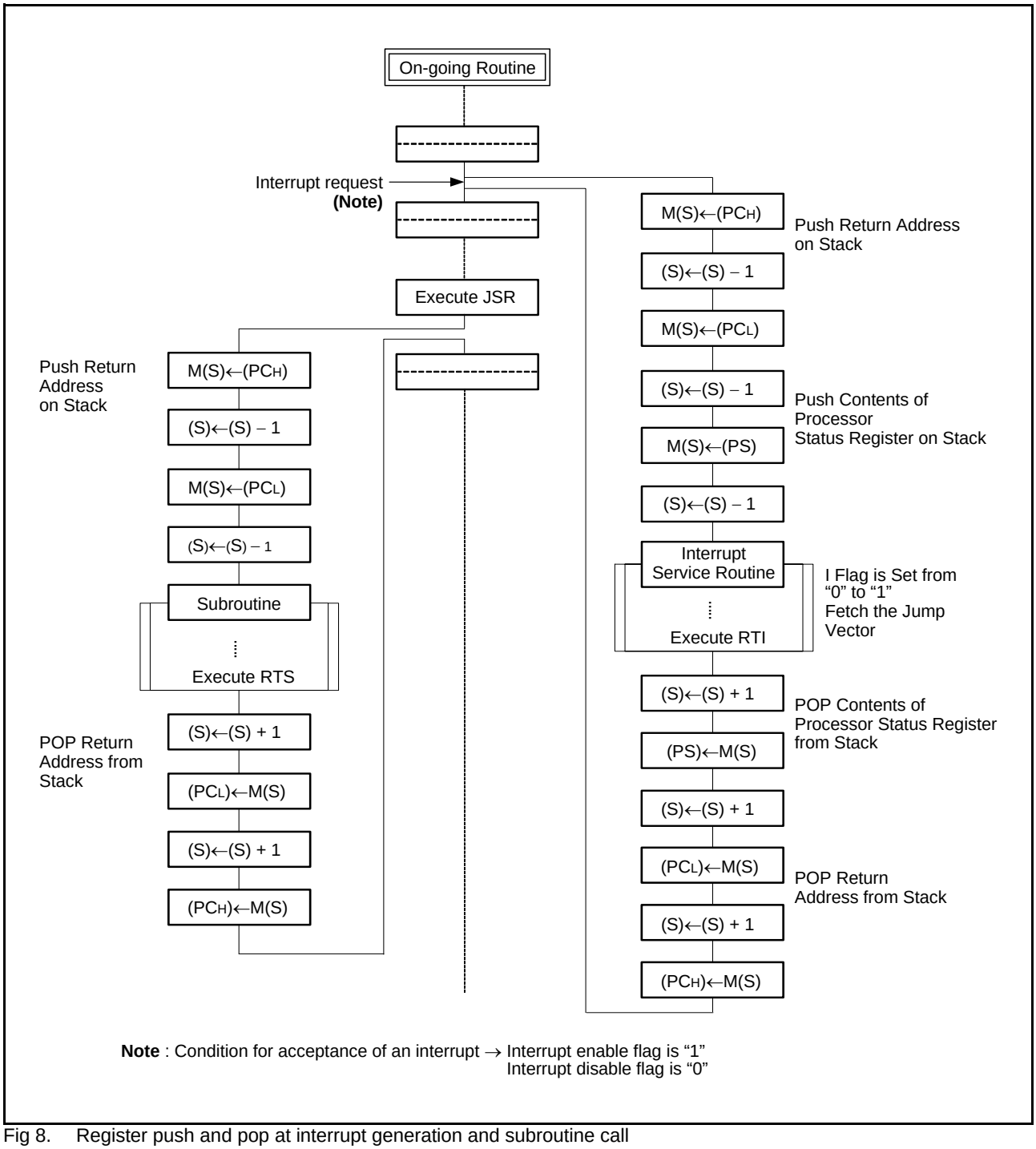


Fig 8. Register push and pop at interrupt generation and subroutine call

Table 4 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

[Processor status register (PS)]

The processor status register is an 8-bit register consisting of 5 flags which indicate the status of the processor after an arithmetic operation and 3 flags which decide MCU operation. Branch operations can be performed by testing the Carry (C) flag, Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

Bit 0: Carry flag (C)

The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

Bit 1: Zero flag (Z)

The Z flag is set if the result of an immediate arithmetic operation or a data transfer is “0”, and cleared if the result is anything other than “0”.

Bit 2: Interrupt disable flag (I)

The I flag disables all interrupts except for the interrupt generated by the BRK instruction.
Interrupts are disabled when the I flag is “1”.

Bit 3: Decimal mode flag (D)

The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is “0”; decimal arithmetic is executed when it is “1”.
Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can execute decimal arithmetic.

Bit 4: Break flag (B)

The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always “0”. When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to “1”.

Bit 5: Index X mode flag (T)

When the T flag is “0”, arithmetic operations are performed between accumulator and memory. When the T flag is “1”, direct arithmetic operations and direct data transfers are enabled between memory locations.

Bit 6: Overflow flag (V)

The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to –128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.

Bit 7: Negative flag (N)

The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 5 Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	–	SEI	SED	–	SET	–	–
Clear instruction	CLC	–	CLI	CLD	–	CLT	CLV	–

[CPU Mode Register (CPUM)] 003B16

The CPU mode register contains the stack page selection bit, the internal system clock control bits, etc.
The CPU mode register is allocated at address 003B16.

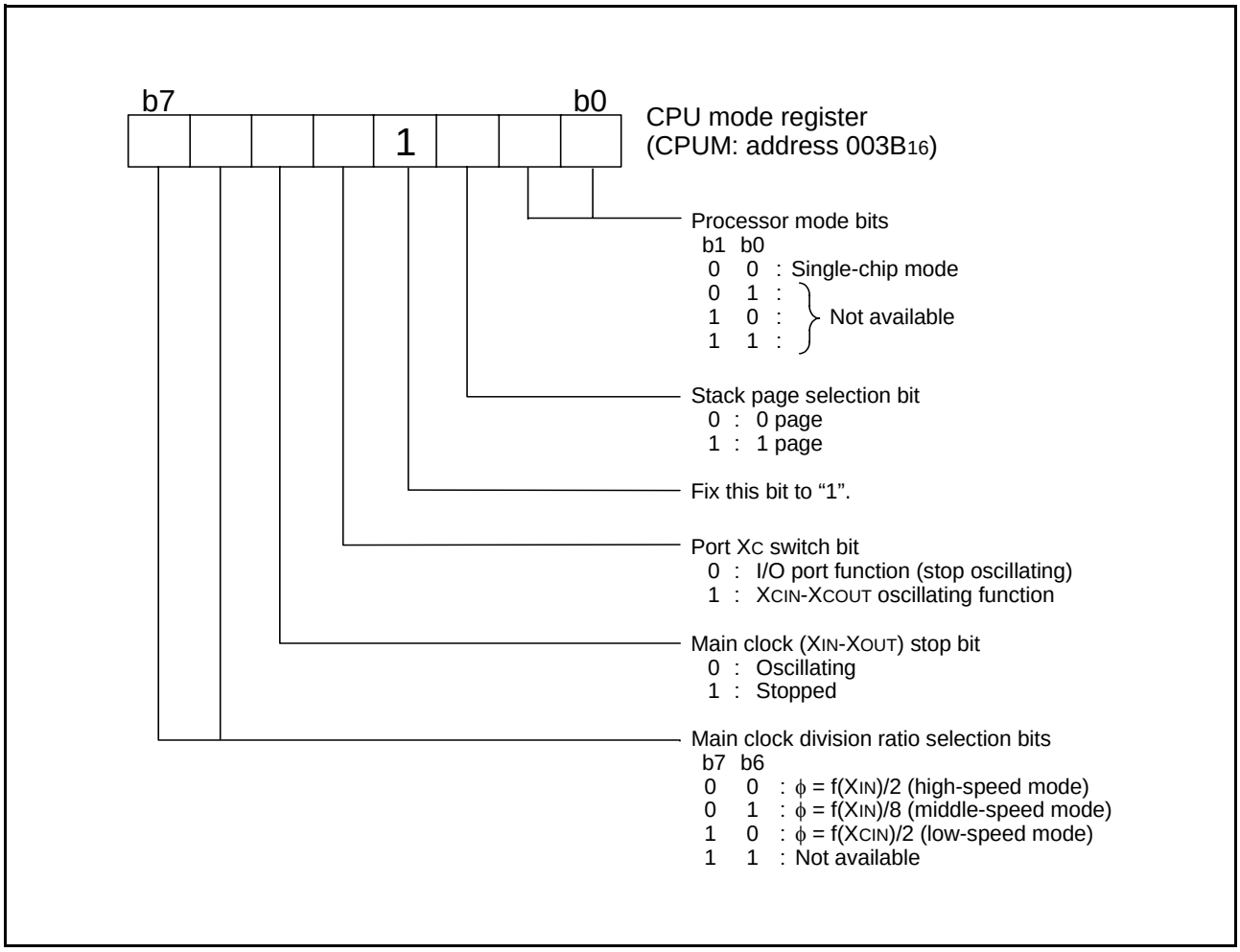


Fig 9. Structure of CPU mode register

MISRG

(1) Bit 0 of address 0010$_{16}$: Oscillation stabilizing time set after STP instruction released bit

When the MCU stops the clock oscillation by the STP instruction and the STP instruction has been released by an external interrupt source, usually, the fixed values of Timer 1 and Prescaler 12 (Timer 1 = 01$_{16}$, Prescaler 12 = FF$_{16}$) are automatically reloaded in order for the oscillation to stabilize. The user can inhibit the automatic setting by setting "1" to bit 0 of MISRG (address 0010$_{16}$).
However, by setting this bit to "1", the previous values, set just before the STP instruction was executed, will remain in Timer 1 and Prescaler 12. Therefore, you will need to set an appropriate value to each register, in accordance with the oscillation stabilizing time, before executing the STP instruction.
Figure 10 shows the structure of MISRG.

(2) Bits 1, 2, 3 of address 0010$_{16}$: Middle-speed Mode Automatic Switch Function

In order to switch the clock mode of an MCU which has a sub-clock, the following procedure is necessary:
set CPU mode register (003B$_{16}$) --> start main clock oscillation --> wait for oscillation stabilization --> switch to middle-speed mode (or high-speed mode).
However, the 3803 group (Spec.H QzROM version) has the built-in function which automatically switches from low to middle-speed mode by program.

• Middle-speed mode automatic switch by program

The middle-speed mode can also be automatically switched by program while operating in low-speed mode. By setting the middle-speed automatic switch start bit (bit 3) of MISRG (address 0010$_{16}$) to "1" in the condition that the middle-speed mode automatic switch set bit is "1" while operating in low-speed mode, the MCU will automatically switch to middle-speed mode. In this case, the oscillation stabilizing time of the main clock can be selected by the middle-speed automatic switch wait time set bit (bit 2) of MISRG (address 0010$_{16}$).

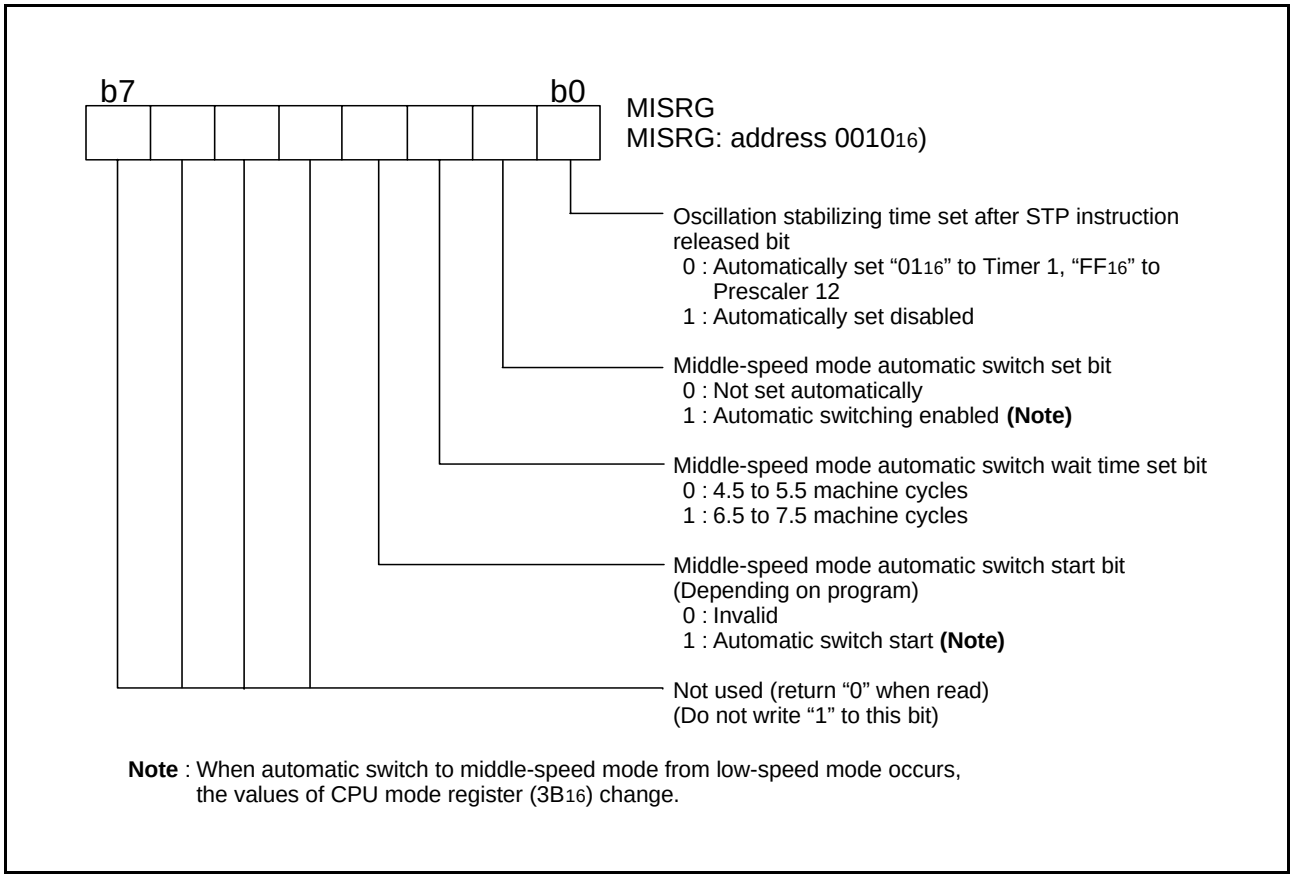


Fig 10. Structure of MISRG

MEMORY

• Special Function Register (SFR) Area

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

• RAM

The RAM is used for data storage and for stack area of subroutine calls and interrupts.

• ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is a user area for storing programs. In the QzROM version, 1 byte of address FFDB16 is also a reserved area.

• Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

• Zero Page

Access to this area with only 2 bytes is possible in the zero page addressing mode.

• Special Page

Access to this area with only 2 bytes is possible in the special page addressing mode.

• ROM Code Protect Address (address FFDB16)

Address FFDB16, which is the reserved ROM area of QzROM, is the ROM code protect address. "0016" or "FE16" is written into this address when selecting the protect bit write by using a serial programmer or selecting protect enabled for writing shipment by Renesas Technology corp. When "0016" or "FE16" is set to the ROM code protect address, the protect function is enabled, so that reading or writing from/to QzROM is disabled by a serial programmer.
As for the QzROM product in blank, the ROM code is protected by selecting the protect bit write at ROM writing with a serial programmer.
The protect can be performed, dividing twice. The protect area 1 is from the beginning address of ROM to address "EFFF16". As for the QzROM product shipped after writing, "0016" (protect enabled to all area), "FE16" (protect enabled to the protect area 1) or "FF16" (protect disabled) is written into the ROM code protect address when Renesas Technology corp. performs writing.
The writing of "0016", "FE16" or "FF16" can be selected as ROM option setup ("MASK option" written in the mask file converter) when ordering.

<Notes>

Since the contents of RAM are undefined at reset, be sure to set an initial value before use.

ROM area

ROM size (bytes)	Address YYYY16	Address ZZZZ16
4096	F00016	F08016
8192	E00016	E08016
12288	D00016	D08016
16384	C00016	C08016
20480	B00016	B08016
24576	A00016	A08016
28672	900016	908016
32768	800016	808016
36864	700016	708016
40960	600016	608016
45056	500016	508016
49152	400016	408016
53248	300016	308016
57344	200016	208016
61440	100016	108016

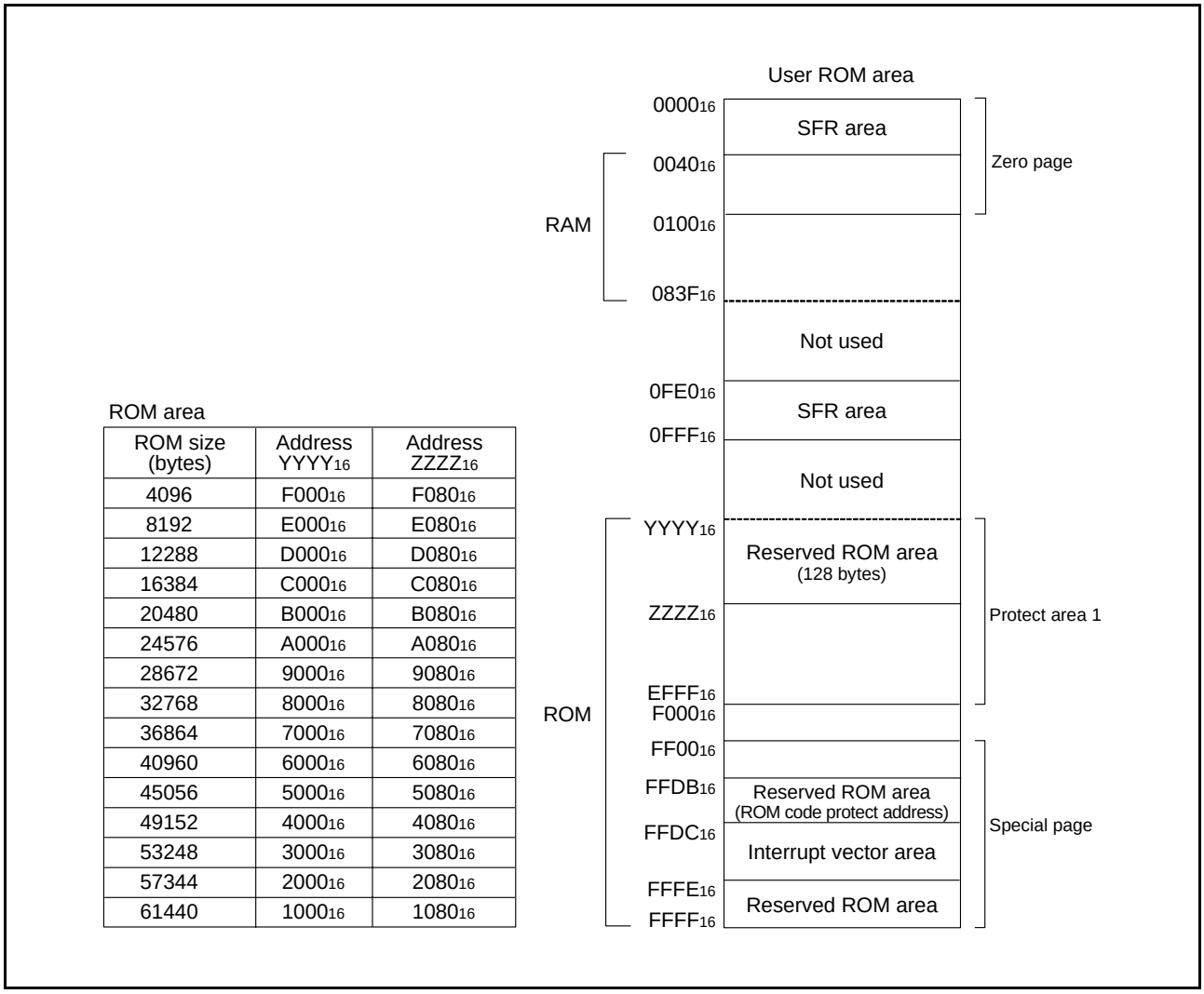


Fig 11. Memory map diagram

0000₁₆	Port P0 (P0)
0001₁₆	Port P0 direction register (P0D)
0002₁₆	Port P1 (P1)
0003₁₆	Port P1 direction register (P1D)
0004₁₆	Port P2 (P2)
0005₁₆	Port P2 direction register (P2D)
0006₁₆	Port P3 (P3)
0007₁₆	Port P3 direction register (P3D)
0008₁₆	Port P4 (P4)
0009₁₆	Port P4 direction register (P4D)
000A₁₆	Port P5 (P5)
000B₁₆	Port P5 direction register (P5D)
000C₁₆	Port P6 (P6)
000D₁₆	Port P6 direction register (P6D)
000E₁₆	Timer 12, X count source selection register (T12XCSS)
000F₁₆	Timer Y, Z count source selection register (TYZCSS)
0010₁₆	MISRG
0011₁₆	Reserved **(Note 1)**
0012₁₆	Reserved **(Note 1)**
0013₁₆	Reserved **(Note 1)**
0014₁₆	Reserved **(Note 1)**
0015₁₆	Reserved **(Note 1)**
0016₁₆	Reserved **(Note 1)**
0017₁₆	Reserved **(Note 1)**
0018₁₆	Transmit/Receive buffer register 1 (TB1/RB1)
0019₁₆	Serial I/O1 status register (SIO1STS)
001A₁₆	Serial I/O1 control register (SIO1CON)
001B₁₆	UART1 control register (UART1CON)
001C₁₆	Baud rate generator (BRG1)
001D₁₆	Serial I/O2 control register (SIO2CON)
001E₁₆	Watchdog timer control register (WDTCON)
001F₁₆	Serial I/O2 register (SIO2)

0020₁₆	Prescaler 12 (PRE12)
0021₁₆	Timer 1 (T1)
0022₁₆	Timer 2 (T2)
0023₁₆	Timer XY mode register (TM)
0024₁₆	Prescaler X (PREX)
0025₁₆	Timer X (TX)
0026₁₆	Prescaler Y (PREY)
0027₁₆	Timer Y (TY)
0028₁₆	Timer Z low-order (TZL)
0029₁₆	Timer Z high-order (TZH)
002A₁₆	Timer Z mode register (TZM)
002B₁₆	PWM control register (PWMCON)
002C₁₆	PWM prescaler (PREPWM)
002D₁₆	PWM register (PWM)
002E₁₆	
002F₁₆	Baud rate generator 3 (BRG3)
0030₁₆	Transmit/Receive buffer register 3 (TB3/RB3)
0031₁₆	Serial I/O3 status register (SIO3STS)
0032₁₆	Serial I/O3 control register (SIO3CON)
0033₁₆	UART3 control register (UART3CON)
0034₁₆	AD/DA control register (ADCON)
0035₁₆	AD conversion register 1 (AD1)
0036₁₆	DA1 conversion register (DA1)
0037₁₆	DA2 conversion register (DA2)
0038₁₆	AD conversion register 2 (AD2)
0039₁₆	Interrupt source selection register (INTSEL)
003A₁₆	Interrupt edge selection register (INTEDGE)
003B₁₆	CPU mode register (CPUM)
003C₁₆	Interrupt request register 1 (IREQ1)
003D₁₆	Interrupt request register 2 (IREQ2)
003E₁₆	Interrupt control register 1 (ICON1)
003F₁₆	Interrupt control register 2 (ICON2)

0FE0₁₆	Reserved **(Note 1)**
0FE1₁₆	Reserved **(Note 1)**
0FE2₁₆	Reserved **(Note 1)**
0FE3₁₆	Reserved **(Note 1)**
0FE4₁₆	Reserved **(Note 1)**
0FE5₁₆	Reserved **(Note 1)**
0FE6₁₆	Reserved **(Note 1)**
0FE7₁₆	Reserved **(Note 1)**
0FE8₁₆	Reserved **(Note 1)**
0FE9₁₆	Reserved **(Note 1)**
0FEA₁₆	Reserved **(Note 1)**
0FEB₁₆	Reserved **(Note 1)**
0FEC₁₆	Reserved **(Note 1)**
0FED₁₆	Reserved **(Note 1)**
0FEE₁₆	Reserved **(Note 1)**
0FEF₁₆	Reserved **(Note 1)**

0FF0₁₆	Port P0 pull-up control register (PULL0)
0FF1₁₆	Port P1 pull-up control register (PULL1)
0FF2₁₆	Port P2 pull-up control register (PULL2)
0FF3₁₆	Port P3 pull-up control register (PULL3)
0FF4₁₆	Port P4 pull-up control register (PULL4)
0FF5₁₆	Port P5 pull-up control register (PULL5)
0FF6₁₆	Port P6 pull-up control register (PULL6)

Notes 1: Do not write any data to these addresses, because these areas are reserved.
2: Do not access to the SFR area including nothing.

Fig 12. Memory map of special function register (SFR)

I/O PORTS

The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input port or output port.
When "0" is written to the bit corresponding to a pin, that pin becomes an input pin. When "1" is written to that bit, that pin becomes an output pin.

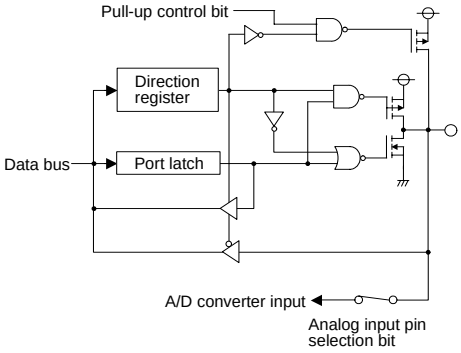
If data is read from a pin which is set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.
By setting the port P0 pull-up control register (address $0FF0_{16}$) to the port P6 pull-up control register (address $0FF6_{16}$) ports can control pull-up with a program. However, the contents of these registers do not affect ports programmed as the output ports.

Table 6 I/O port function

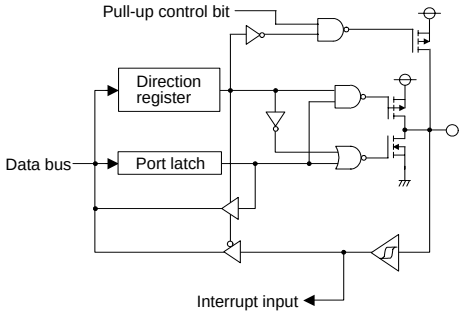
Pin	Name	Input/ Output	I/O Structure	Non-Port Function	Related SFRs	Ref. No.
$P0_0$/AN_8–$P0_7$/AN_{15}	Port P0	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	A/D converter input	AD/DA control register	(1)
$P1_0$/INT_{41} $P1_1$/INT_{01}	Port P1			External interrupt input	Interrupt edge selection register	(2)
$P1_2$–$P1_7$						(3)
$P2_0$(LED_0)– $P2_7$(LED_7)	Port P2					
$P3_0$/DA_1 $P3_1$/DA_2	Port P3			D/A converter output	AD/DA control register	(4)
$P3_2$, $P3_3$			CMOS compatible input level N-channel open-drain output			(5)
$P3_4$/RxD_3 $P3_5$/TxD_3 $P3_6$/$SCLK_3$ $P3_7$/$\overline{SRDY_3}$			CMOS compatible input level CMOS 3-state output	Serial I/O3 function I/O	Serial I/O3 control register UART3 control register	(6) (7) (8) (9)
$P4_0$/INT_{40}/$XCOUT$ $P4_1$/INT_{00}/$XCIN$	Port P4			External interrupt input Sub-clock generating circuit	Interrupt edge selection register CPU mode register	(10) (11)
$P4_2$/INT_1 $P4_3$/INT_2				External interrupt input	Interrupt edge selection register	(2)
$P4_4$/RxD_1 $P4_5$/TxD_1 $P4_6$/$SCLK_1$				Serial I/O1 function I/O	Serial I/O1 control register UART1 control register	(6) (7) (8)
$P4_7$/$\overline{SRDY_1}$/$CNTR_2$				Serial I/O1 function I/O Timer Z function I/O	Serial I/O1 control register Timer Z mode register	(12)
$P5_0$/SIN_2 $P5_1$/$SOUT_2$ $P5_2$/$SCLK_2$ $P5_3$/$\overline{SRDY_2}$	Port P5			Serial I/O2 function I/O	Serial I/O2 control register	(13) (14) (15) (16)
$P5_4$/$CNTR_0$ $P5_5$/$CNTR_1$				Timer X, Y function I/O	Timer XY mode register	(17)
$P5_6$/PWM				PWM output	PWM control register	(18)
$P5_7$/INT_3				External interrupt input	Interrupt edge selection register	(2)
$P6_0$/AN_0–$P6_7$/AN_7	Port P6			A/D converter input	AD/DA control register	(1)

NOTES:
1. Refer to the applicable sections how to use double-function ports as function I/O ports.
2. Make sure that the input level at each pin is either 0 V or V_{CC} during execution of the STP instruction.
   When an input level is at an intermediate potential, a current will flow from V_{CC} to V_{SS} through the input-stage gate.

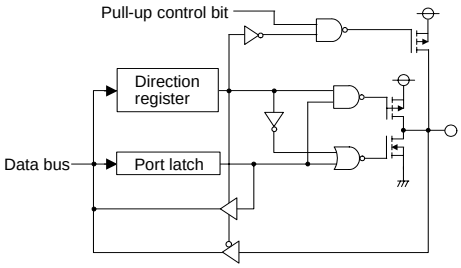
(1) Ports P0, P6



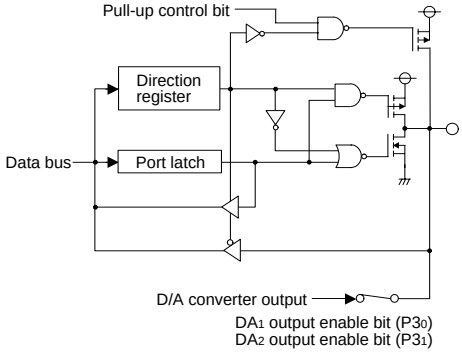
(2) Ports P10, P11, P42, P43, P57



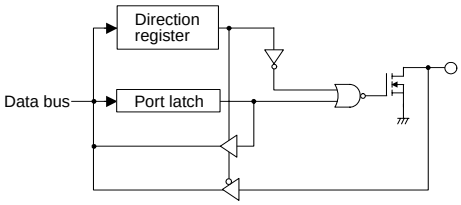
(3) Ports P12 to P17, P2



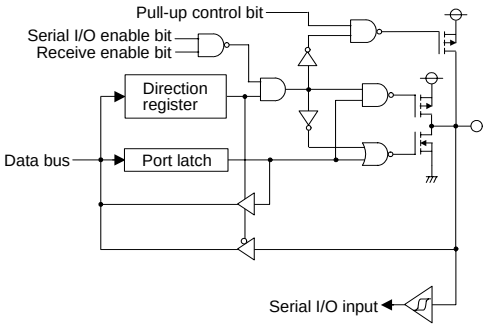
(4) Ports P30, P31



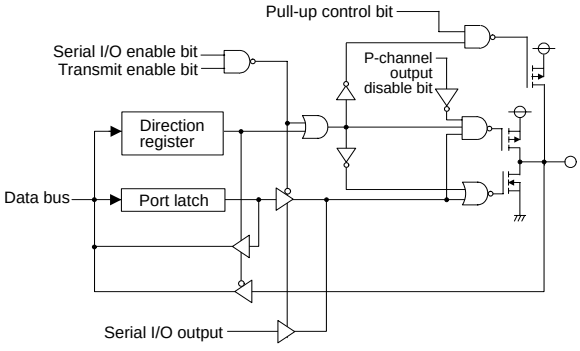
(5) Ports P32, P33



(6) Ports P34, P44



(7) Ports P35, P45



(8) Ports P36, P46

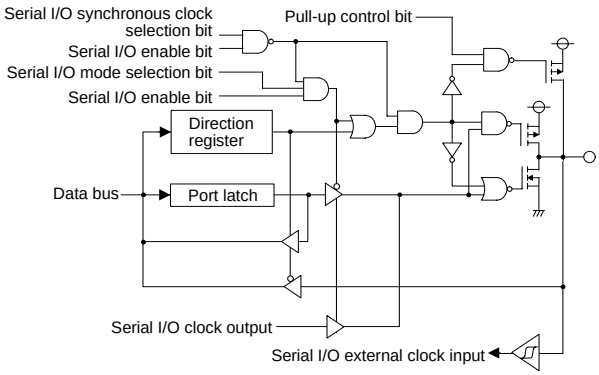
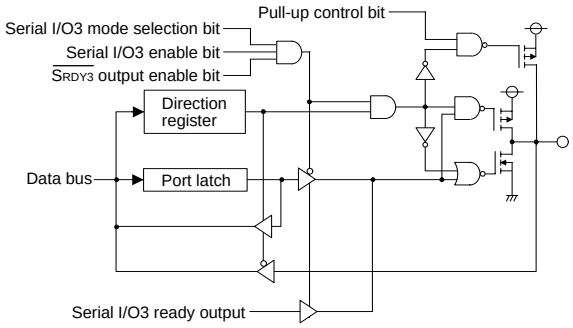
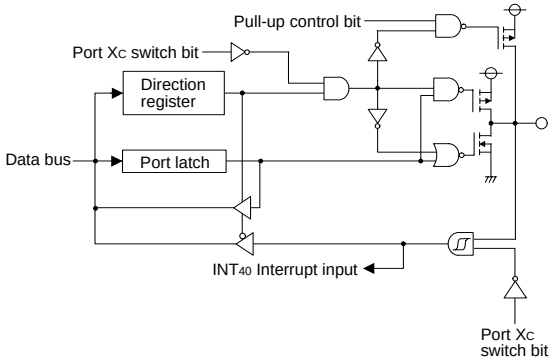


Fig 13. Port block diagram (1)

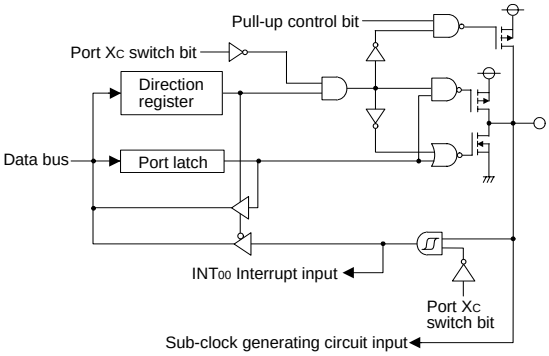
(9) Port P3$_7$



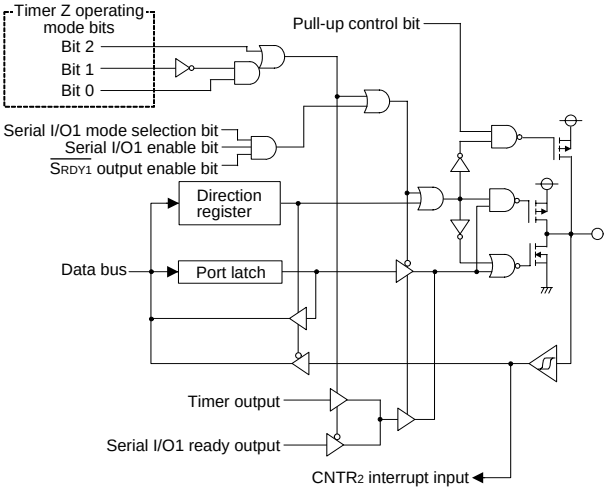
(10) Port P4$_0$



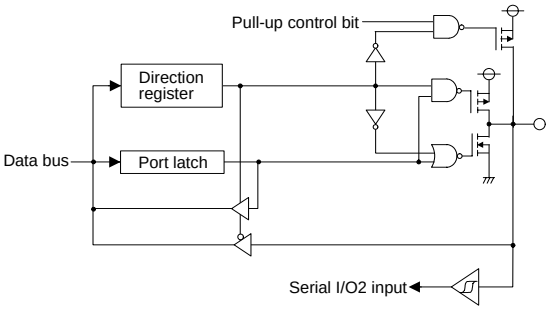
(11) Port P4$_1$



(12) Port P4$_7$



(13) Port P5$_0$



(14) Port P5$_1$

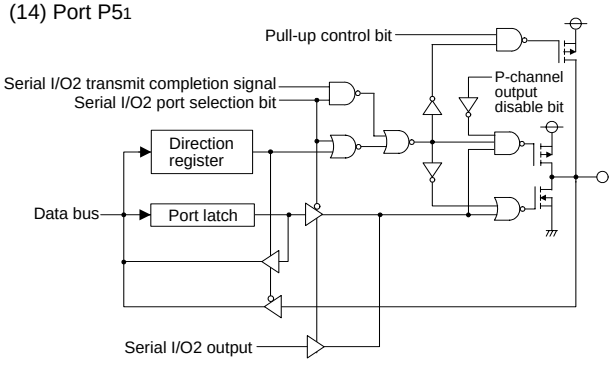


Fig 14. Port block diagram (2)

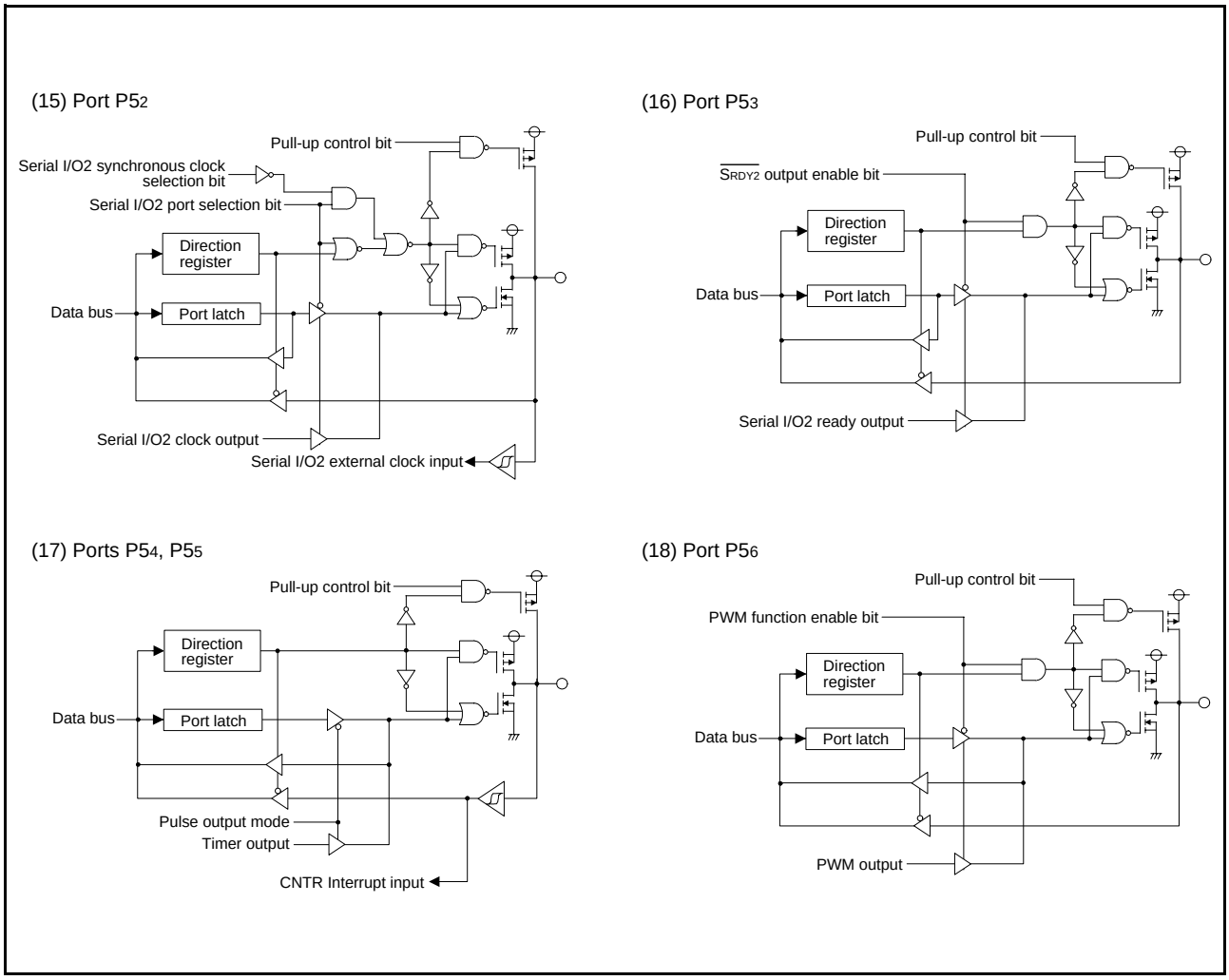
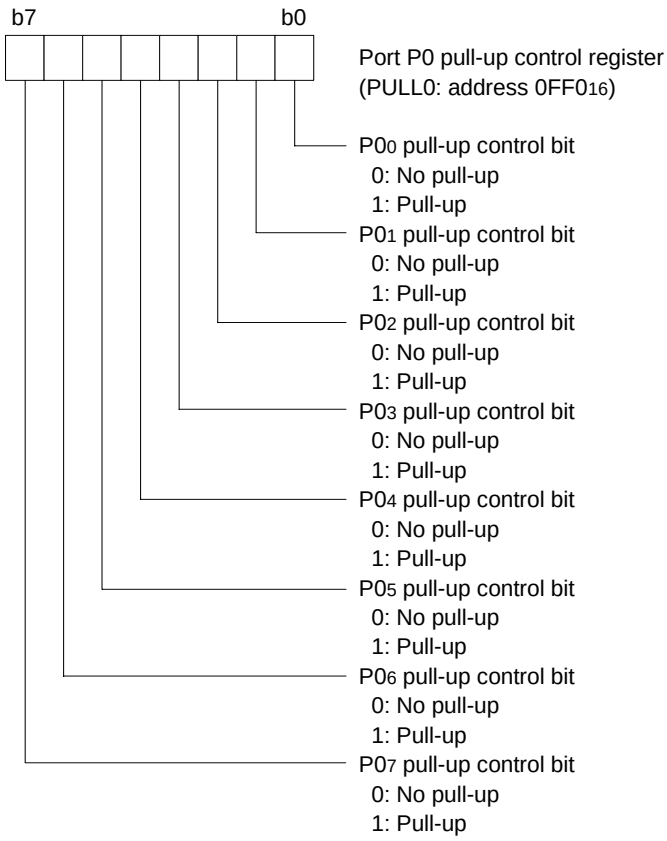
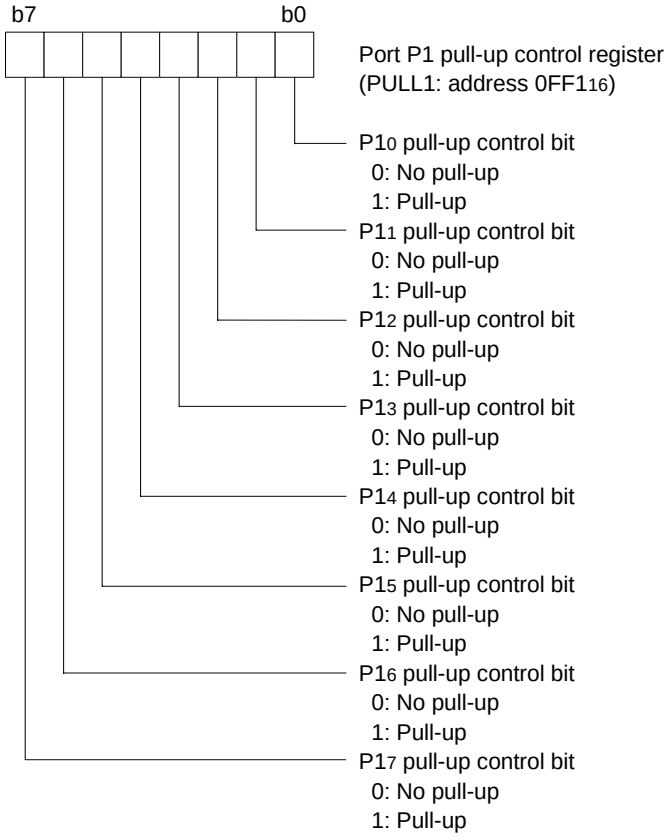


Fig 15. Port block diagram (3)

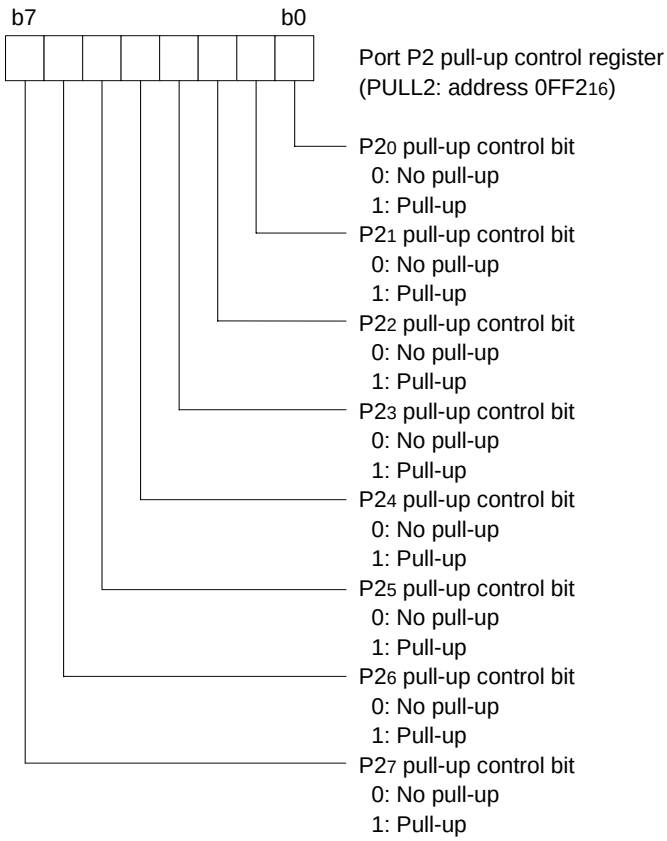


Note: Pull-up control is valid when the corresponding bit of the port direction register is "0" (input). When that bit is "1" (output), pull-up cannot be set to the port of which pull-up is selected.

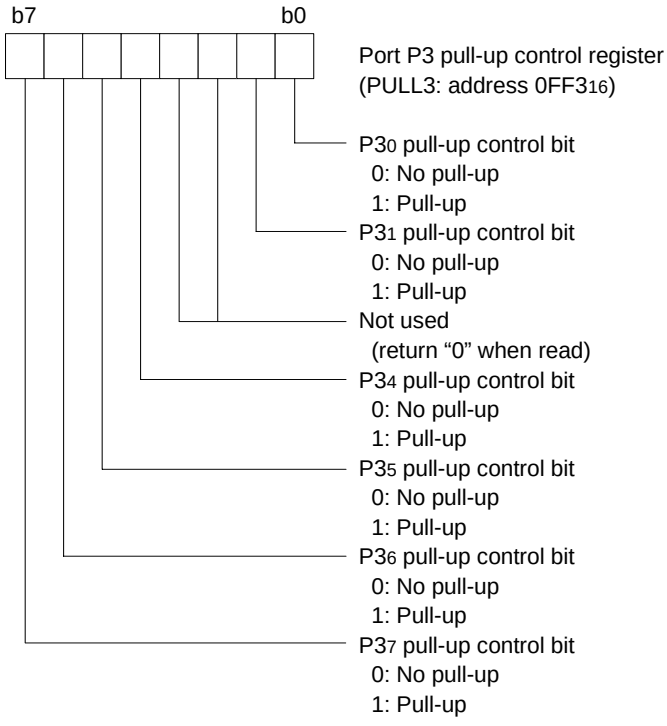


Note: Pull-up control is valid when the corresponding bit of the port direction register is "0" (input). When that bit is "1" (output), pull-up cannot be set to the port of which pull-up is selected.

Fig 16. Structure of port pull-up control register (1)

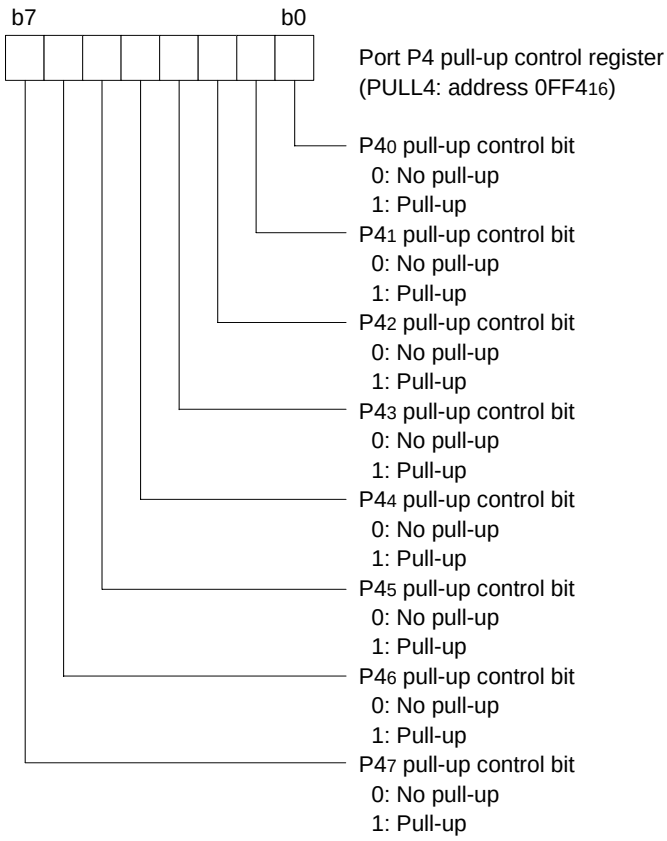


Note: Pull-up control is valid when the corresponding bit of the port direction register is "0" (input). When that bit is "1" (output), pull-up cannot be set to the port of which pull-up is selected.

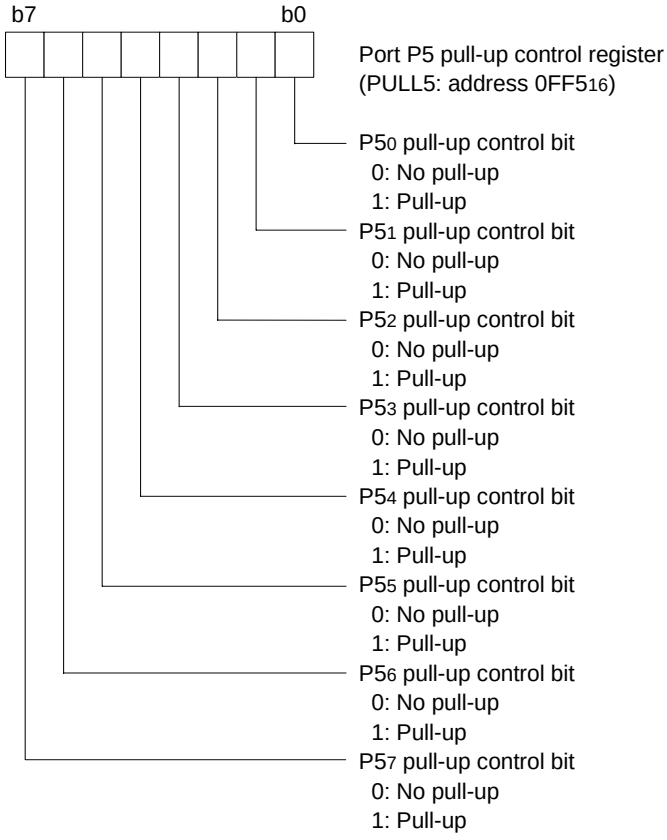


Note: Pull-up control is valid when the corresponding bit of the port direction register is "0" (input). When that bit is "1" (output), pull-up cannot be set to the port of which pull-up is selected.

Fig 17. Structure of port pull-up control register (2)



Note: Pull-up control is valid when the corresponding bit of the port direction register is "0" (input). When that bit is "1" (output), pull-up cannot be set to the port of which pull-up is selected.



Note: Pull-up control is valid when the corresponding bit of the port direction register is "0" (input). When that bit is "1" (output), pull-up cannot be set to the port of which pull-up is selected.

Fig 18. Structure of port pull-up control register (3)

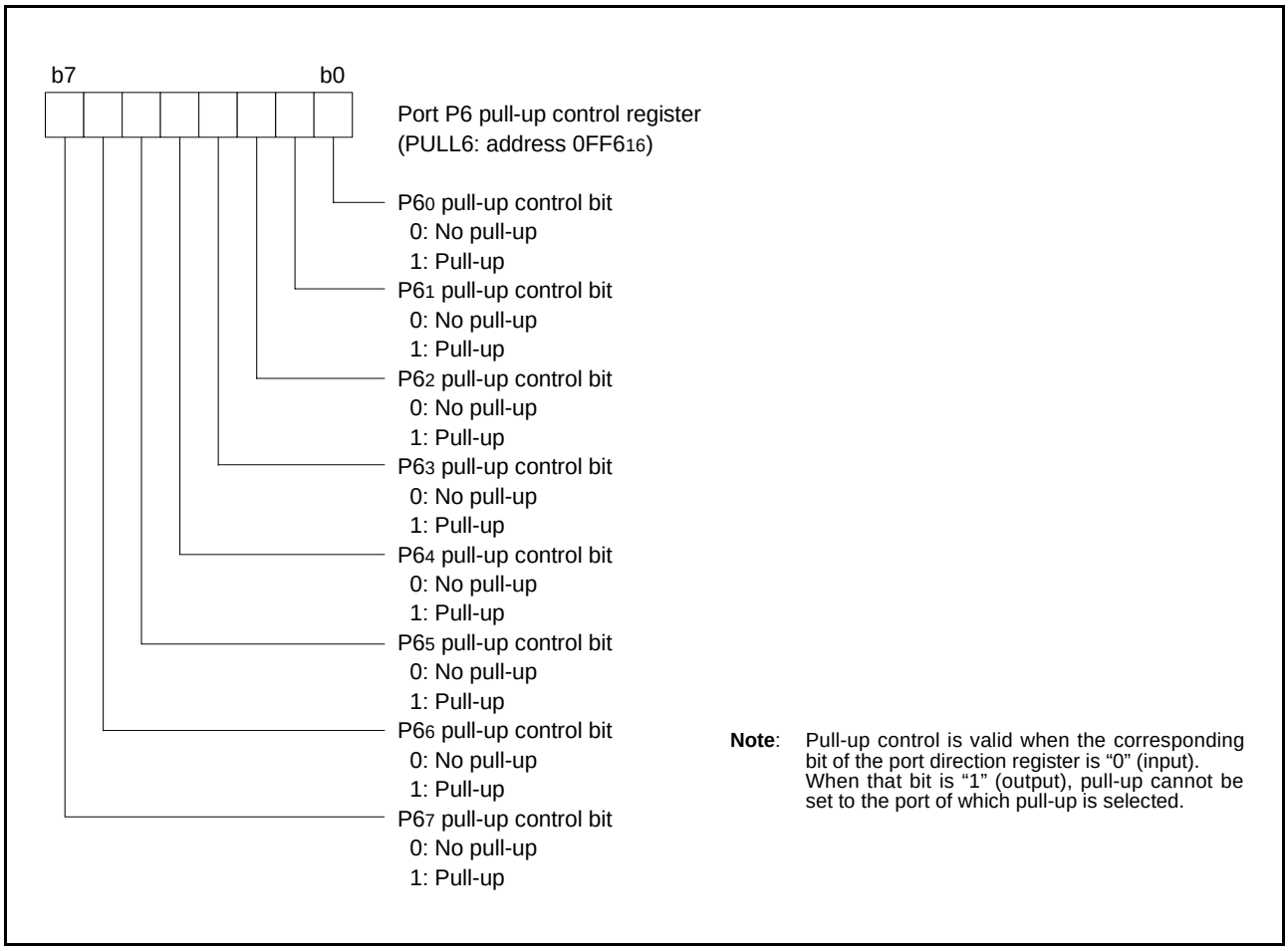


Fig 19. Structure of port pull-up control register (4)

Termination of unused pins

• Termination of common pins

I/O ports: Select an input port or an output port and follow each processing method.
In addition, it is recommended that related registers be overwritten periodically to prevent malfunctions, etc.

Output ports: Open.

Input ports: If the input level become unstable, through current flow to an input circuit, and the power supply current may increase.
Especially, when expecting low consumption current (at STP or WIT instruction execution etc.), pull-up or pull-down input ports to prevent through current (built-in resistor can be used).
We recommend processing unused pins through a resistor which can secure $I_{OH(avg)}$ or $I_{OL(avg)}$.
Because, when an I/O port or a pin which have an output function is selected as an input port, it may operate as an output port by incorrect operation etc.

Table 7 Termination of unused pins

Pins	Termination
P0, P1, P2, P3, P4, P5, P6	• Set to the input mode and connect each to V_{CC} or V_{SS} through a resistor of 1 kΩ to 10 kΩ. • Set to the output mode and open at “L” or “H” output state.
V_{REF}	Connect to V_{CC} or V_{SS} (GND).
AV_{SS}	Connect to V_{SS} (GND).
X_{OUT}	Open (only when using external clock)

INTERRUPTS

The 3803 group (Spec.H QzROM version) interrupts are vector interrupts with a fixed priority scheme, and generated by 16 sources among 21 sources: 8 external, 12 internal, and 1 software.

The interrupt sources, vector addresses(1), and interrupt priority are shown in Table 8.

Each interrupt except the BRK instruction interrupt has the interrupt request bit and the interrupt enable bit. These bits and the interrupt disable flag (I flag) control the acceptance of interrupt requests. Figure 20 shows an interrupt control diagram.

An interrupt requests is accepted when all of the following conditions are satisfied:

- Interrupt disable flag.....“0”
- Interrupt request bit.....“1”
- Interrupt enable bit.....“1”

Though the interrupt priority is determined by hardware, priority processing can be performed by software using the above bits and flag.

Table 8 Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses(1)		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset(2)	1	FFFD16	FFFC16	At reset	Non-maskable
INT0	2	FFFB16	FFFA16	At detection of either rising or falling edge of INT0 input	External interrupt (active edge selectable)
Timer Z				At timer Z underflow	
INT1	3	FFF916	FFF816	At detection of either rising or falling edge of INT1 input	External interrupt (active edge selectable)
Serial I/O1 reception	4	FFF716	FFF616	At completion of serial I/O1 data reception	Valid when serial I/O1 is selected
Serial I/O1 transmission	5	FFF516	FFF416	At completion of serial I/O1 transmission shift or when transmission buffer is empty	Valid when serial I/O1 is selected
Timer X	6	FFF316	FFF216	At timer X underflow	
Timer Y	7	FFF116	FFF016	At timer Y underflow	
Timer 1	8	FFEF16	FFEE16	At timer 1 underflow	STP release timer underflow
Timer 2	9	FFED16	FFEC16	At timer 2 underflow	
CNTR0	10	FFEB16	FFEA16	At detection of either rising or falling edge of CNTR0 input	External interrupt (active edge selectable)
CNTR1	11	FFE916	FFE816	At detection of either rising or falling edge of CNTR1 input	External interrupt (active edge selectable)
Serial I/O3 reception				At completion of serial I/O3 data reception	Valid when serial I/O3 is selected
Serial I/O2	12	FFE716	FFE616	At completion of serial I/O2 data transmission or reception	Valid when serial I/O2 is selected
Timer Z				At timer Z underflow	
INT2	13	FFE516	FFE416	At detection of either rising or falling edge of INT2 input	External interrupt (active edge selectable)
INT3	14	FFE316	FFE216	At detection of either rising or falling edge of INT3 input	External interrupt (active edge selectable)
INT4	15	FFE116	FFE016	At detection of either rising or falling edge of INT4 input	External interrupt (active edge selectable)
CNTR2				At detection of either rising or falling edge of CNTR2 input	External interrupt (active edge selectable)
A/D conversion	16	FFDF16	FFDE16	At completion of A/D conversion	
Serial I/O3 transmission				At completion of serial I/O3 transmission shift or when transmission buffer is empty	Valid when serial I/O3 is selected
BRK instruction	17	FFDD16	FFDC16	At BRK instruction execution	Non-maskable software interrupt

NOTES:
1. Vector addresses contain interrupt jump destination addresses.
2. Reset function in the same way as an interrupt with the highest priority.

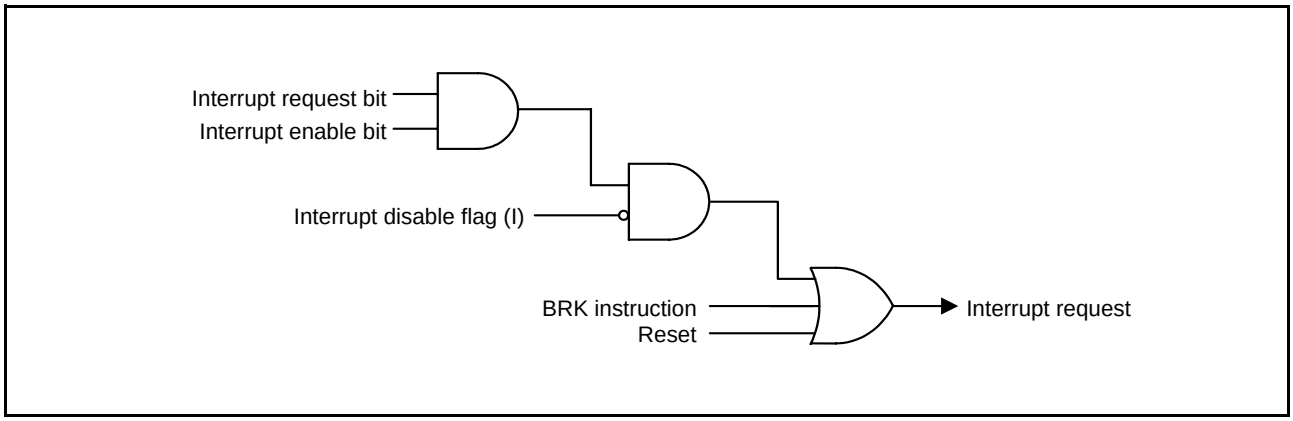


Fig 20. Interrupt control diagram

• Interrupt Disable Flag

The interrupt disable flag is assigned to bit 2 of the processor status register. This flag controls the acceptance of all interrupt requests except for the BRK instruction. When this flag is set to "1", the acceptance of interrupt requests is disabled. When it is set to "0", acceptance of interrupt requests is enabled. This flag is set to "1" with the SET instruction and set to "0" with the CLI instruction.

When an interrupt request is accepted, the contents of the processor status register are pushed onto the stack while the interrupt disable flag remains set to "0". Subsequently, this flag is automatically set to "1" and multiple interrupts are disabled. To use multiple interrupts, set this flag to "0" with the CLI instruction within the interrupt processing routine.

The contents of the processor status register are popped off the stack with the RTI instruction.

• Interrupt Request Bits

Once an interrupt request is generated, the corresponding interrupt request bit is set to "1" and remains "1" until the request is accepted. When the request is accepted, this bit is automatically set to "0".

Each interrupt request bit can be set to "0", but cannot be set to "1", by software.

• Interrupt Enable Bits

The interrupt enable bits control the acceptance of the corresponding interrupt requests. When an interrupt enable bit is set to "0", the acceptance of the corresponding interrupt request is disabled. If an interrupt request occurs in this condition, the corresponding interrupt request bit is set to "1", but the interrupt request is not accepted. When an interrupt enable bit is set to "1", acceptance of the corresponding interrupt request is enabled.

Each interrupt enable bit can be set to "0" or "1" by software.

The interrupt enable bit for an unused interrupt should be set to "0".

• Interrupt Source Selection

Any of the following combinations can be selected by the interrupt source selection register (0039_{16}).

1. INT_0 or timer Z
2. $CNTR_1$ or Serial I/O3 reception
3. Serial I/O2 or timer Z
4. INT_4 or $CNTR_2$
5. A/D conversion or serial I/O3 transmission

• External Interrupt Pin Selection

For external interrupts INT_0 and INT_4, the INT_0, INT_4 interrupt switch bit in the interrupt edge selection register (bit 6 of address $003A_{16}$) can be used to select INT_{00} and INT_{40} pin input or INT_{01} and INT_{41} pin input.

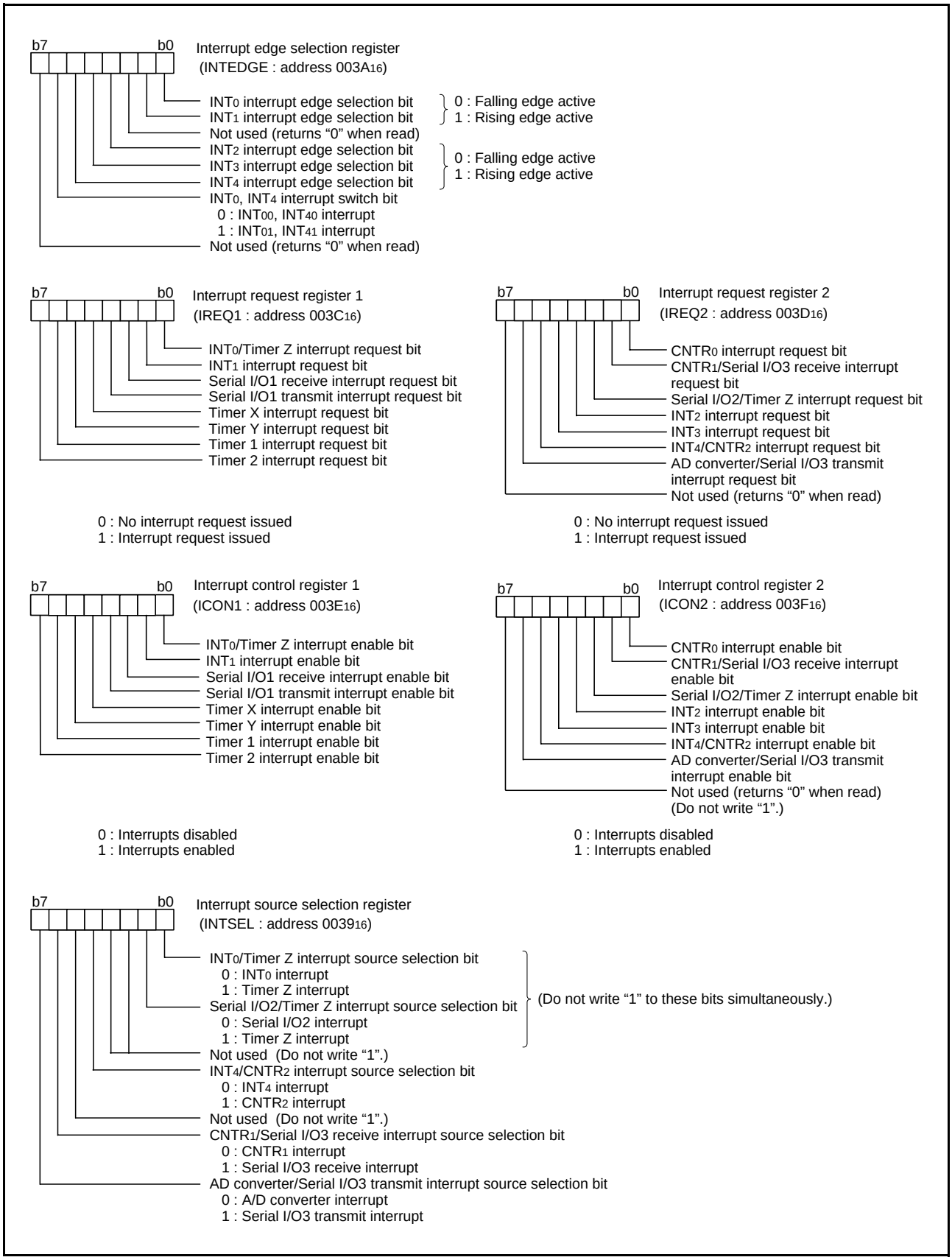


Fig 21. Structure of interrupt-related registers

• Interrupt Request Generation, Acceptance, and Handling

Interrupts have the following three phases.

(i) Interrupt Request Generation
An interrupt request is generated by an interrupt source (external interrupt signal input, timer underflow, etc.) and the corresponding request bit is set to "1".

(ii) Interrupt Request Acceptance
Based on the interrupt acceptance timing in each instruction cycle, the interrupt control circuit determines acceptance conditions (interrupt request bit, interrupt enable bit, and interrupt disable flag) and interrupt priority levels for accepting interrupt requests. When two or more interrupt requests are generated simultaneously, the highest priority interrupt is accepted. The value of interrupt request bit for an unaccepted interrupt remains the same and acceptance is determined at the next interrupt acceptance timing point.

(iii) Handling of Accepted Interrupt Request
The accepted interrupt request is processed.

Figure 22 shows the time up to execution in the interrupt processing routine, and Figure 23 shows the interrupt sequence. Figure 24 shows the timing of interrupt request generation, interrupt request bit, and interrupt request acceptance.

• Interrupt Handling Execution

When interrupt handling is executed, the following operations are performed automatically.

(1) Once the currently executing instruction is completed, an interrupt request is accepted.
(2) The contents of the program counters and the processor status register at this point are pushed onto the stack area in order from 1 to 3.
1. High-order bits of program counter (PCH)
2. Low-order bits of program counter (PCL)
3. Processor status register (PS)
(3) Concurrently with the push operation, the jump address of the corresponding interrupt (the start address of the interrupt processing routine) is transferred from the interrupt vector to the program counter.
(4) The interrupt request bit for the corresponding interrupt is set to "0". Also, the interrupt disable flag is set to "1" and multiple interrupts are disabled.
(5) The interrupt routine is executed.
(6) When the RTI instruction is executed, the contents of the registers pushed onto the stack area are popped off in the order from 3 to 1. Then, the routine that was before running interrupt processing resumes.

As described above, it is necessary to set the stack pointer and the jump address in the vector area corresponding to each interrupt to execute the interrupt processing routine.

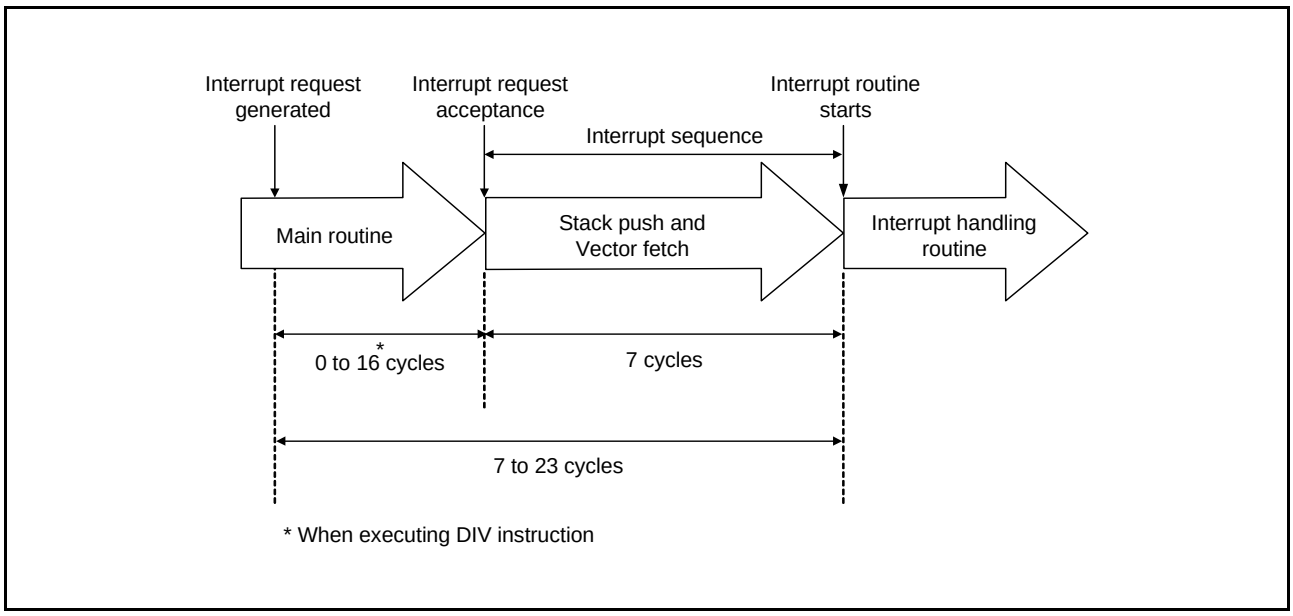
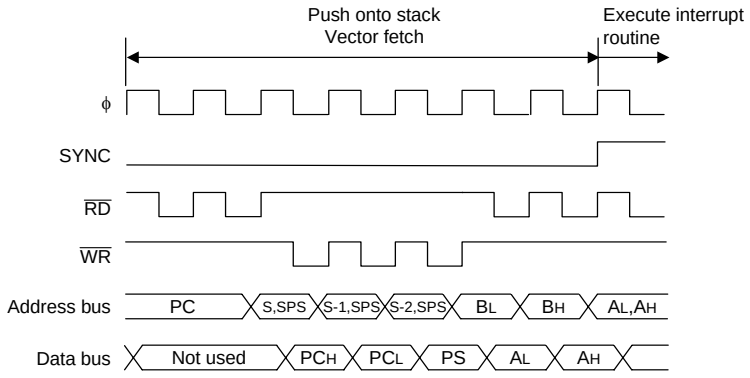
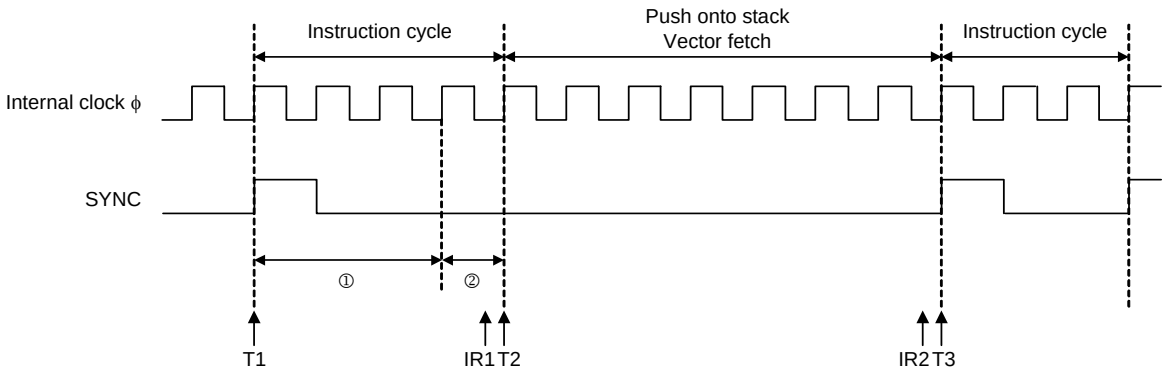


Fig 22. Time up to execution in interrupt routine



SYNC : CPU operation code fetch cycle
(This is an internal signal that cannot be observed from the external unit.)
BL, BH: Vector address of each interrupt
AL, AH: Jump destination address of each interrupt
SPS : "00_{16}" or "01_{16}"
([SPS] is a page selected by the stack page selection bit of CPU mode register.)

Fig 23. Interrupt sequence



T1 T2 T3 : Interrupt acceptance timing points
IR1 IR2 : Timings points at which the interrupt request bit is set to "1".

Note : Period 2 indicates the last ϕ cycle during one instruction cycle.

(1) The interrupt request bit for an interrupt request generated during period 1 is set to "1" at timing point IR1.
(2) The interrupt request bit for an interrupt request generated during period 2 is set to "1" at timing point IR1 or IR2. The timing point at which the bit is set to "1" varies depending on conditions. When two or more interrupt requests are generated during the period 2, each request bit may be set to "1" at timing point IR1 or IR2 separately.

Fig 24. Timing of interrupt request generation, interrupt request bit, and interrupt acceptance

<Notes>

The interrupt request bit may be set to "1" in the following cases.

- When setting the external interrupt active edge
  Related bits:
  INT_0 interrupt edge selection bit
  (bit 0 of interrupt edge selection register (address $003A_{16}$))
  INT_1 interrupt edge selection bit
  (bit 1 of interrupt edge selection register (address $003A_{16}$))
  INT_2 interrupt edge selection bit
  (bit 3 of interrupt edge selection register (address $003A_{16}$))
  INT_3 interrupt edge selection bit
  (bit 4 of interrupt edge selection register (address $003A_{16}$))
  INT_4 interrupt edge selection bit
  (bit 5 of interrupt edge selection register (address $003A_{16}$))
  $CNTR_0$ activate edge switch bit
  (bit 2 of timer XY mode register (address 0023_{16}))
  $CNTR_1$ activate edge switch bit
  (bits 6 of timer XY mode register (address 0023_{16}))
  $CNTR_2$ activate edge switch bit
  (bits 5 of timer Z mode register (address $002A_{16}$))

- When switching the interrupt sources of an interrupt vector address where two or more interrupt sources are assigned
  Related bits:
  INT_0, INT_4 interrupt switch bit
  (bit 6 of interrupt edge selection register (address $003A_{16}$))
  INT_0/Timer Z interrupt source selection bit
  (bit 0 of interrupt source selection register (address 0039_{16}))
  Serial I/O2/Timer Z interrupt source selection bit
  (bit 1 of interrupt source selection register (address 0039_{16}))
  INT_4/$CNTR_2$ interrupt source selection bit
  (bit 4 of interrupt source selection register (address 0039_{16}))
  $CNTR_1$/Serial I/O3 receive interrupt source selection bit
  (bit 6 of interrupt source selection register (address 0039_{16}))
  AD conversion/Serial I/O3 transmit interrupt source selection bit
  (bit 6 of interrupt source selection register (address 0039_{16}))

If it is not necessary to generate an interrupt synchronized with these settings, take the following sequence.

(1) Set the corresponding enable bit to "0" (disabled).
(2) Set the interrupt edge selection bit (the active edge switch bit) or the interrupt source bit.
(3) Set the corresponding interrupt request bit to "0" after one or more instructions have been executed.
(4) Set the corresponding interrupt enable bit to "1" (enabled).

TIMERS

8-bit Timers

The 3803 group (Spec.H QzROM version) has four 8-bit timers: timer 1, timer 2, timer X, and timer Y.
The timer 1 and timer 2 use one prescaler in common, and the timer X and timer Y use each prescaler. Those are 8-bit prescalers. Each of the timers and prescalers has a timer latch or a prescaler latch.
The division ratio of each timer or prescaler is given by 1/(n + 1), where n is the value in the corresponding timer or prescaler latch. All timers are down-counters. When the timer reaches "00$_{16}$", an underflow occurs at the next count pulse and the contents of the corresponding timer latch are reloaded into the timer and the count is continued. When the timer underflows, the interrupt request bit corresponding to that timer is set to "1".

• Timer divider

The divider count source is switched by the main clock division ratio selection bits of CPU mode register (bits 7 and 6 at address 003B$_{16}$). When these bits are "00" (high-speed mode) or "01" (middle-speed mode), X_{IN} is selected. When these bits are "10" (low-speed mode), X_{CIN} is selected.

• Prescaler 12

The prescaler 12 counts the output of the timer divider. The count source is selected by the timer 12, X count source selection register among 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512, 1/1024 of f(X_{IN}) or f(X_{CIN}).

• Timer 1 and Timer 2

The timer 1 and timer 2 counts the output of prescaler 12 and periodically set the interrupt request bit.

• Prescaler X and prescaler Y

The prescaler X and prescaler Y count the output of the timer divider or f(X_{CIN}). The count source is selected by the timer 12, X count source selection register (address 000E$_{16}$) and the timer Y, Z count source selection register (address 000F$_{16}$) among 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512, and 1/1024 of f(X_{IN}) or f(X_{CIN}); and f(X_{CIN}).

• Timer X and Timer Y

The timer X and timer Y can each select one of four operating modes by setting the timer XY mode register (address 0023$_{16}$).

(1) Timer mode

• Mode selection

This mode can be selected by setting "00" to the timer X operating mode bits (bits 1 and 0) and the timer Y operating mode bits (bits 5 and 4) of the timer XY mode register (address 0023$_{16}$).

• Explanation of operation

The timer count operation is started by setting "0" to the timer X count stop bit (bit 3) and the timer Y count stop bit (bit 7) of the timer XY mode register (address 0023$_{16}$).
When the timer reaches "00$_{16}$", an underflow occurs at the next count pulse and the contents of timer latch are reloaded into the timer and the count is continued.

(2) Pulse Output Mode

• Mode selection

This mode can be selected by setting "01" to the timer X operating mode bits (bits 1 and 0) and the timer Y operating mode bits (bits 5 and 4) of the timer XY mode register (address 0023$_{16}$).

• Explanation of operation

The operation is the same as the timer mode's. Moreover the pulse which is inverted each time the timer underflows is output from $CNTR_0$/$CNTR_1$ pin. Regardless of the timer counting or not the output of $CNTR_0$/$CNTR_1$ pin is initialized to the level of specified by their active edge switch bits when writing to the timer. When the $CNTR_0$ active edge switch bit (bit 2) and the $CNTR_1$ active edge switch bit (bit 6) of the timer XY mode register (address 0023$_{16}$) is "0", the output starts with "H" level. When it is "1", the output starts with "L" level.
Switching the $CNTR_0$ or $CNTR_1$ active edge switch bit will reverse the output level of the corresponding $CNTR_0$ or $CNTR_1$ pin.

• Precautions

Set the double-function port of $CNTR_0$/$CNTR_1$ pin and port $P5_4$/$P5_5$ to output in this mode.

(3) Event Counter Mode

• Mode selection

This mode can be selected by setting "10" to the timer X operating mode bits (bits 1 and 0) and the timer Y operating mode bits (bits 5 and 4) of the timer XY mode register (address 0023$_{16}$).

• Explanation of operation

The operation is the same as the timer mode's except that the timer counts signals input from the $CNTR_0$ or $CNTR_1$ pin. The valid edge for the count operation depends on the $CNTR_0$ active edge switch bit (bit 2) or the $CNTR_1$ active edge switch bit (bit 6) of the timer XY mode register (address 0023$_{16}$). When it is "0", the rising edge is valid. When it is "1", the falling edge is valid.

• Precautions

Set the double-function port of $CNTR_0$/$CNTR_1$ pin and port $P5_4$/$P5_5$ to input in this mode.

(4) Pulse Width Measurement Mode

• Mode selection

This mode can be selected by setting "11" to the timer X operating mode bits (bits 1 and 0) and the timer Y operating mode bits (bits 5 and 4) of the timer XY mode register (address 0023_{16}).

• Explanation of operation

When the $CNTR_0$ active edge switch bit (bit 2) or the $CNTR_1$ active edge switch bit (bit 6) of the timer XY mode register (address 0023_{16}) is "1", the timer counts during the term of one falling edge of $CNTR_0$/$CNTR_1$ pin input until the next rising edge of input ("L" term). When it is "0", the timer counts during the term of one rising edge input until the next falling edge input ("H" term).

• Precautions

Set the double-function port of $CNTR_0$/$CNTR_1$ pin and port $P5_4$/$P5_5$ to input in this mode.

The count operation can be stopped by setting "1" to the timer X count stop bit (bit 3) and the timer Y count stop bit (bit 7) of the timer XY mode register (address 0023_{16}). The interrupt request bit is set to "1" each time the timer underflows.

• Precautions when switching count source

When switching the count source by the timer 12, X and Y count source selection bits, the value of timer count is altered in inconsiderable amount owing to generating of thin pulses on the count input signals.

Therefore, select the timer count source before setting the value to the prescaler and the timer.

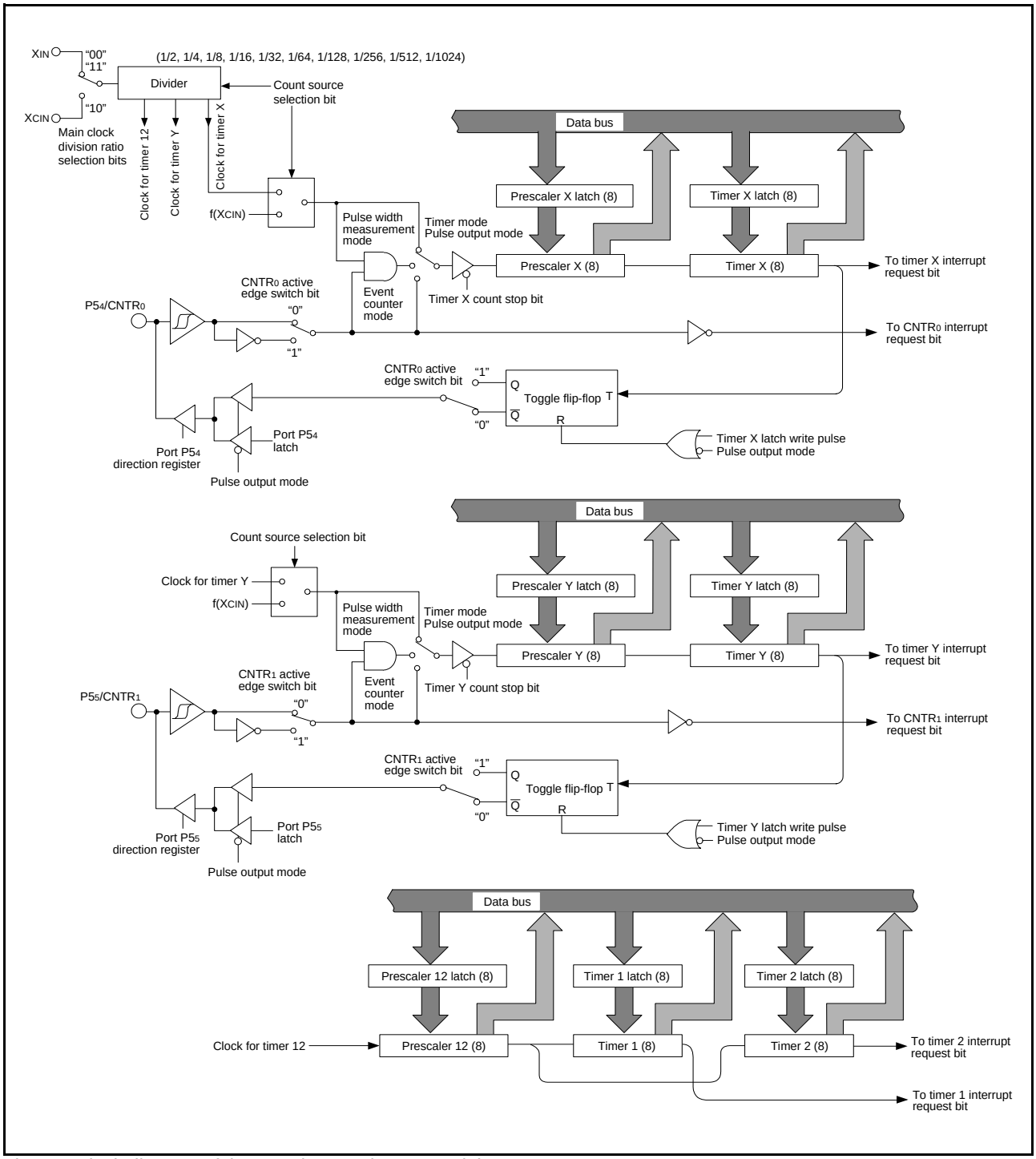


Fig 25. Block diagram of timer X, timer Y, timer 1, and timer 2

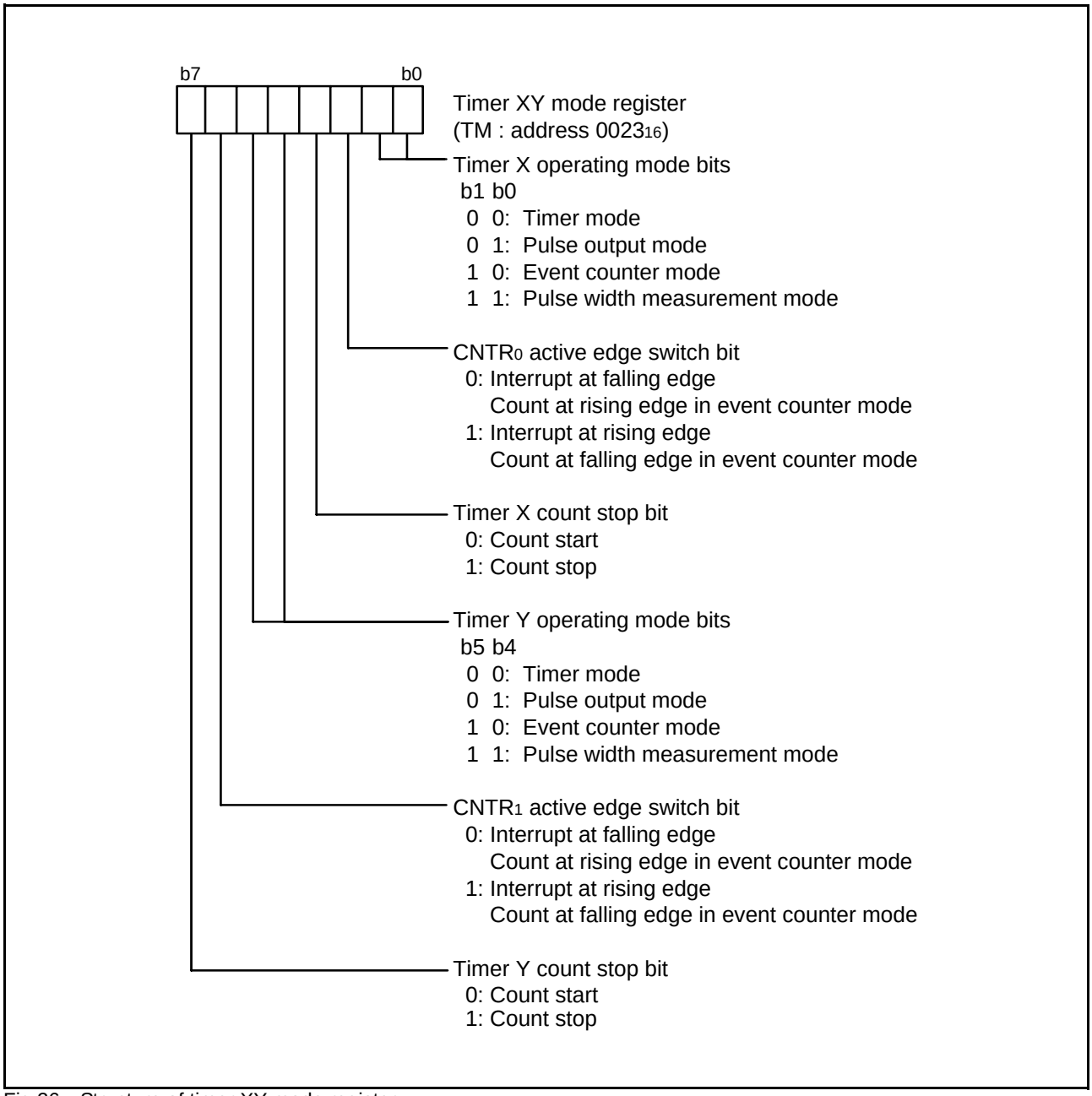


Fig 26. Structure of timer XY mode register

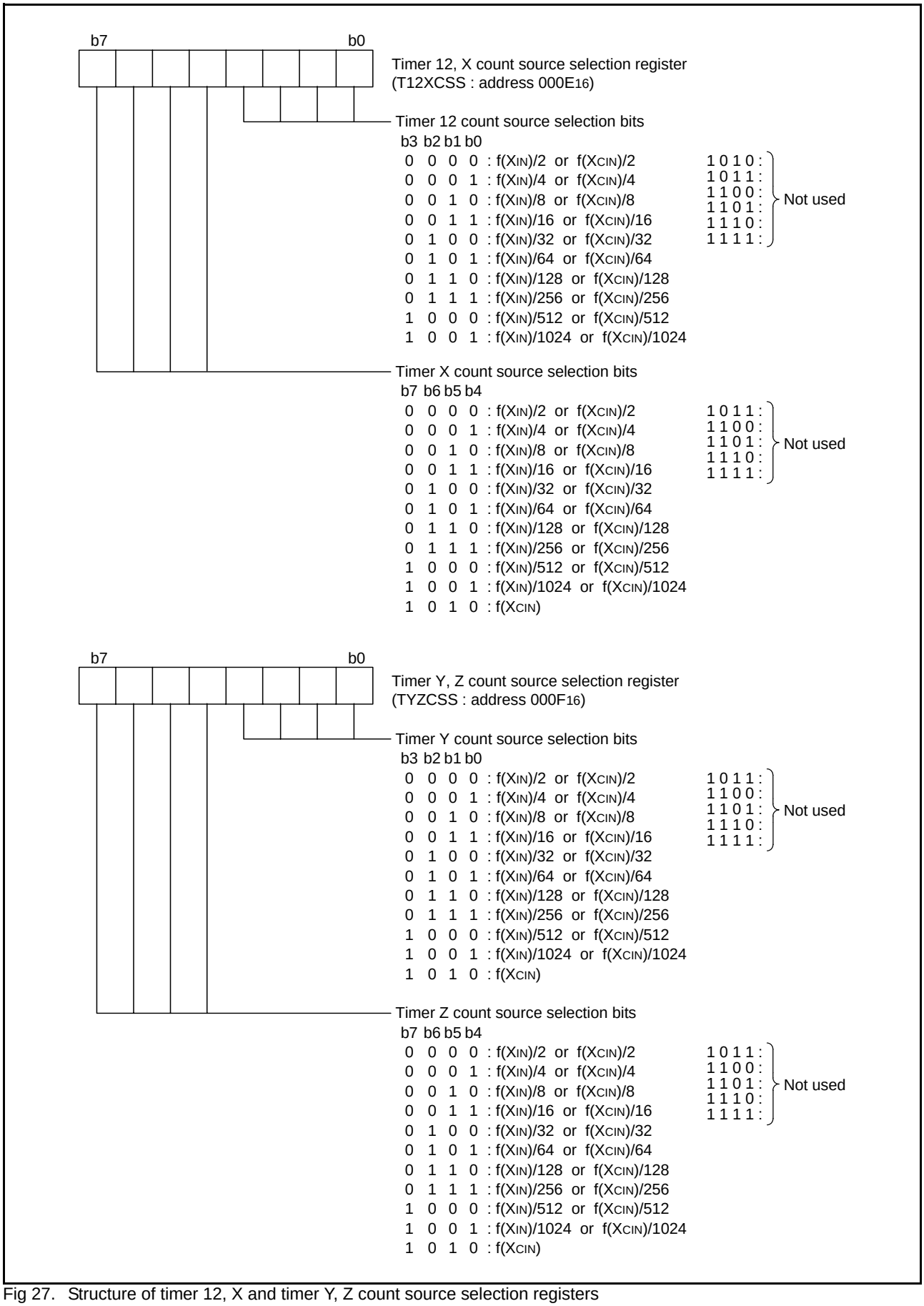


Fig 27. Structure of timer 12, X and timer Y, Z count source selection registers

16-bit Timer

The timer Z is a 16-bit timer. When the timer reaches "0000$_{16}$", an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When the timer underflows, the interrupt request bit corresponding to the timer Z is set to "1".
When reading/writing to the timer Z, perform reading/writing to both the high-order byte and the low-order byte. When reading the timer Z, read from the high-order byte first, followed by the low-order byte. Do not perform the writing to the timer Z between read operation of the high-order byte and read operation of the low-order byte. When writing to the timer Z, write to the low-order byte first, followed by the high-order byte. Do not perform the reading to the timer Z between write operation of the low-order byte and write operation of the high-order byte.
The timer Z can select the count source by the timer Z count source selection bits of timer Y, Z count source selection register (bits 7 to 4 at address 000F$_{16}$).
Timer Z can select one of seven operating modes by setting the timer Z mode register (address 002A$_{16}$).

(1) Timer mode

• Mode selection

This mode can be selected by setting "000" to the timer Z operating mode bits (bits 2 to 0) and setting "0" to the timer/event counter mode switch bit (b7) of the timer Z mode register (address 002A$_{16}$).

• Count source selection

In high- or middle-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(X$_{IN}$); or f(X$_{CIN}$) can be selected as the count source.
In low-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(X$_{CIN}$); or f(X$_{CIN}$) can be selected as the count source.

• Interrupt

When an underflow occurs, the INT$_0$/timer Z interrupt request bit (bit 0) of the interrupt request register 1 (address 003C$_{16}$) is set to "1".

• Explanation of operation

During timer stop, usually write data to a latch and a timer at the same time to set the timer value.
The timer count operation is started by setting "0" to the timer Z count stop bit (bit 6) of the timer Z mode register (address 002A$_{16}$).
When the timer reaches "0000$_{16}$", an underflow occurs at the next count pulse and the contents of timer latch are reloaded into the timer and the count is continued.
When writing data to the timer during operation, the data is written only into the latch. Then the new latch value is reloaded into the timer at the next underflow.

(2) Event counter mode

• Mode selection

This mode can be selected by setting "000" to the timer Z operating mode bits (bits 2 to 0) and setting "1" to the timer/event counter mode switch bit (bit 7) of the timer Z mode register (address 002A$_{16}$).
The valid edge for the count operation depends on the CNTR$_2$ active edge switch bit (bit 5) of the timer Z mode register (address 002A$_{16}$). When it is "0", the rising edge is valid. When it is "1", the falling edge is valid.

• Interrupt

The interrupt at an underflow is the same as the timer mode's.

• Explanation of operation

The operation is the same as the timer mode's.
Set the double-function port of CNTR$_2$ pin and port P4$_7$ to input in this mode.
Figure 30 shows the timing chart of the timer/event counter mode.

(3) Pulse output mode

• Mode selection

This mode can be selected by setting "001" to the timer Z operating mode bits (bits 2 to 0) and setting "0" to the timer/event counter mode switch bit (b7) of the timer Z mode register (address 002A$_{16}$).

• Count source selection

In high- or middle-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(X$_{IN}$); or f(X$_{CIN}$) can be selected as the count source.
In low-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(X$_{CIN}$); or f(X$_{CIN}$) can be selected as the count source.

• Interrupt

The interrupt at an underflow is the same as the timer mode's.

• Explanation of operation

The operation is the same as the timer mode's. Moreover the pulse which is inverted each time the timer underflows is output from CNTR$_2$ pin. When the CNTR$_2$ active edge switch bit (bit 5) of the timer Z mode register (address 002A$_{16}$) is "0", the output starts with "H" level. When it is "1", the output starts with "L" level.

• Precautions

The double-function port of CNTR$_2$ pin and port P4$_7$ is automatically set to the timer pulse output port in this mode.
The output from CNTR$_2$ pin is initialized to the level depending on CNTR$_2$ active edge switch bit by writing to the timer.
When the value of the CNTR$_2$ active edge switch bit is changed, the output level of CNTR$_2$ pin is inverted.
Figure 31 shows the timing chart of the pulse output mode.

(4) Pulse period measurement mode

• Mode selection

This mode can be selected by setting "010" to the timer Z operating mode bits (bits 2 to 0) and setting "0" to the timer/event counter mode switch bit (b7) of the timer Z mode register (address 002A16).

• Count source selection

In high- or middle-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(XIN); or f(XCIN) can be selected as the count source.
In low-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(XCIN); or f(XCIN) can be selected as the count source.

• Interrupt

The interrupt at an underflow is the same as the timer mode's. When the pulse period measurement is completed, the INT4/CNTR2 interrupt request bit (bit 5) of the interrupt request register 2 (address 003D16) is set to "1".

• Explanation of operation

The cycle of the pulse which is input from the CNTR2 pin is measured. When the CNTR2 active edge switch bit (bit 5) of the timer Z mode register (address 002A16) is "0", the timer counts during the term from one falling edge of CNTR2 pin input to the next falling edge. When it is "1", the timer counts during the term from one rising edge input to the next rising edge input.
When the valid edge of measurement completion/start is detected, the 1's complement of the timer value is written to the timer latch and "FFFF16" is set to the timer.
Furthermore when the timer underflows, the timer Z interrupt request occurs and "FFFF16" is set to the timer. When reading the timer Z, the value of the timer latch (measured value) is read. The measured value is retained until the next measurement completion.

• Precautions

Set the double-function port of CNTR2 pin and port P47 to input in this mode.
A read-out of timer value is impossible in this mode. The timer can be written to only during timer stop (no measurement of pulse period).
Since the timer latch in this mode is specialized for the read-out of measured values, do not perform any write operation during measurement.
"FFFF16" is set to the timer when the timer underflows or when the valid edge of measurement start/completion is detected. Consequently, the timer value at start of pulse period measurement depends on the timer value just before measurement start.
Figure 32 shows the timing chart of the pulse period measurement mode.

(5) Pulse width measurement mode

• Mode selection

This mode can be selected by setting "011" to the timer Z operating mode bits (bits 2 to 0) and setting "0" to the timer/event counter mode switch bit (b7) of the timer Z mode register (address 002A16).

• Count source selection

In high- or middle-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(XIN); or f(XCIN) can be selected as the count source.
In low-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(XCIN); or f(XCIN) can be selected as the count source.

• Interrupt

The interrupt at an underflow is the same as the timer mode's. When the pulse widths measurement is completed, the INT4/CNTR2 interrupt request bit (bit 5) of the interrupt request register 2 (address 003D16) is set to "1".

• Explanation of operation

The pulse width which is input from the CNTR2 pin is measured. When the CNTR2 active edge switch bit (bit 5) of the timer Z mode register (address 002A16) is "0", the timer counts during the term from one rising edge input to the next falling edge input ("H" term). When it is "1", the timer counts during the term from one falling edge of CNTR2 pin input to the next rising edge of input ("L" term).
When the valid edge of measurement completion is detected, the 1's complement of the timer value is written to the timer latch.
When the valid edge of measurement completion/start is detected, "FFFF16" is set to the timer.
When the timer Z underflows, the timer Z interrupt occurs and "FFFF16" is set to the timer Z. When reading the timer Z, the value of the timer latch (measured value) is read. The measured value is retained until the next measurement completion.

• Precautions

Set the double-function port of CNTR2 pin and port P47 to input in this mode.
A read-out of timer value is impossible in this mode. The timer can be written to only during timer stop (no measurement of pulse widths).
Since the timer latch in this mode is specialized for the read-out of measured values, do not perform any write operation during measurement.
"FFFF16" is set to the timer when the timer underflows or when the valid edge of measurement start/completion is detected. Consequently, the timer value at start of pulse width measurement depends on the timer value just before measurement start.
Figure 33 shows the timing chart of the pulse width measurement mode.

(6) Programmable waveform generating mode

• Mode selection

This mode can be selected by setting "100" to the timer Z operating mode bits (bits 2 to 0) and setting "0" to the timer/event counter mode switch bit (b7) of the timer Z mode register (address 002A16).

• Count source selection

In high- or middle-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(XIN); or f(XCIN) can be selected as the count source.
In low-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(XCIN); or f(XCIN) can be selected as the count source.

• Interrupt

The interrupt at an underflow is the same as the timer mode's.

• Explanation of operation

The operation is the same as the timer mode's. Moreover the timer outputs the data set in the output level latch (bit 4) of the timer Z mode register (address 002A16) from the CNTR2 pin each time the timer underflows.
Changing the value of the output level latch and the timer latch after an underflow makes it possible to output an optional waveform from the CNTR2 pin.

• Precautions

The double-function port of CNTR2 pin and port P47 is automatically set to the programmable waveform generating port in this mode.
Figure 34 shows the timing chart of the programmable waveform generating mode.

(7) Programmable one-shot generating mode

• Mode selection

This mode can be selected by setting "101" to the timer Z operating mode bits (bits 2 to 0) and setting "0" to the timer/event counter mode switch bit (b7) of the timer Z mode register (address 002A16).

• Count source selection

In high- or middle-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(XIN); or f(XCIN) can be selected as the count source.

• Interrupt

The interrupt at an underflow is the same as the timer mode's.
The trigger to generate one-shot pulse can be selected by the INT1 active edge selection bit (bit 1) of the interrupt edge selection register (address 003A16). When it is "0", the falling edge active is selected; when it is "1", the rising edge active is selected.
When the valid edge of the INT1 pin is detected, the INT1 interrupt request bit (bit 1) of the interrupt request register 1 (address 003C16) is set to "1".

• Explanation of operation

1. "H" one-shot pulse; Bit 5 of timer Z mode register = "0"
   The output level of the CNTR2 pin is initialized to "L" at mode selection. When trigger generation (input signal to INT1 pin) is detected, "H" is output from the CNTR2 pin. When an underflow occurs, "L" is output. The "H" one-shot pulse width is set by the setting value to the timer Z register low-order and high-order. When trigger generating is detected during timer count stop, although "H" is output from the CNTR2 pin, "H" output state continues because an underflow does not occur.
2. "L" one-shot pulse; Bit 5 of timer Z mode register = "1"
   The output level of the CNTR2 pin is initialized to "H" at mode selection. When trigger generation (input signal to INT1 pin) is detected, "L" is output from the CNTR2 pin. When an underflow occurs, "H" is output. The "L" one-shot pulse width is set by the setting value to the timer Z low-order and high-order. When trigger generating is detected during timer count stop, although "L" is output from the CNTR2 pin, "L" output state continues because an underflow does not occur.

• Precautions

Set the double-function port of INT1 pin and port P42 to input in this mode.
The double-function port of CNTR2 pin and port P47 is automatically set to the programmable one-shot generating port in this mode.
This mode cannot be used in low-speed mode.
If the value of the CNTR2 active edge switch bit is changed during one-shot generating enabled or generating one-shot pulse, then the output level from CNTR2 pin changes.
Figure 35 shows the timing chart of the programmable one-shot generating mode.

<Notes regarding all modes>

• Timer Z write control

Which write control can be selected by the timer Z write control bit (bit 3) of the timer Z mode register (address 002A16), writing data to both the latch and the timer at the same time or writing data only to the latch.

When the operation "writing data only to the latch" is selected, the value is set to the timer latch by writing data to the address of timer Z and the timer is updated at next underflow. After reset release, the operation "writing data to both the latch and the timer at the same time" is selected, and the value is set to both the latch and the timer at the same time by writing data to the address of timer Z.

In the case of writing data only to the latch, if writing data to the latch and an underflow are performed almost at the same time, the timer value may become undefined.

• Timer Z read control

A read-out of timer value is impossible in pulse period measurement mode and pulse width measurement mode. In the other modes, a read-out of timer value is possible regardless of count operating or stopped. However, a read-out of timer latch value is impossible.

• Switch of interrupt active edge of CNTR2 and INT1

Each interrupt active edge depends on setting of the CNTR2 active edge switch bit and the INT1 active edge selection bit.

• Switch of count source

When switching the count source by the timer Z count source selection bits, the value of timer count is altered in inconsiderable amount owing to generating of thin pulses on the count input signals.

Therefore, select the timer count source before setting the value to the prescaler and the timer.

• Usage of CNTR2 pin as normal I/O port P47

To use the CNTR2 pin as normal I/O port P47, set timer Z operating mode bits (b2, b1, b0) of timer Z mode register (address 002A16) to "000".

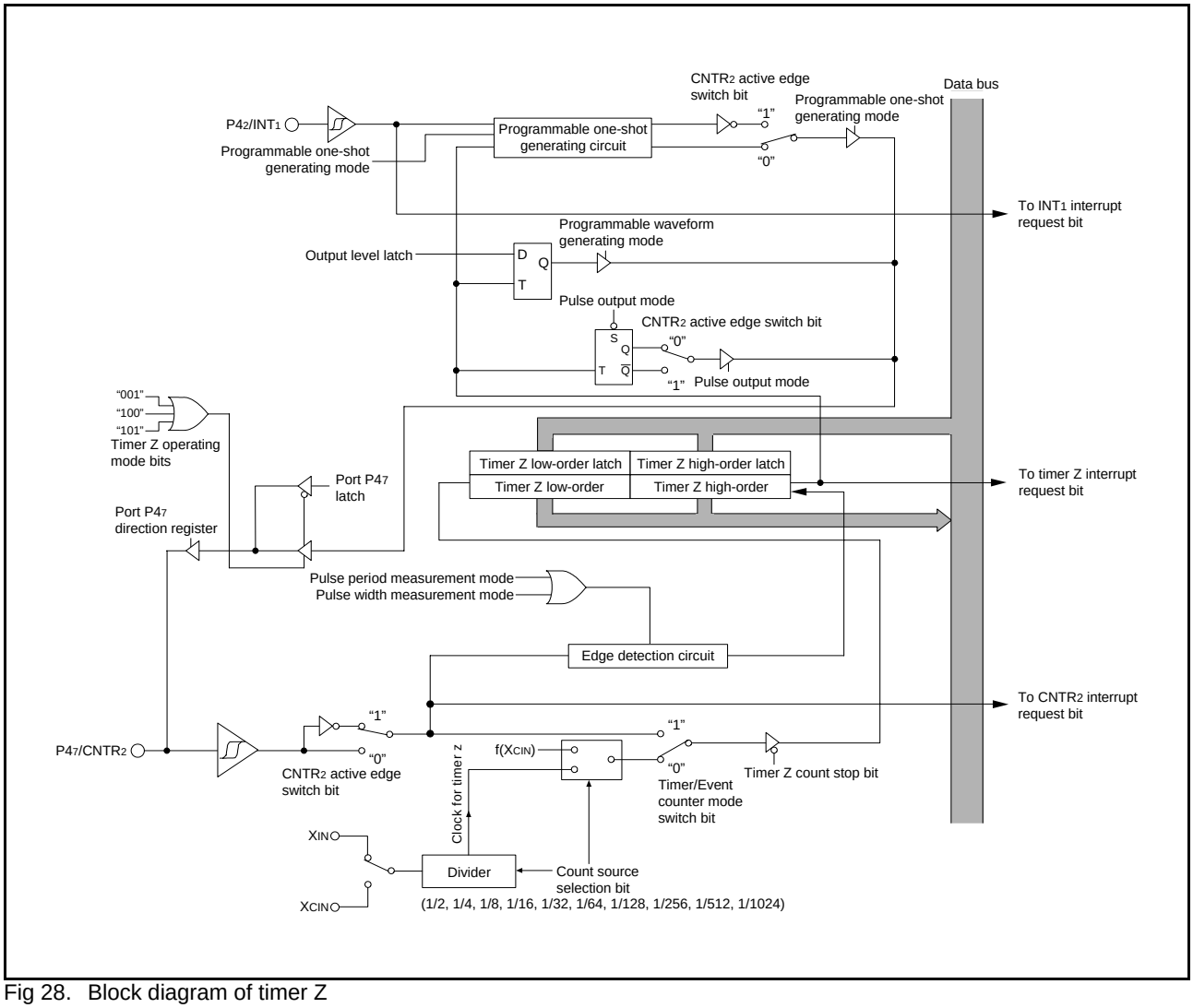
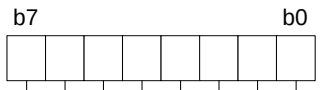


Fig 28. Block diagram of timer Z



Timer Z mode register
(TZM : address 002A16)

Timer Z operating mode bits
b2 b1 b0
0 0 0 : Timer/Event counter mode
0 0 1 : Pulse output mode
0 1 0 : Pulse period measurement mode
0 1 1 : Pulse width measurement mode
1 0 0 : Programmable waveform generating mode
1 0 1 : Programmable one-shot generating mode
1 1 0 : Not available
1 1 1 : Not available

Timer Z write control bit
0 : Writing data to both latch and timer simultaneously
1 : Writing data only to latch

Output level latch
0 : "L" output
1 : "H" output

CNTR2 active edge switch bit
0 : •Event counter mode: Count at rising edge
•Pulse output mode: Start outputting "H"
•Pulse period measurement mode: Measurement between two falling edges
•Pulse width measurement mode: Measurement of "H" term
•Programmable one-shot generating mode: After start outputting "L", "H" one-shot pulse generated
•Interrupt at falling edge
1 : •Event counter mode: Count at falling edge
•Pulse output mode: Start outputting "L"
•Pulse period measurement mode: Measurement between two rising edges
•Pulse width measurement mode: Measurement of "L" term
•Programmable one-shot generating mode: After start outputting "H", "L" one-shot pulse generated
•Interrupt at rising edge

Timer Z count stop bit
0 : Count start
1 : Count stop

Timer/Event counter mode switch bit **(Note)**
0 : Timer mode
1 : Event counter mode

Note: When selecting the modes except the timer/event counter mode, set "0" to this bit.

Fig 29. Structure of timer Z mode register

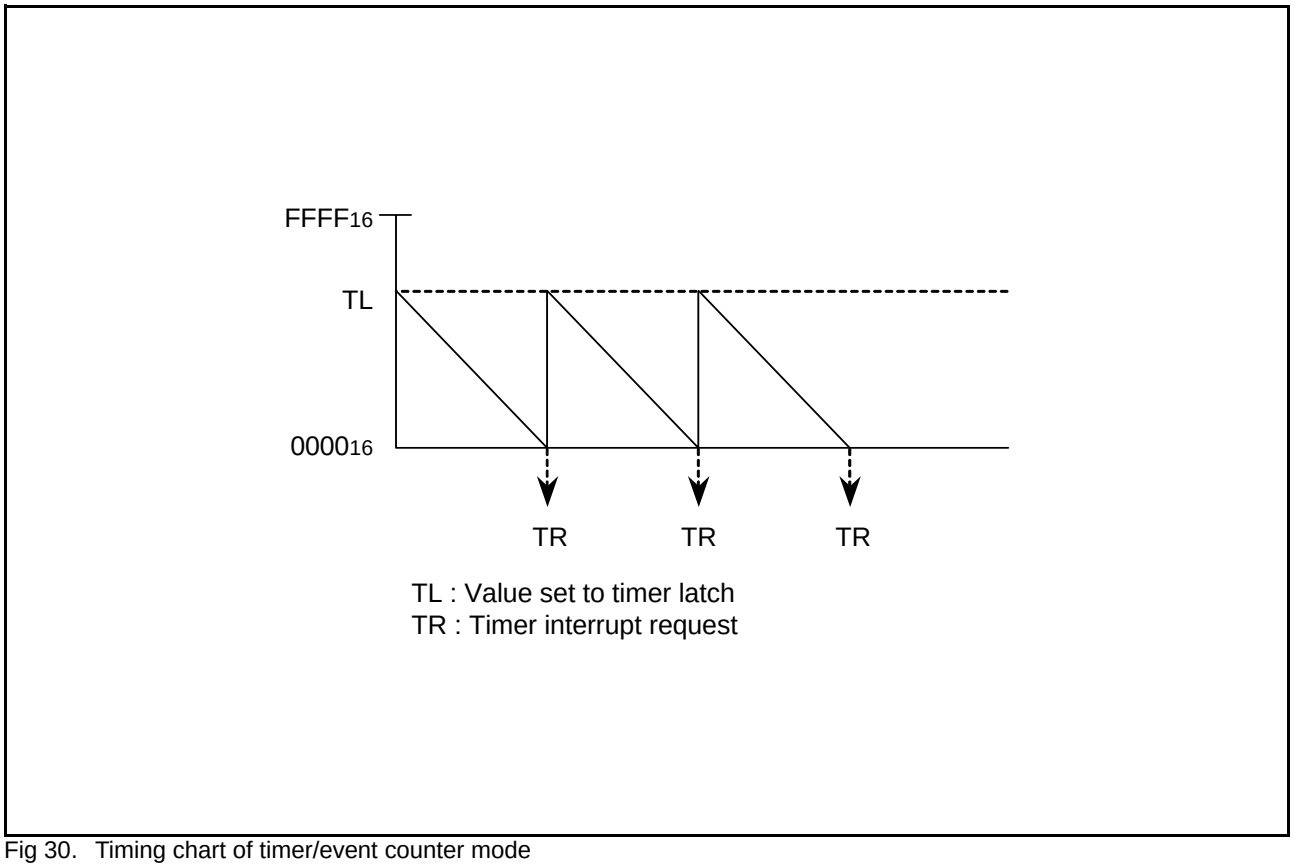


Fig 30. Timing chart of timer/event counter mode

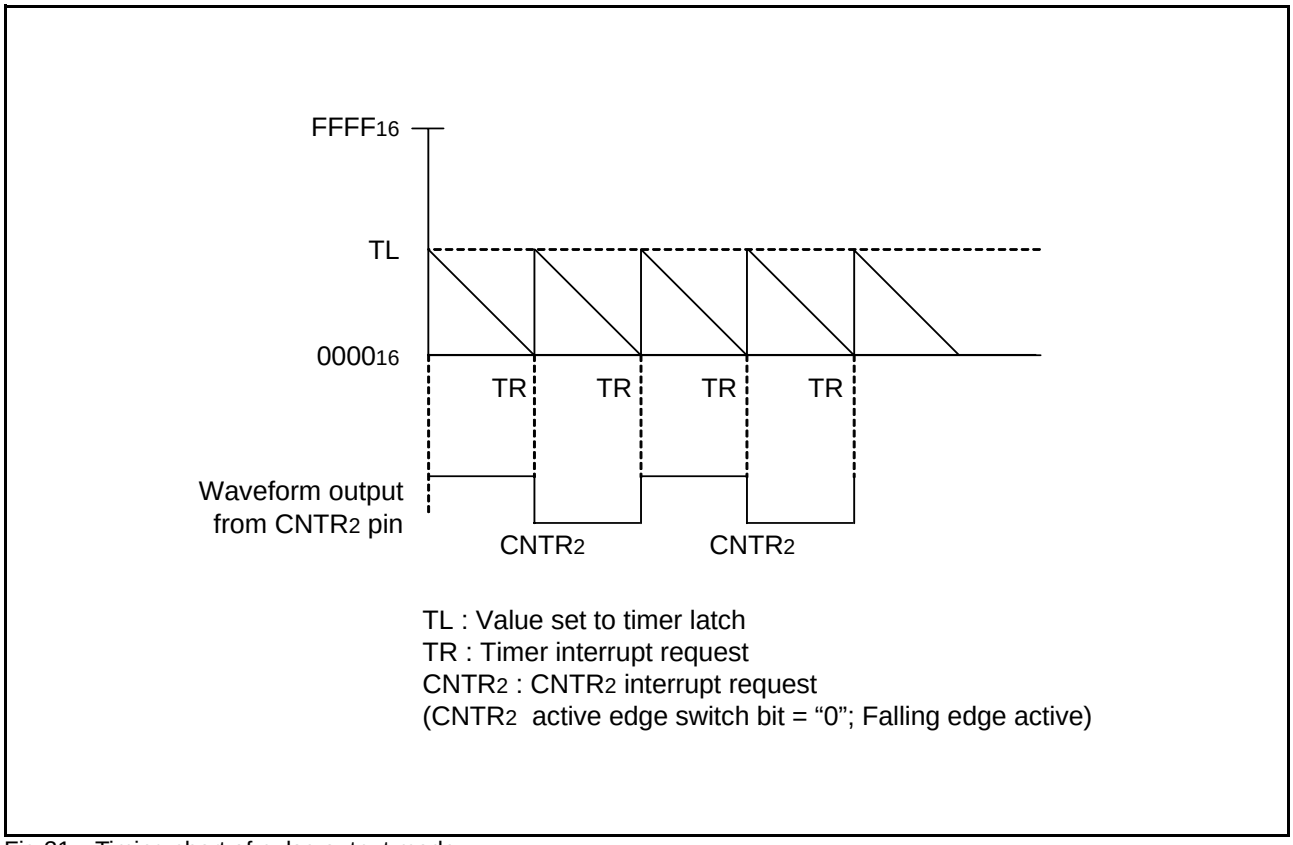


Fig 31. Timing chart of pulse output mode

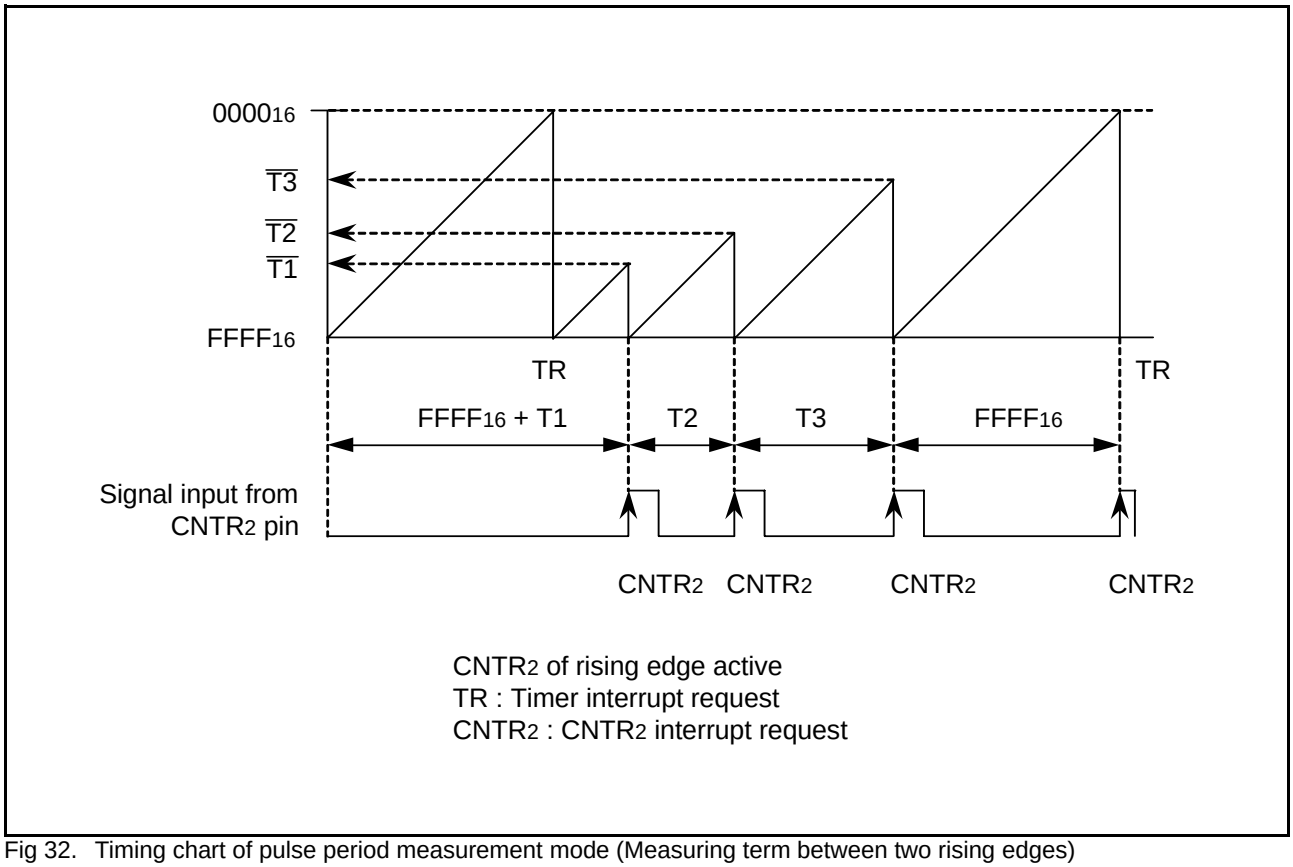


Fig 32. Timing chart of pulse period measurement mode (Measuring term between two rising edges)

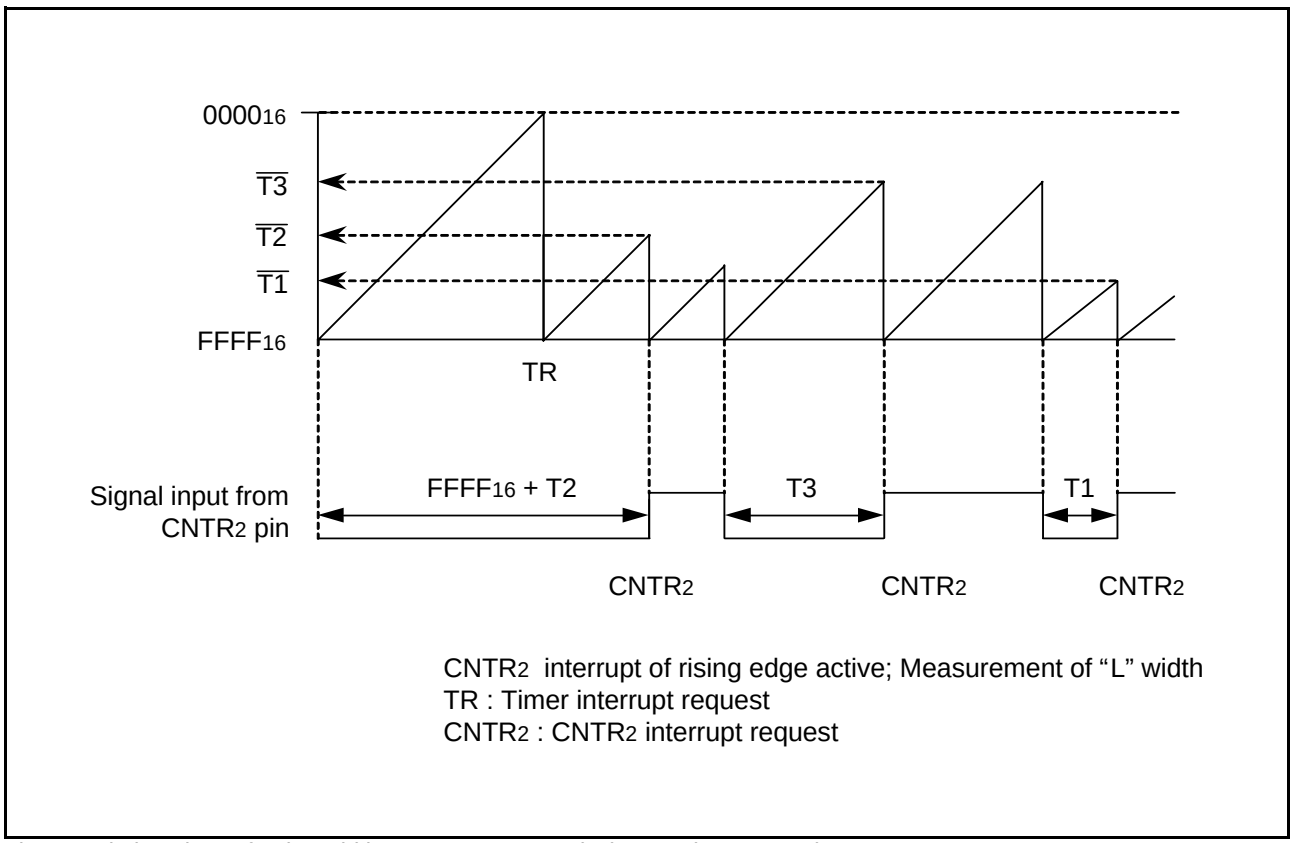


Fig 33. Timing chart of pulse width measurement mode (Measuring “L” term)

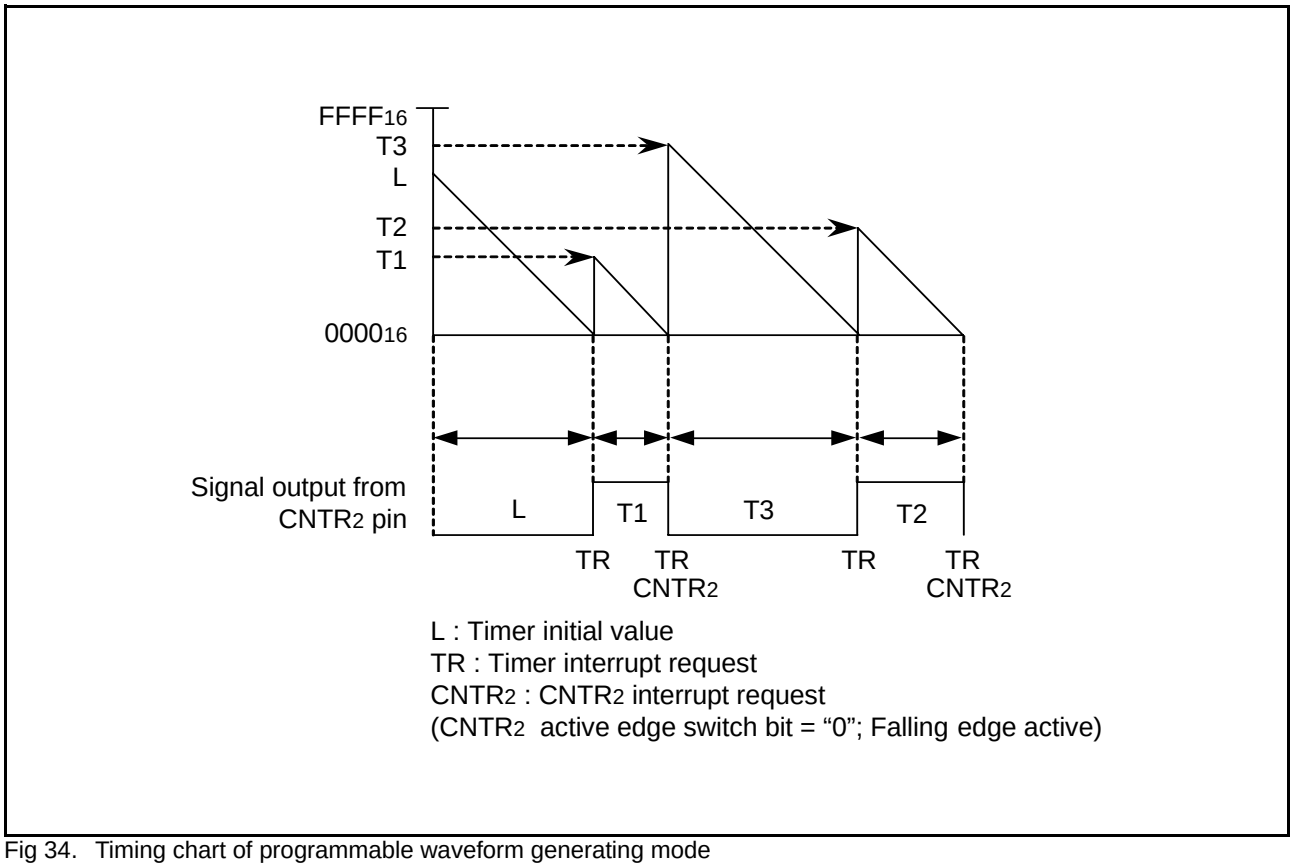


Fig 34. Timing chart of programmable waveform generating mode

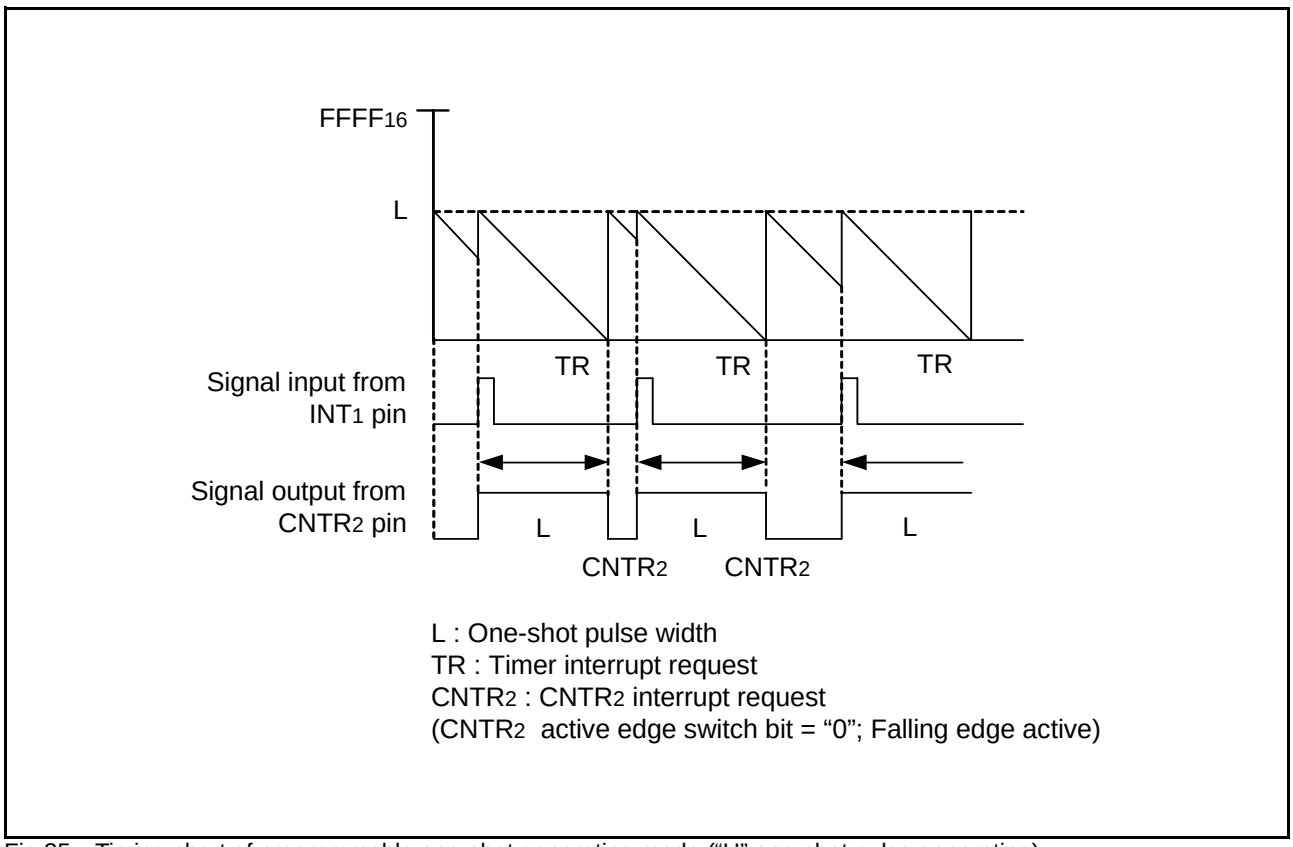


Fig 35. Timing chart of programmable one-shot generating mode (“H” one-shot pulse generating)

SERIAL INTERFACE

Serial I/O1

Serial I/O1 can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O1 mode can be selected by setting the serial I/O1 mode selection bit of the serial I/O1 control register (bit 6 of address 001A16) to "1".
For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the transmit/receive buffer register.

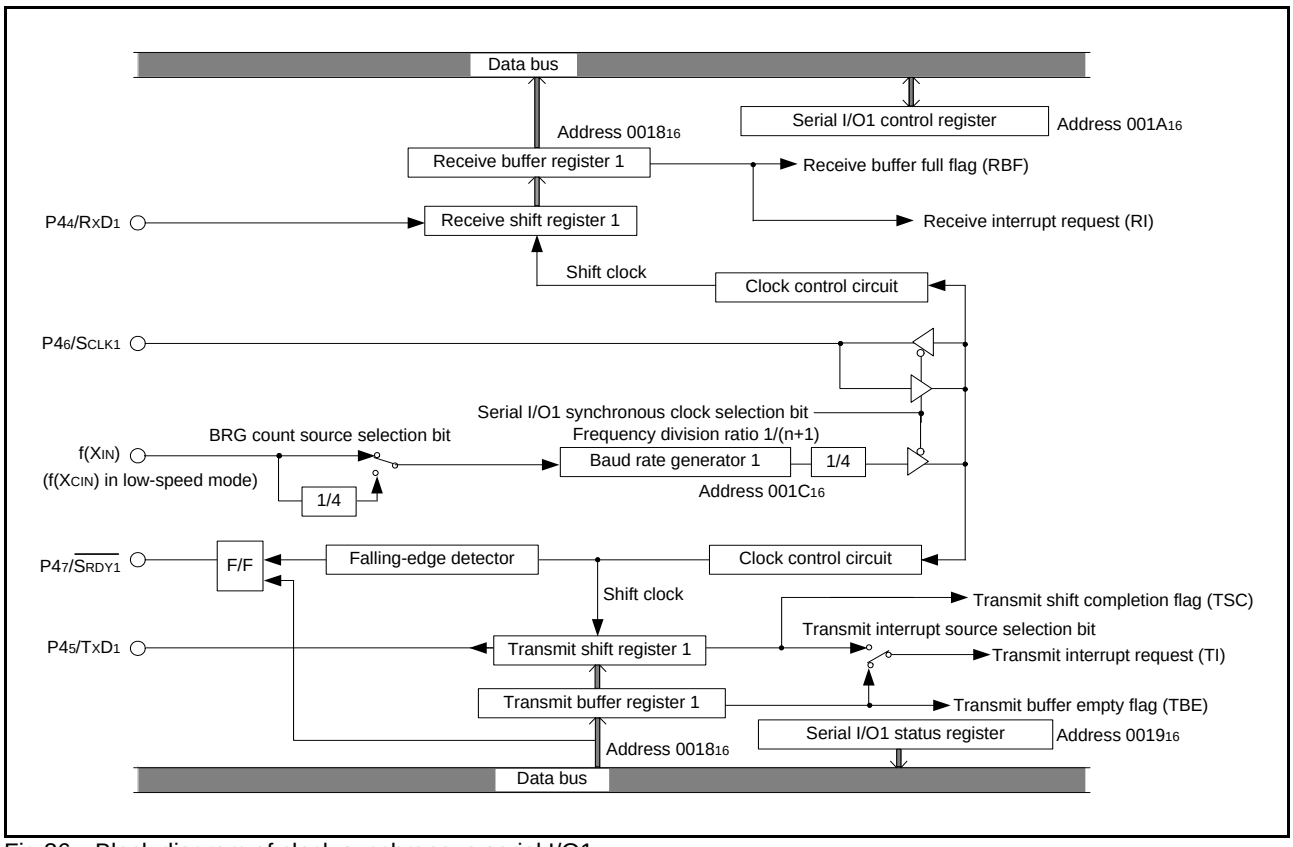
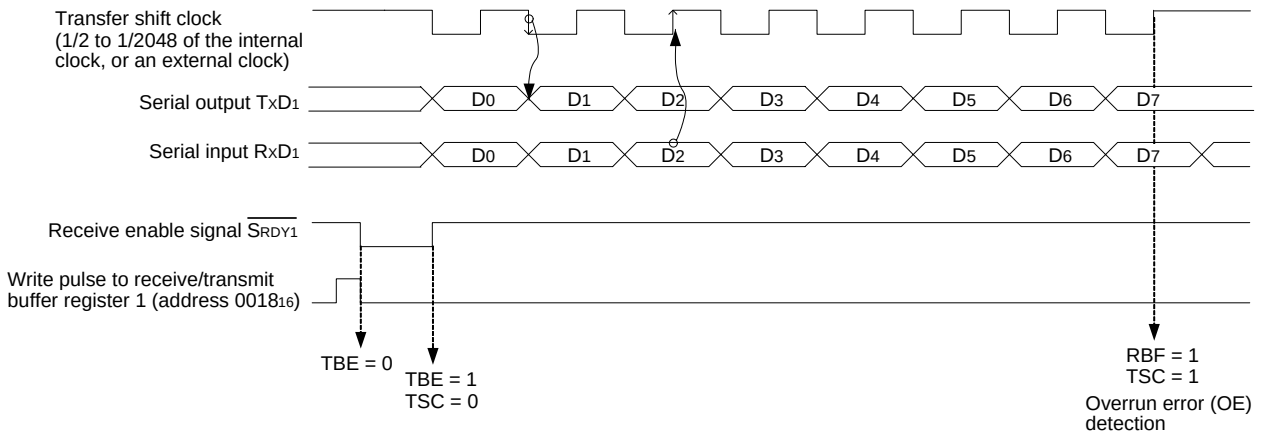


Fig 36. Block diagram of clock synchronous serial I/O1



Notes 1: As the transmit interrupt (TI), which can be selected, either when the transmit buffer has emptied (TBE=1) or after the transmit shift operation has ended (TSC=1), by setting the transmit interrupt source selection bit (TIC) of the serial I/O1 control register.
2: If data is written to the transmit buffer register 1 when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the TxD1 pin.
3: The receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes "1".

Fig 37. Operation of clock synchronous serial I/O1

(2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O1 mode selection bit (b6) of the serial I/O1 control register to "0".
Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have the buffer register 1, but the two buffer registers have the same address in a memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register 1, and receive data is read from the receive buffer register 1.
The transmit buffer register 1 can also hold the next data to be transmitted, and the receive buffer register 1 can hold a character while the next character is being received.

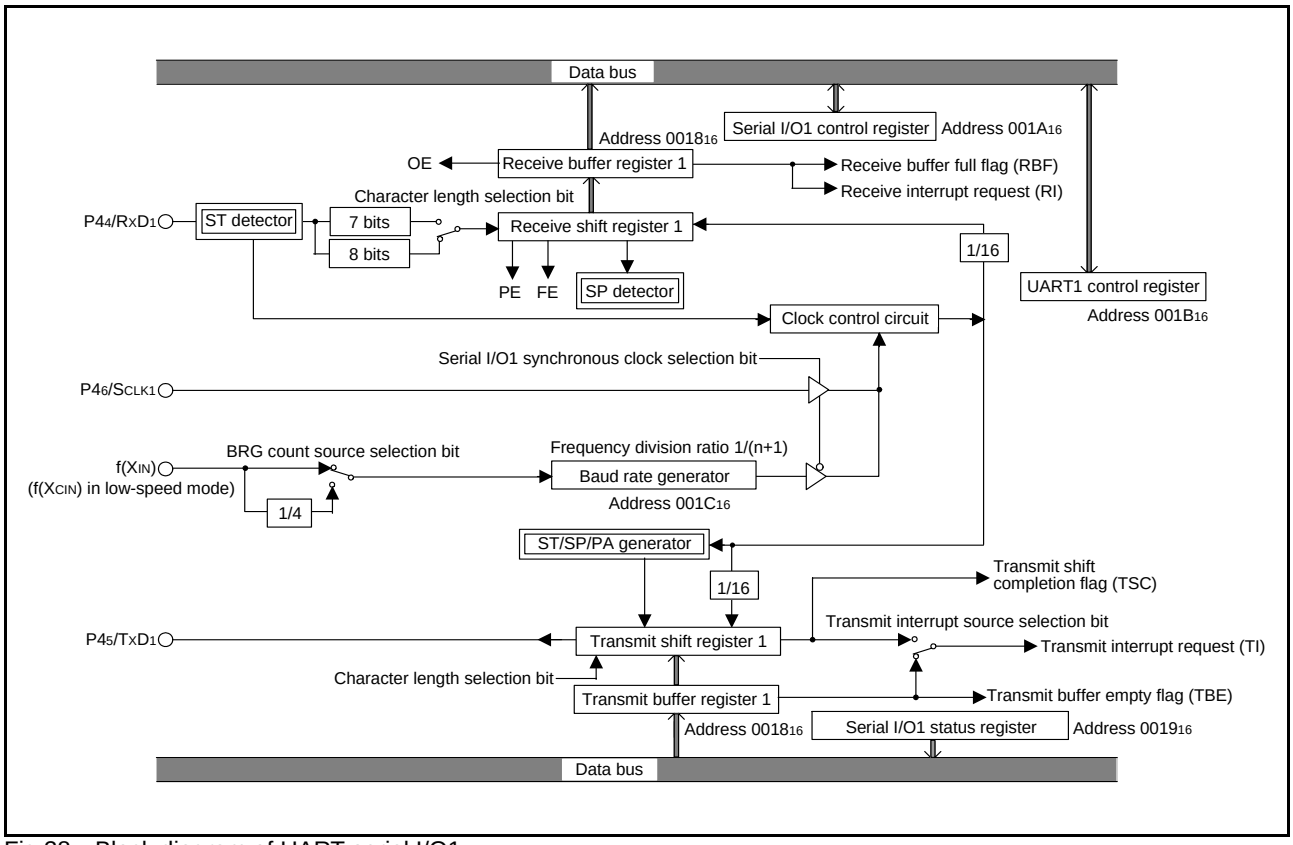
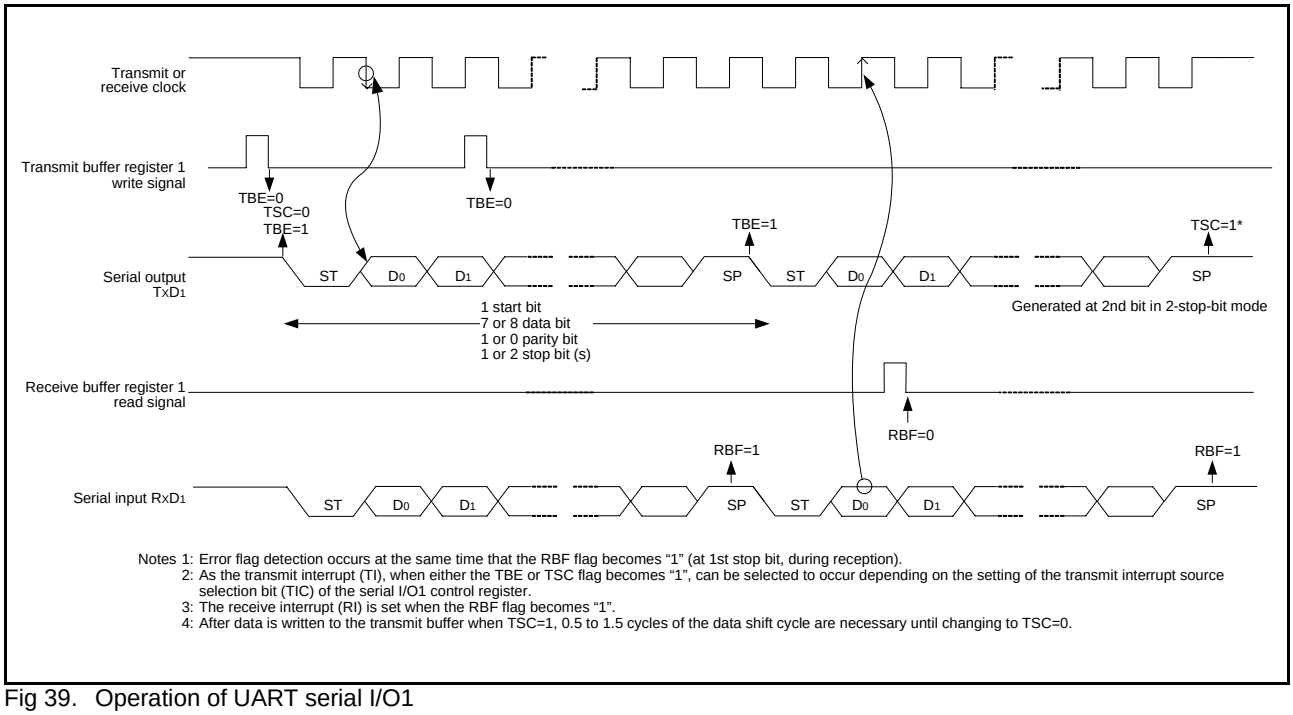


Fig 38. Block diagram of UART serial I/O1



Notes 1: Error flag detection occurs at the same time that the RBF flag becomes "1" (at 1st stop bit, during reception).
2: As the transmit interrupt (TI), when either the TBE or TSC flag becomes "1", can be selected to occur depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O1 control register.
3: The receive interrupt (RI) is set when the RBF flag becomes "1".
4: After data is written to the transmit buffer when TSC=1, 0.5 to 1.5 cycles of the data shift cycle are necessary until changing to TSC=0.

Fig 39. Operation of UART serial I/O1

[Transmit Buffer Register 1/Receive Buffer Register 1 (TB1/RB1)] 0018$_{16}$

The transmit buffer register 1 and the receive buffer register 1 are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

[Serial I/O1 Status Register (SIO1STS)] 0019$_{16}$

The read-only serial I/O1 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O1 function and various errors.
Three of the flags (bits 4 to 6) are valid only in UART mode.
The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer register 1 is read.
If there is an error, it is detected at the same time that data is transferred from the receive shift register 1 to the receive buffer register 1, and the receive buffer full flag is set. A write to the serial I/O1 status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "0" to the serial I/O1 enable bit SIOE (bit 7 of the serial I/O1 control register) also clears all the status flags, including the error flags.
Bits 0 to 6 of the serial I/O1 status register are initialized to "0" at reset, but if the transmit enable bit (bit 4) of the serial I/O1 control register has been set to "1", the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

[Serial I/O1 Control Register (SIO1CON)] 001A$_{16}$

The serial I/O1 control register consists of eight control bits for the serial I/O1 function.

[UART1 Control Register (UART1CON)] 001B$_{16}$

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer, and one bit (bit 4) which is always valid and sets the output structure of the $P4_5/TxD_1$ pin.

[Baud Rate Generator 1 (BRG1)] 001C$_{16}$

The baud rate generator determines the baud rate for serial transfer.
The baud rate generator divides the frequency of the count source by 1/(n + 1), where n is the value written to the baud rate generator.

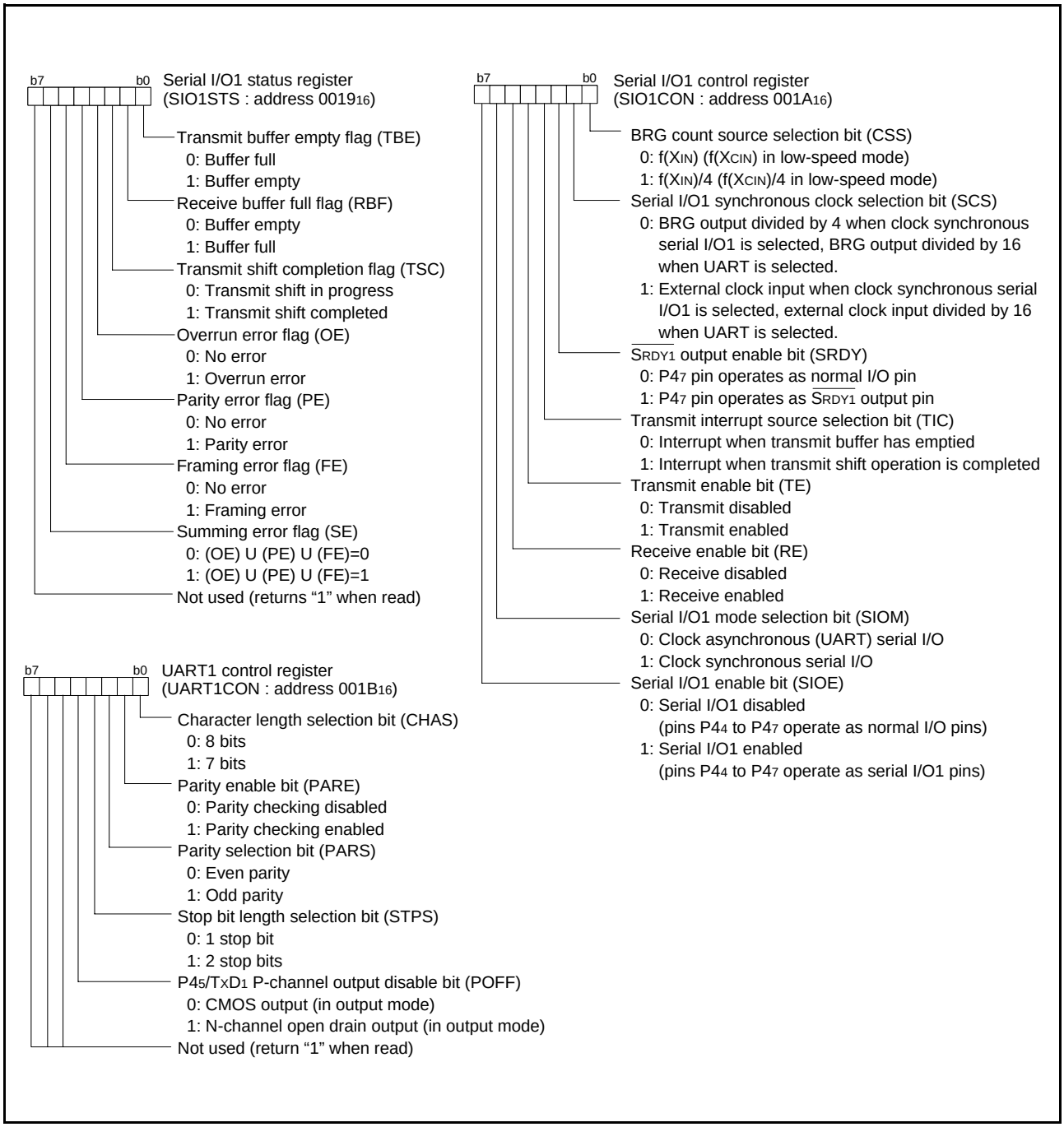


Fig 40. Structure of serial I/O1 control registers

<Notes concerning serial I/O1>

1. Notes when selecting clock synchronous serial I/O

1.1 Stop of transmission operation

• Note

Clear the serial I/O1 enable bit and the transmit enable bit to "0" (serial I/O and transmit disabled).

• Reason

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O1 enable bit is cleared to "0" (serial I/O disabled), the internal transmission is running (in this case, since pins TxD1, RxD1, SCLK1, and SRDY1 function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register 1 in this state, data starts to be shifted to the transmit shift register 1. When the serial I/O1 enable bit is set to "1" at this time, the data during internally shifting is output to the TxD1 pin and an operation failure occurs.

1.2 Stop of receive operation

• Note

Clear the receive enable bit to "0" (receive disabled), or clear the serial I/O1 enable bit to "0" (serial I/O disabled).

1.3 Stop of transmit/receive operation

• Note

Clear both the transmit enable bit and receive enable bit to "0" (transmit and receive disabled).

(when data is transmitted and received in the clock synchronous serial I/O mode, any one of data transmission and reception cannot be stopped.)

• Reason

In the clock synchronous serial I/O mode, the same clock is used for transmission and reception. If any one of transmission and reception is disabled, a bit error occurs because transmission and reception cannot be synchronized.

In this mode, the clock circuit of the transmission circuit also operates for data reception. Accordingly, the transmission circuit does not stop by clearing only the transmit enable bit to "0" (transmit disabled). Also, the transmission circuit is not initialized by clearing the serial I/O1 enable bit to "0" (serial I/O disabled) (refer to 1.1).

2. Notes when selecting clock asynchronous serial I/O

2.1 Stop of transmission operation

• Note

Clear the transmit enable bit to "0" (transmit disabled). The transmission operation does not stop by clearing the serial I/O1 enable bit to "0".

• Reason

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O1 enable bit is cleared to "0" (serial I/O disabled), the internal transmission is running (in this case, since pins TxD1, RxD1, SCLK1, and SRDY1 function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register 1 in this state, data starts to be shifted to the transmit shift register 1. When the serial I/O1 enable bit is set to "1" at this time, the data during internally shifting is output to the TxD1 pin and an operation failure occurs.

2.2 Stop of receive operation

• Note

Clear the receive enable bit to "0" (receive disabled).

2.3 Stop of transmit/receive operation

• Note 1 (only transmission operation is stopped)

Clear the transmit enable bit to "0" (transmit disabled). The transmission operation does not stop by clearing the serial I/O1 enable bit to "0".

• Reason

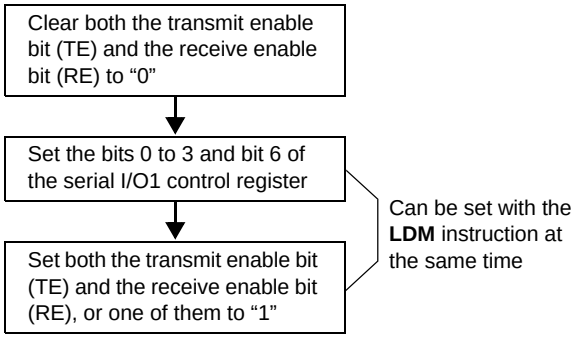
Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O1 enable bit is cleared to "0" (serial I/O disabled), the internal transmission is running (in this case, since pins TxD1, RxD1, SCLK1, and SRDY1 function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register 1 in this state, data starts to be shifted to the transmit shift register 1. When the serial I/O1 enable bit is set to "1" at this time, the data during internally shifting is output to the TxD1 pin and an operation failure occurs.

• Note 2 (only receive operation is stopped)

Clear the receive enable bit to "0" (receive disabled).

3. $\overline{\text{SRDY1}}$ output of reception side
- Note
  When signals are output from the $\overline{\text{SRDY1}}$ pin on the reception side by using an external clock in the clock synchronous serial I/O mode, set all of the receive enable bit, the $\overline{\text{SRDY1}}$ output enable bit, and the transmit enable bit to "1" (transmit enabled).

4. Setting serial I/O1 control register again
- Note
  Set the serial I/O1 control register again after the transmission and the reception circuits are reset by clearing both the transmit enable bit and the receive enable bit to "0".



5.Data transmission control with referring to transmit shift register completion flag
- Note
  After the transmit data is written to the transmit buffer register, the transmit shift register completion flag changes from "1" to "0" with a delay of 0.5 to 1.5 shift clocks. When data transmission is controlled with referring to the flag after writing the data to the transmit buffer register, note the delay.

6. Transmission control when external clock is selected
- Note
  When an external clock is used as the synchronous clock for data transmission, set the transmit enable bit to "1" at "H" of the SCLK1 input level. Also, write data to the transmit buffer register 1 at "H" of the SCLK1 input level.

7. Transmit interrupt request when transmit enable bit is set
- Note
  When using the transmit interrupt, take the following sequence.
  1. Set the serial I/O1 transmit interrupt enable bit to "0" (disabled).
  2. Set the transmit enable bit to "1".
  3. Set the serial I/O1 transmit interrupt request bit to "0" after 1 or more instruction has executed.
  4. Set the serial I/O1 transmit interrupt enable bit to "1" (enabled).

- Reason
  When the transmit enable bit is set to "1", the transmit buffer empty flag and the transmit shift register shift completion flag are also set to "1". Therefore, regardless of selecting which timing for the generating of transmit interrupts, the interrupt request is generated and the serial I/O1 transmit interrupt request bit is set at this point.

Serial I/O2

The serial I/O2 function can be used only for clock synchronous serial I/O.

For clock synchronous serial I/O2, the transmitter and the receiver must use the same clock. If the internal clock is used, transfer is started by a write signal to the serial I/O2 register (address 001F16).

[Serial I/O2 Control Register (SIO2CON)] 001D16

The serial I/O2 control register contains eight bits which control various serial I/O2 functions.

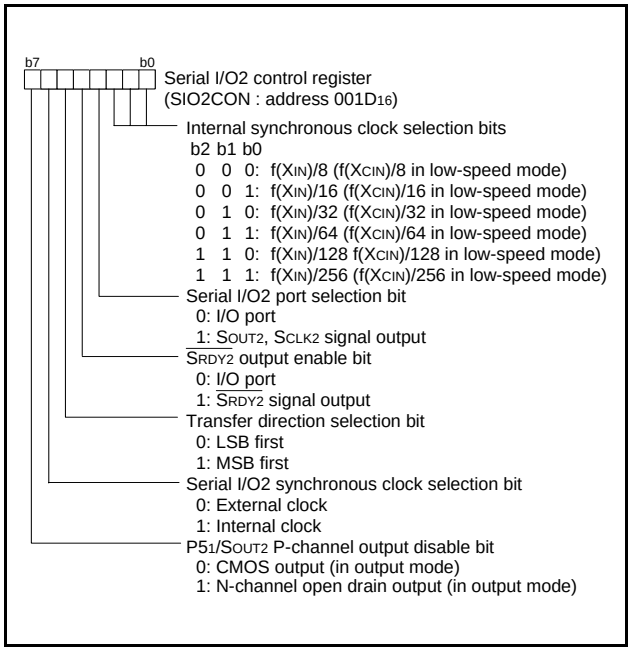


Fig 41. Structure of Serial I/O2 control register

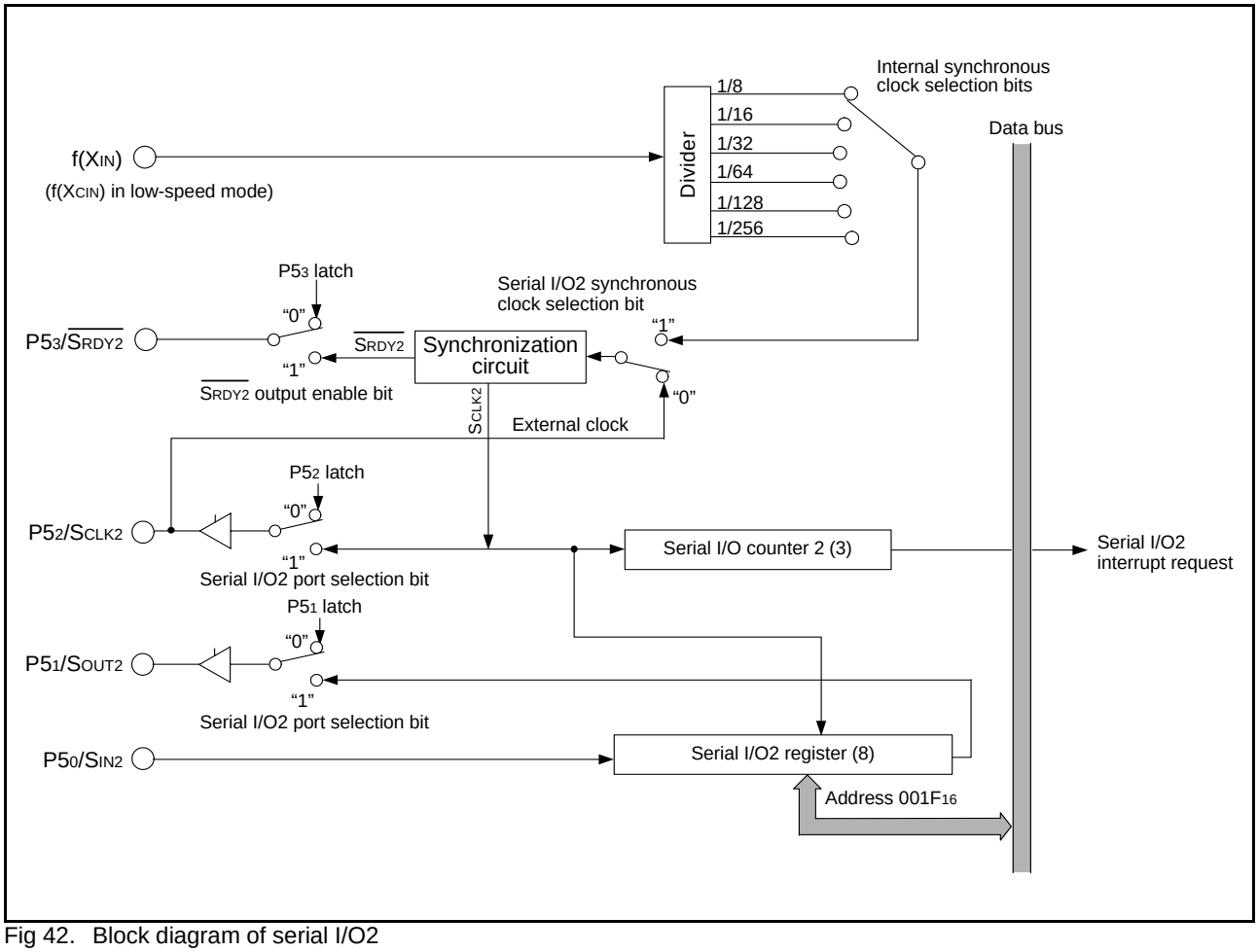
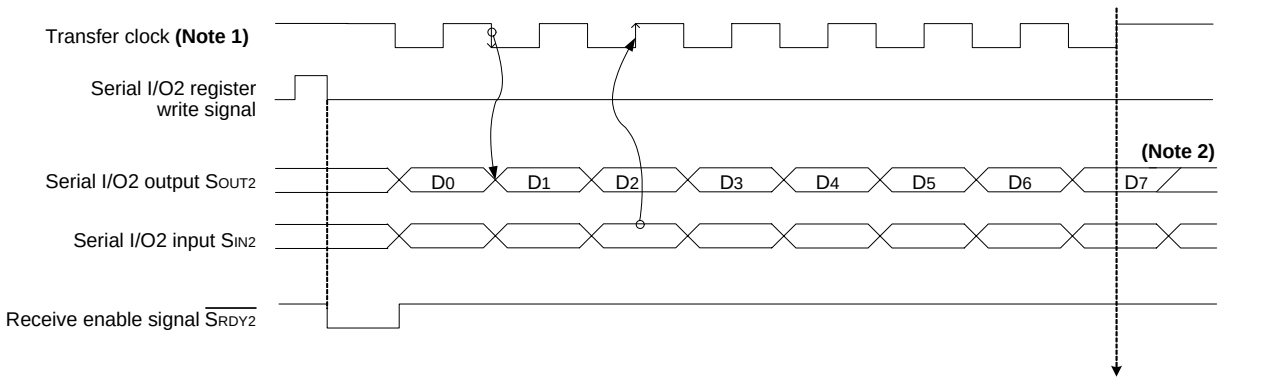


Fig 42. Block diagram of serial I/O2



Notes1: When the internal clock is selected as the transfer clock, the divide ratio of f(X_{IN}), or (f(X_{CIN}) in low-speed mode, can be selected by setting bits 0 to 2 of the serial I/O2 control register.
2: When the internal clock is selected as the transfer clock, the S_{OUT2} pin goes to high impedance after transfer completion.

Fig 43. Timing of serial I/O2

Serial I/O3

Serial I/O3 can be used as either clock synchronous or asynchronous (UART) serial I/O3. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O3 mode can be selected by setting the serial I/O3 mode selection bit of the serial I/O3 control register (bit 6 of address 0032_{16}) to "1".
For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the transmit/receive buffer register 3.

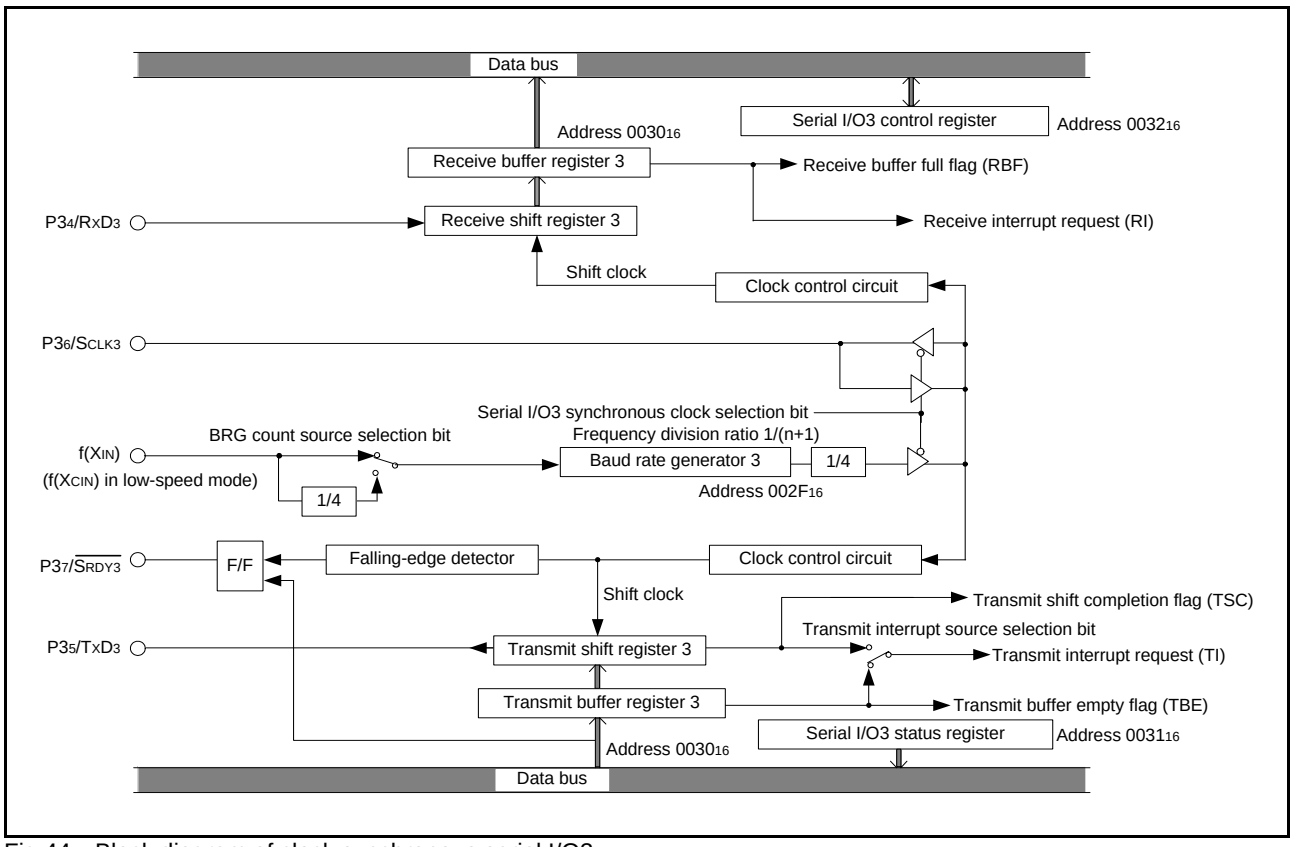
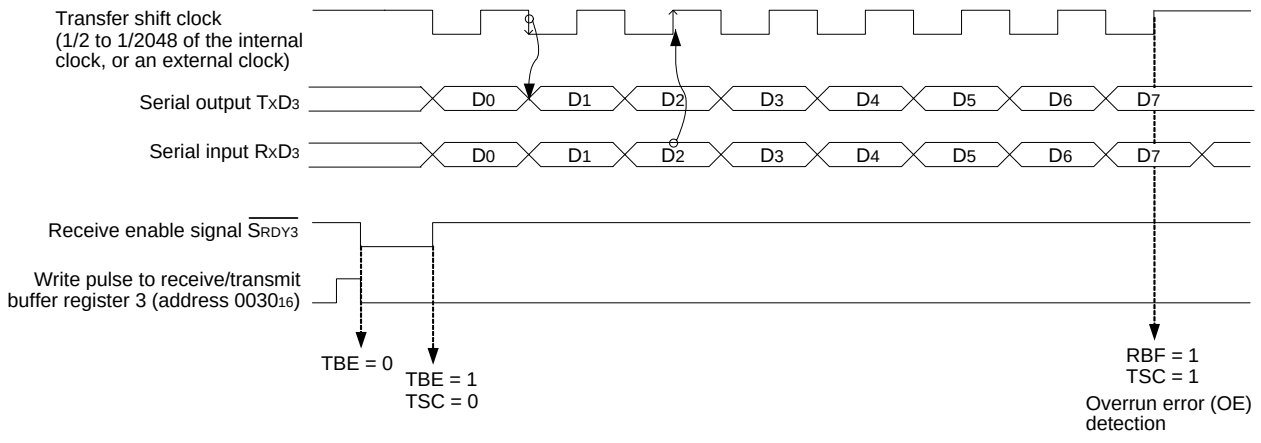


Fig 44. Block diagram of clock synchronous serial I/O3



Notes 1: As the transmit interrupt (TI), which can be selected, either when the transmit buffer has emptied (TBE=1) or after the transmit shift operation has ended (TSC=1), by setting the transmit interrupt source selection bit (TIC) of the serial I/O3 control register.
2: If data is written to the transmit buffer register 3 when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the TxD₃ pin.
3: The receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes "1".

Fig 45. Operation of clock synchronous serial I/O3

(2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O3 mode selection bit (b6) of the serial I/O3 control register to "0".
Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have the buffer register 3, but the two buffers have the same address in a memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register 3, and receive data is read from the receive buffer register 3.
The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register 3 can hold a character while the next character is being received.

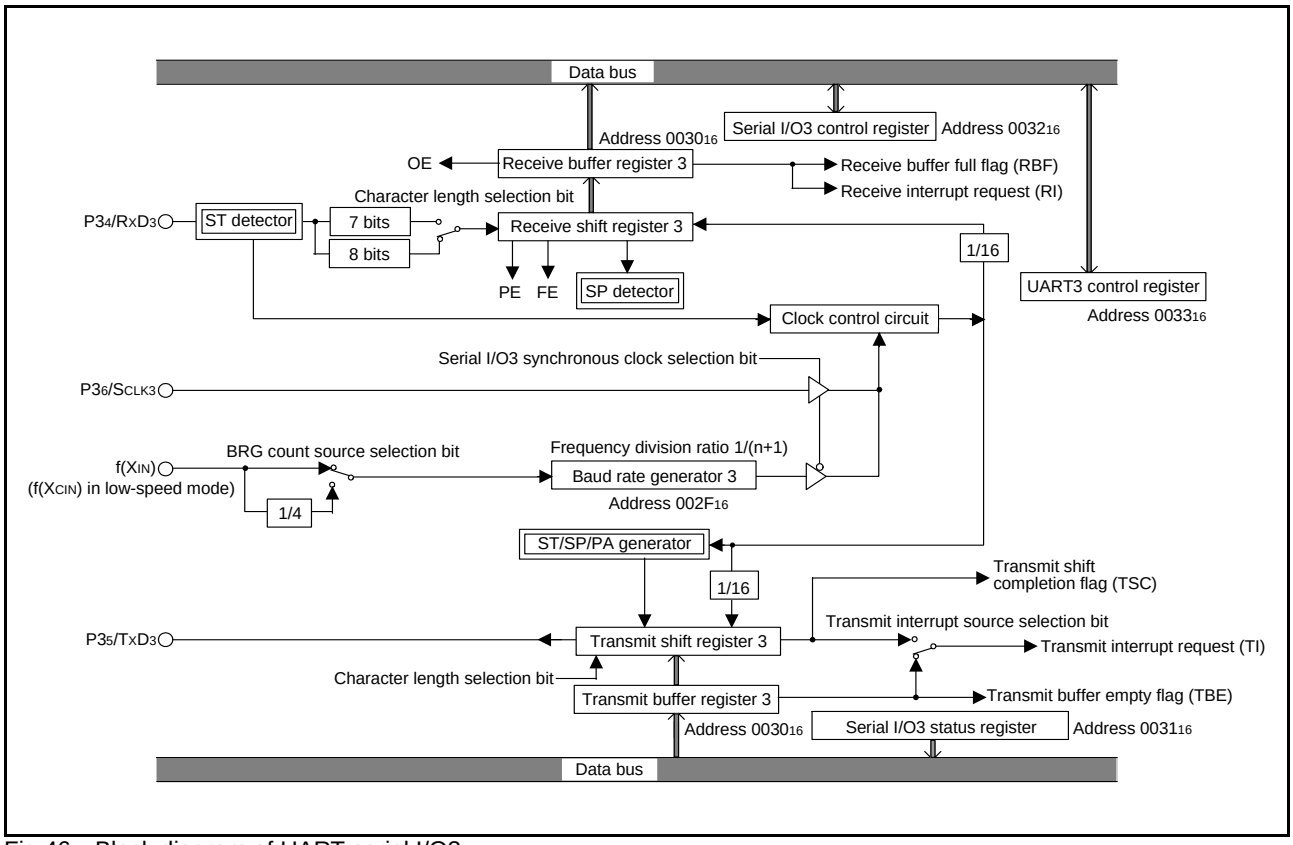
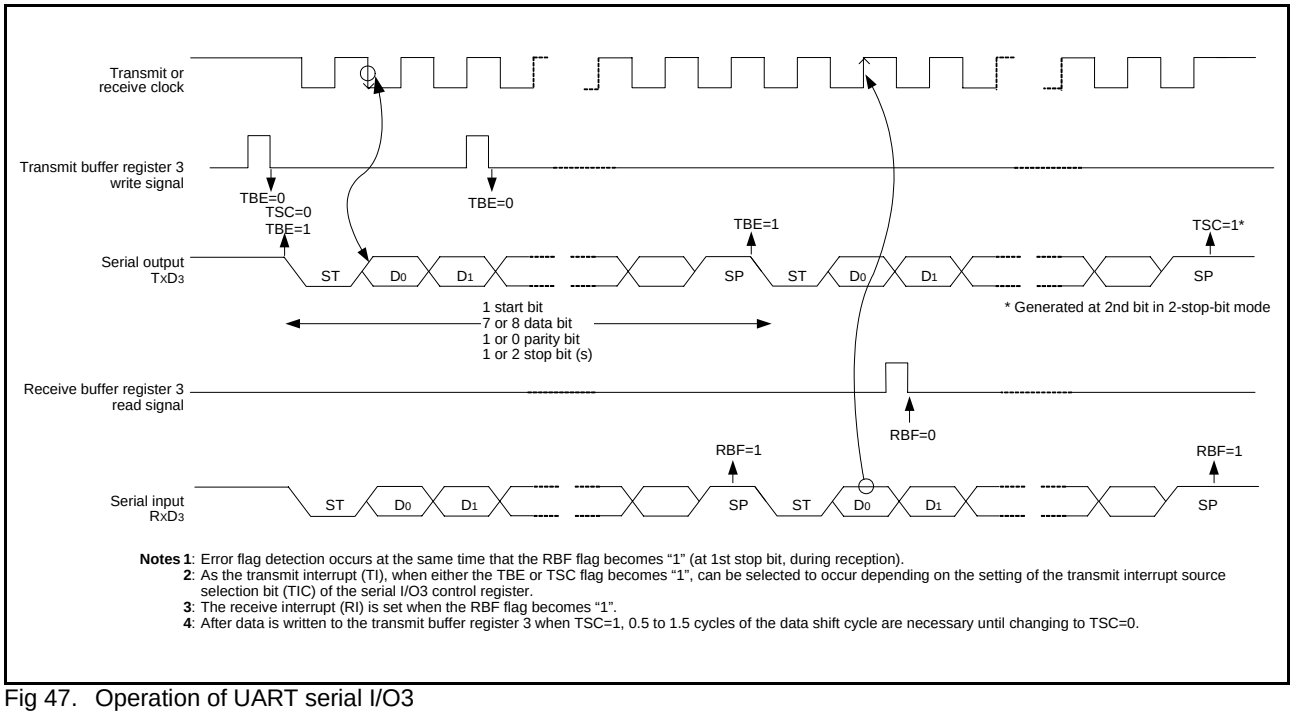


Fig 46. Block diagram of UART serial I/O3



Notes 1: Error flag detection occurs at the same time that the RBF flag becomes "1" (at 1st stop bit, during reception).
2: As the transmit interrupt (TI), when either the TBE or TSC flag becomes "1", can be selected to occur depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O3 control register.
3: The receive interrupt (RI) is set when the RBF flag becomes "1".
4: After data is written to the transmit buffer register 3 when TSC=1, 0.5 to 1.5 cycles of the data shift cycle are necessary until changing to TSC=0.

Fig 47. Operation of UART serial I/O3

[Transmit Buffer Register 3/Receive Buffer Register 3 (TB3/RB3)] 0030$_{16}$

The transmit buffer register 3 and the receive buffer register 3 are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

[Serial I/O3 Status Register (SIO3STS)] 0031$_{16}$

The read-only serial I/O3 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O3 function and various errors.
Three of the flags (bits 4 to 6) are valid only in UART mode.
The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer register 3 is read.
If there is an error, it is detected at the same time that data is transferred from the receive shift register 3 to the receive buffer register 3, and the receive buffer full flag is set. A write to the serial I/O3 status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "0" to the serial I/O3 enable bit SIOE (bit 7 of the serial I/O3 control register) also clears all the status flags, including the error flags.
Bits 0 to 6 of the serial I/O3 status register are initialized to "0" at reset, but if the transmit enable bit (bit 4) of the serial I/O3 control register has been set to "1", the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

[Serial I/O3 Control Register (SIO3CON)] 0032$_{16}$

The serial I/O3 control register consists of eight control bits for the serial I/O3 function.

[UART3 Control Register (UART3CON)] 0033$_{16}$

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer, and one bit (bit 4) which is always valid and sets the output structure of the P3$_5$/TxD$_3$ pin.

[Baud Rate Generator 3 (BRG3)] 002F$_{16}$

The baud rate generator determines the baud rate for serial transfer.
The baud rate generator divides the frequency of the count source by 1/(n + 1), where n is the value written to the baud rate generator.

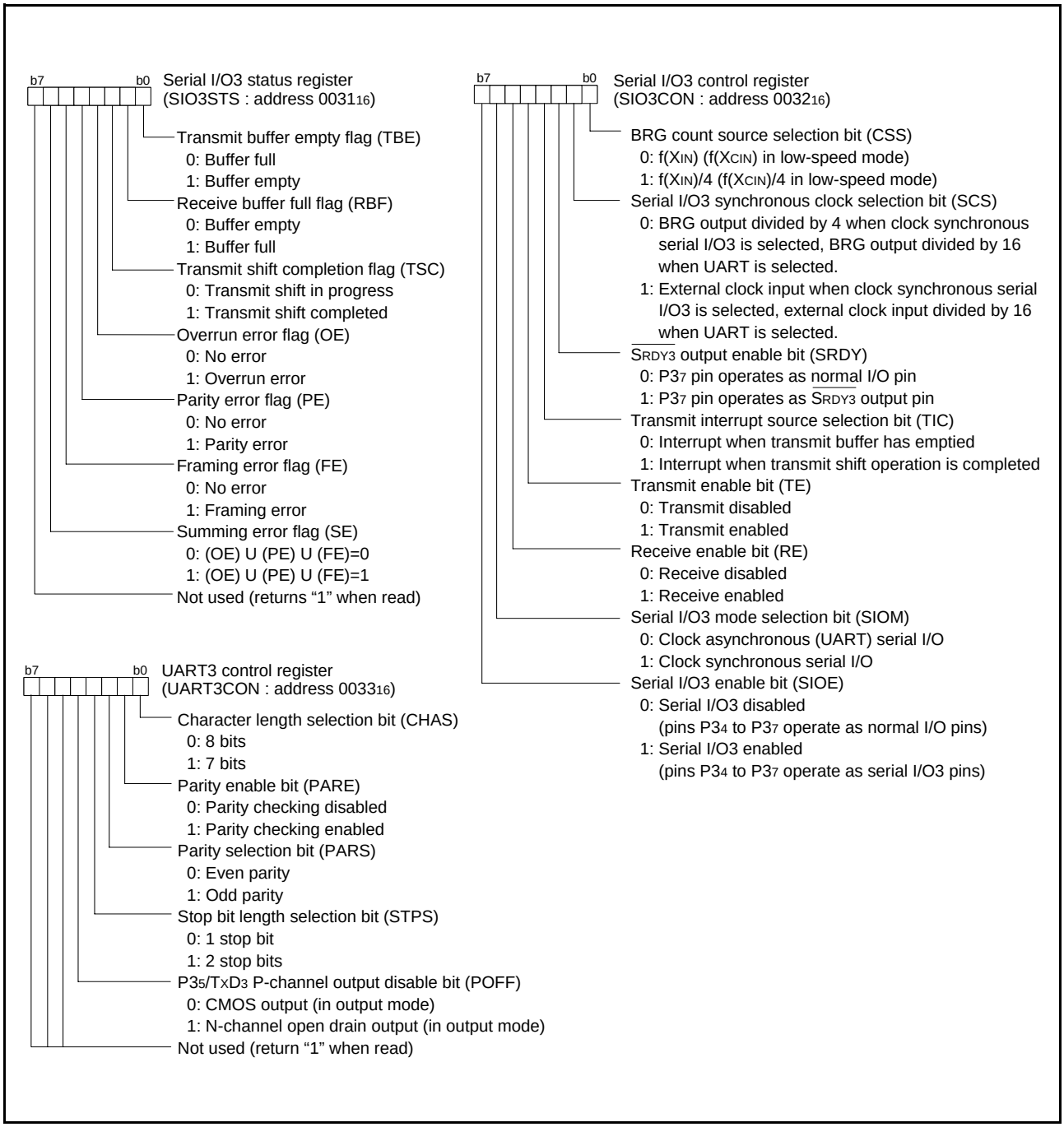


Fig 48. Structure of serial I/O3 control registers

<Notes concerning serial I/O3>

1. Notes when selecting clock synchronous serial I/O

1.1 Stop of transmission operation

• Note

Clear the serial I/O3 enable bit and the transmit enable bit to "0" (serial I/O and transmit disabled).

• Reason

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O3 enable bit is cleared to "0" (serial I/O disabled), the internal transmission is running (in this case, since pins TXD3, RXD3, SCLK3, and SRDY3 function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register 3 in this state, data starts to be shifted to the transmit shift register 3. When the serial I/O3 enable bit is set to "1" at this time, the data during internally shifting is output to the TXD3 pin and an operation failure occurs.

1.2 Stop of receive operation

• Note

Clear the receive enable bit to "0" (receive disabled), or clear the serial I/O3 enable bit to "0" (serial I/O disabled).

1.3 Stop of transmit/receive operation

• Note

Clear both the transmit enable bit and receive enable bit to "0" (transmit and receive disabled).

(when data is transmitted and received in the clock synchronous serial I/O mode, any one of data transmission and reception cannot be stopped.)

• Reason

In the clock synchronous serial I/O mode, the same clock is used for transmission and reception. If any one of transmission and reception is disabled, a bit error occurs because transmission and reception cannot be synchronized.

In this mode, the clock circuit of the transmission circuit also operates for data reception. Accordingly, the transmission circuit does not stop by clearing only the transmit enable bit to "0" (transmit disabled). Also, the transmission circuit is not initialized by clearing the serial I/O3 enable bit to "0" (serial I/O disabled) (refer to 1.1).

2. Notes when selecting clock asynchronous serial I/O

2.1 Stop of transmission operation

• Note

Clear the transmit enable bit to "0" (transmit disabled). The transmission operation does not stop by clearing the serial I/O3 enable bit to "0".

• Reason

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O3 enable bit is cleared to "0" (serial I/O disabled), the internal transmission is running (in this case, since pins TXD3, RXD3, SCLK3, and SRDY3 function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register 3 in this state, data starts to be shifted to the transmit shift register 3. When the serial I/O3 enable bit is set to "1" at this time, the data during internally shifting is output to the TXD3 pin and an operation failure occurs.

2.2 Stop of receive operation

• Note

Clear the receive enable bit to "0" (receive disabled).

2.3 Stop of transmit/receive operation

• Note 1 (only transmission operation is stopped)

Clear the transmit enable bit to "0" (transmit disabled). The transmission operation does not stop by clearing the serial I/O3 enable bit to "0".

• Reason

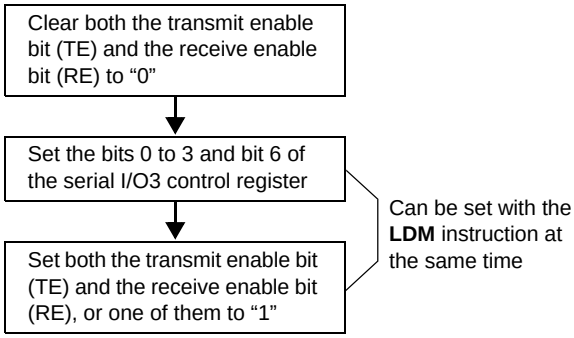
Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O3 enable bit is cleared to "0" (serial I/O disabled), the internal transmission is running (in this case, since pins TXD3, RXD3, SCLK3, and SRDY3 function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register 3 in this state, data starts to be shifted to the transmit shift register 3. When the serial I/O3 enable bit is set to "1" at this time, the data during internally shifting is output to the TXD3 pin and an operation failure occurs.

• Note 2 (only receive operation is stopped)

Clear the receive enable bit to "0" (receive disabled).

3. $\overline{\text{SRDY3}}$ output of reception side
- Note
  When signals are output from the $\overline{\text{SRDY3}}$ pin on the reception side by using an external clock in the clock synchronous serial I/O mode, set all of the receive enable bit, the $\overline{\text{SRDY3}}$ output enable bit, and the transmit enable bit to "1" (transmit enabled).

4. Setting serial I/O3 control register again
- Note
  Set the serial I/O3 control register again after the transmission and the reception circuits are reset by clearing both the transmit enable bit and the receive enable bit to "0".



5.Data transmission control with referring to transmit shift register completion flag
- Note
  After the transmit data is written to the transmit buffer register, the transmit shift register completion flag changes from "1" to "0" with a delay of 0.5 to 1.5 shift clocks. When data transmission is controlled with referring to the flag after writing the data to the transmit buffer register, note the delay.

6. Transmission control when external clock is selected
- Note
  When an external clock is used as the synchronous clock for data transmission, set the transmit enable bit to "1" at "H" of the SCLK3 input level. Also, write data to the transmit buffer register 3 at "H" of the SCLK input level.

7. Transmit interrupt request when transmit enable bit is set
- Note
  When using the transmit interrupt, take the following sequence.
  1. Set the serial I/O3 transmit interrupt enable bit to "0" (disabled).
  2. Set the transmit enable bit to "1".
  3. Set the AD converter/Serial I/O3 transmit interrupt request bit to "0" after 1 or more instruction has executed.
  4. Set the AD converter/Serial I/O3 transmit interrupt enable bit to "1" (enabled).

- Reason
  When the transmit enable bit is set to "1", the transmit buffer empty flag and the transmit shift register shift completion flag are also set to "1". Therefore, regardless of selecting which timing for the generating of transmit interrupts, the interrupt request is generated and the AD converter/Serial I/O3 transmit interrupt is set at this point.

PULSE WIDTH MODULATION (PWM)

The 3803 group (Spec.H QzROM version) has PWM functions with an 8-bit resolution, based on a signal that is the clock input XIN or that clock input divided by 2 or the clock input XCIN or that clock input divided by 2 in low-speed mode.

• Data Setting

The PWM output pin also functions as port P56. Set the PWM period by the PWM prescaler, and set the "H" term of output pulse by the PWM register.
If the value in the PWM prescaler is n and the value in the PWM register is m (where n = 0 to 255 and m = 0 to 255):
PWM period = 255 × (n+1) / f(XIN)
= 31.875 × (n+1) μs
(when f(XIN) = 8 MHz, count source selection bit = "0")
Output pulse "H" term = PWM period × m / 255
= 0.125 × (n+1) × m μs
(when f(XIN) = 8 MHz, count source selection bit = "0")

• PWM Operation

When bit 0 (PWM function enable bit) of the PWM control register is set to "1", operation starts by initializing the PWM output circuit, and pulses are output starting at an "H".
If the PWM register or PWM prescaler is updated during PWM output, the pulses will change in the cycle after the one in which the change was made.

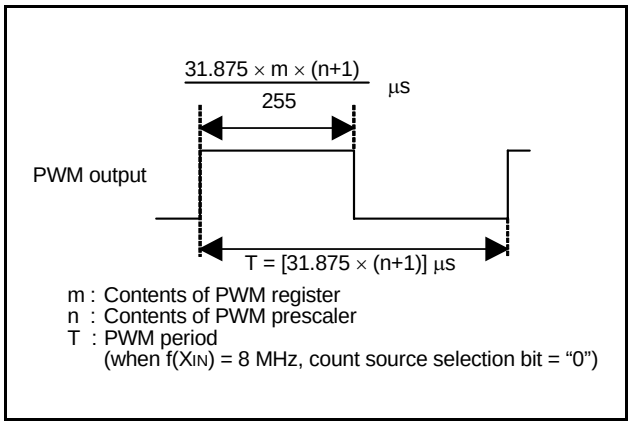


Fig 49. Timing of PWM period

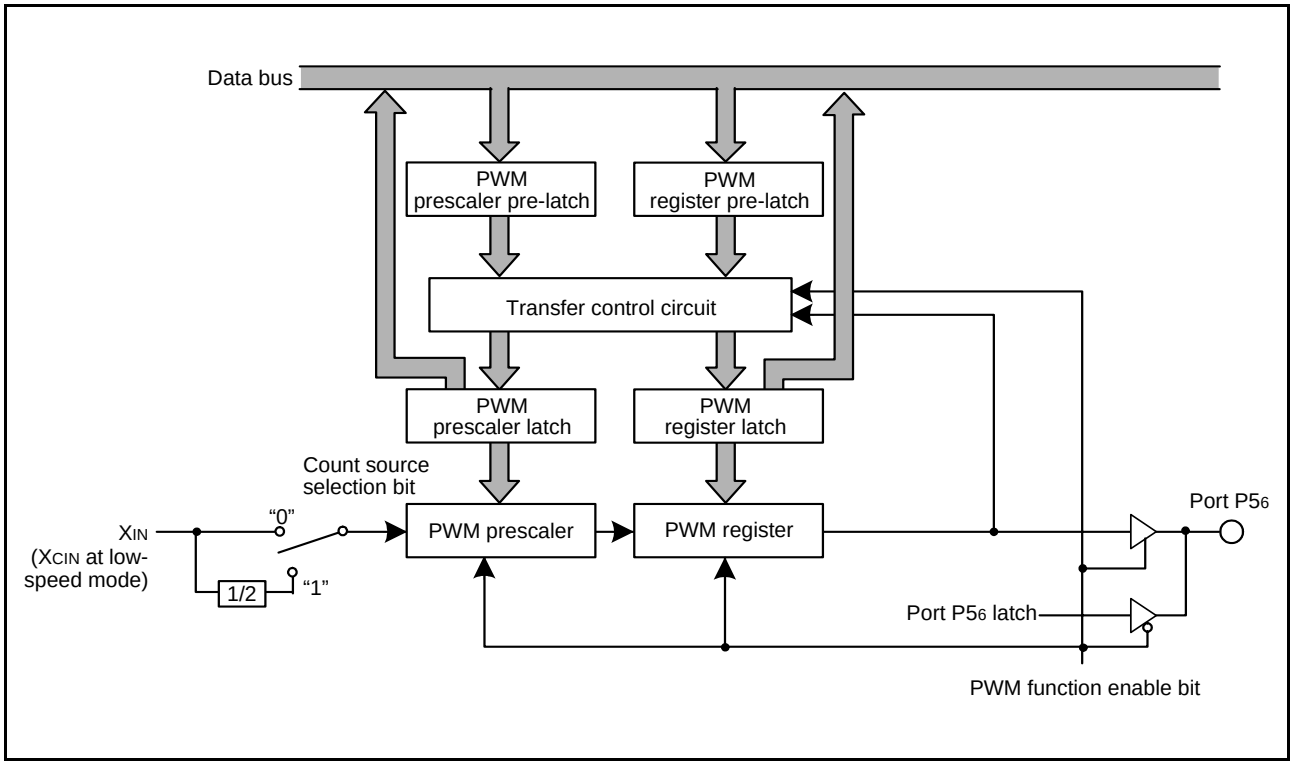


Fig 50. Block diagram of PWM function

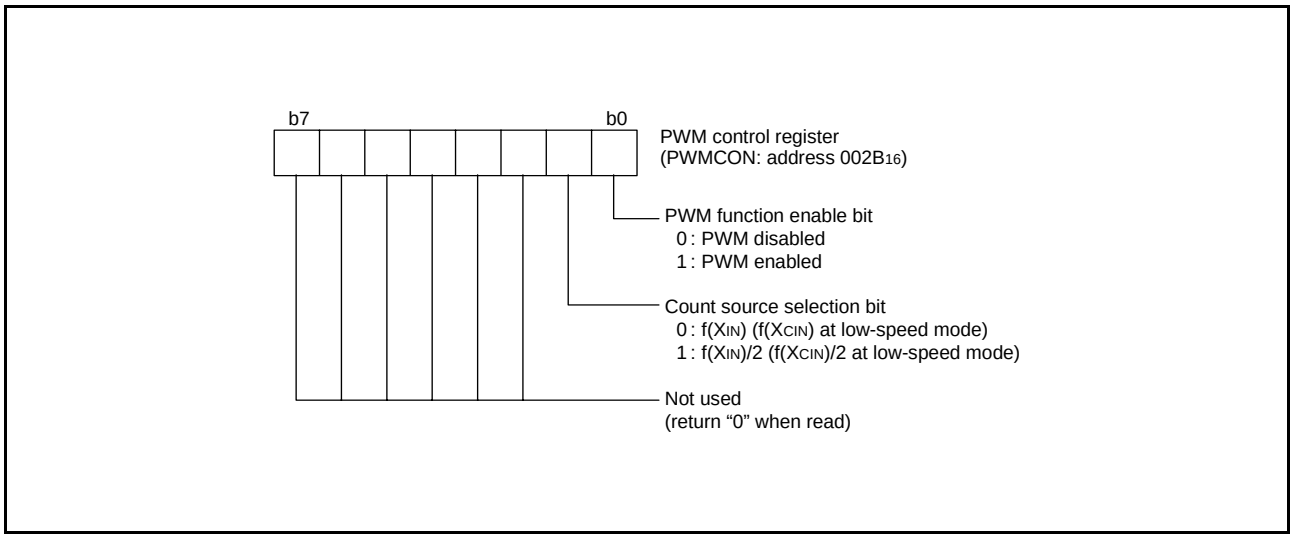


Fig 51. Structure of PWM control register

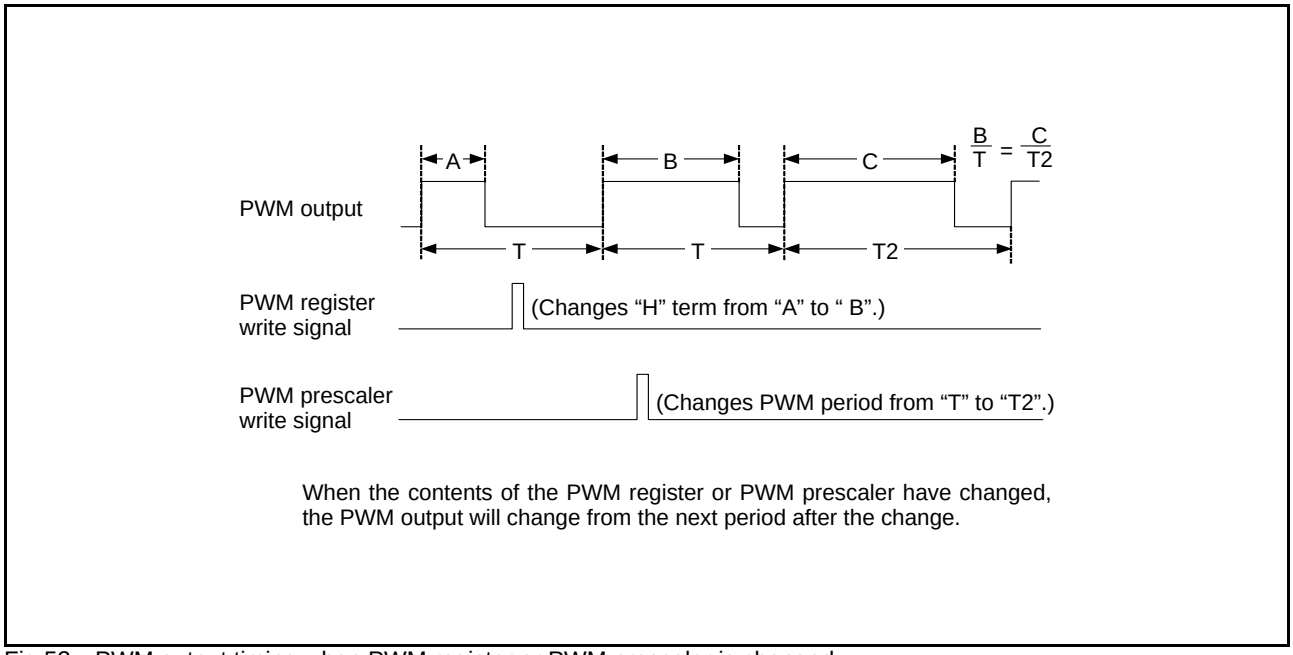


Fig 52. PWM output timing when PWM register or PWM prescaler is changed

<Notes>

The PWM starts after the PWM function enable bit is set to enable and "L" level is output from the PWM pin.
The length of this "L" level output is as follows:

$\frac{n+1}{2 \times f(X_{IN})}$ sec (Count source selection bit = 0, where n is the value set in the prescaler)

$\frac{n+1}{f(X_{IN})}$ sec (Count source selection bit = 1, where n is the value set in the prescaler)

A/D CONVERTER

[AD Conversion Register 1, 2] AD1, AD2

The AD conversion register is a read-only register that stores the result of an A/D conversion. When reading this register during an A/D conversion, the previous conversion result is read.

Bit 7 of the AD conversion register 2 is the conversion mode selection bit. When this bit is set to "0", the A/D converter becomes the 10-bit A/D mode. When this bit is set to "1", that becomes the 8-bit A/D mode. The conversion result of the 8-bit A/D mode is stored in the AD conversion register 1. As for 10-bit A/D mode, not only 10-bit reading but also only high-order 8-bit reading of conversion result can be performed by selecting the reading procedure of the AD conversion registers 1, 2 after A/D conversion is completed (in Figure 55).

As for 10-bit A/D mode, the 8-bit reading inclined to MSB is performed when reading the AD converter register 1 after A/D conversion is started; and when the AD converter register 1 is read after reading the AD converter register 2, the 8-bit reading inclined to LSB is performed.

[AD/DA Control Register] ADCON

The AD/DA control register controls the A/D conversion process. Bits 0 to 2 and bit 4 select a specific analog input pin. Bit 3 signals the completion of an A/D conversion. The value of this bit remains at "0" during an A/D conversion, and changes to "1" when an A/D conversion ends. Writing "0" to this bit starts the A/D conversion.

[Comparison Voltage Generator]

The comparison voltage generator divides the voltage between AVSS and VREF into 1024, and that outputs the comparison voltage in the 10-bit A/D mode (256 division in 8-bit A/D mode). The A/D converter successively compares the comparison voltage Vref in each mode, dividing the VREF voltage (see below), with the input voltage.

- 10-bit A/D mode (10-bit reading)

$$Vref = \frac{VREF}{1024} \times n \ (n = 0 - 1023)$$

- 10-bit A/D mode (8-bit reading)

$$Vref = \frac{VREF}{256} \times n \ (n = 0 - 255)$$

- 8-bit A/D mode

$$Vref = \frac{VREF}{256} \times n \ (n - 0.5) \ (n = 1 - 255)$$

$$= 0 \qquad (n = 0)$$

[Channel Selector]

The channel selector selects one of ports P67/AN7 to P60/AN0 or P07/AN15 to P00/AN8, and inputs the voltage to the comparator.

[Comparator and Control Circuit]

The comparator and control circuit compares an analog input voltage with the comparison voltage, and then stores the result in the AD conversion registers 1, 2. When an A/D conversion is completed, the control circuit sets the AD conversion completion bit and the AD converter/Serial I/O3 transmit interrupt request bit to "1".

Note that because the comparator consists of a capacitor coupling, set f(XIN) to 500 kHz or more during an A/D conversion.

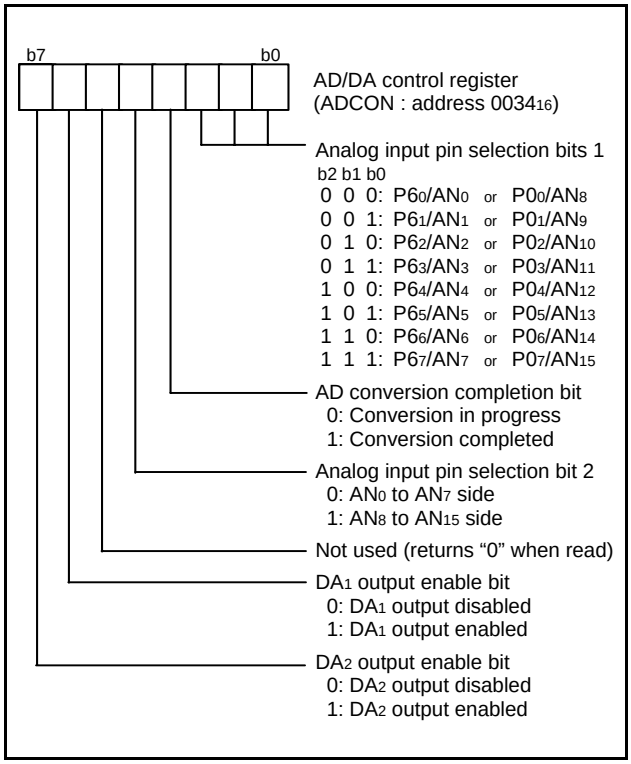


Fig 53. Structure of AD/DA control register

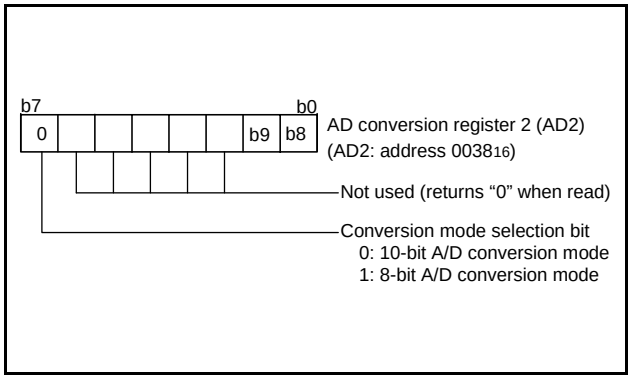


Fig 54. Structure of AD conversion register 2

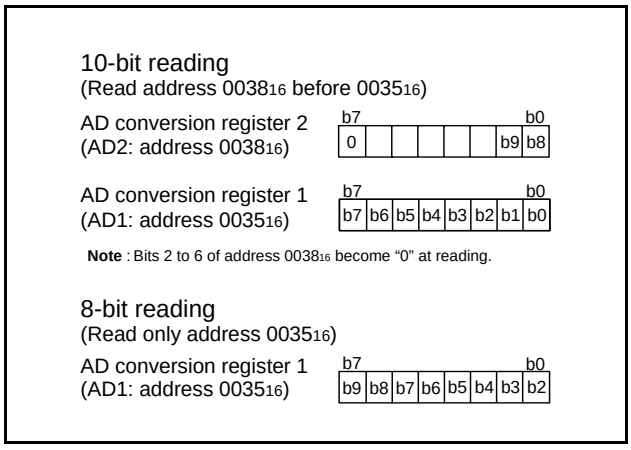


Fig 55. Structure of 10-bit A/D mode reading

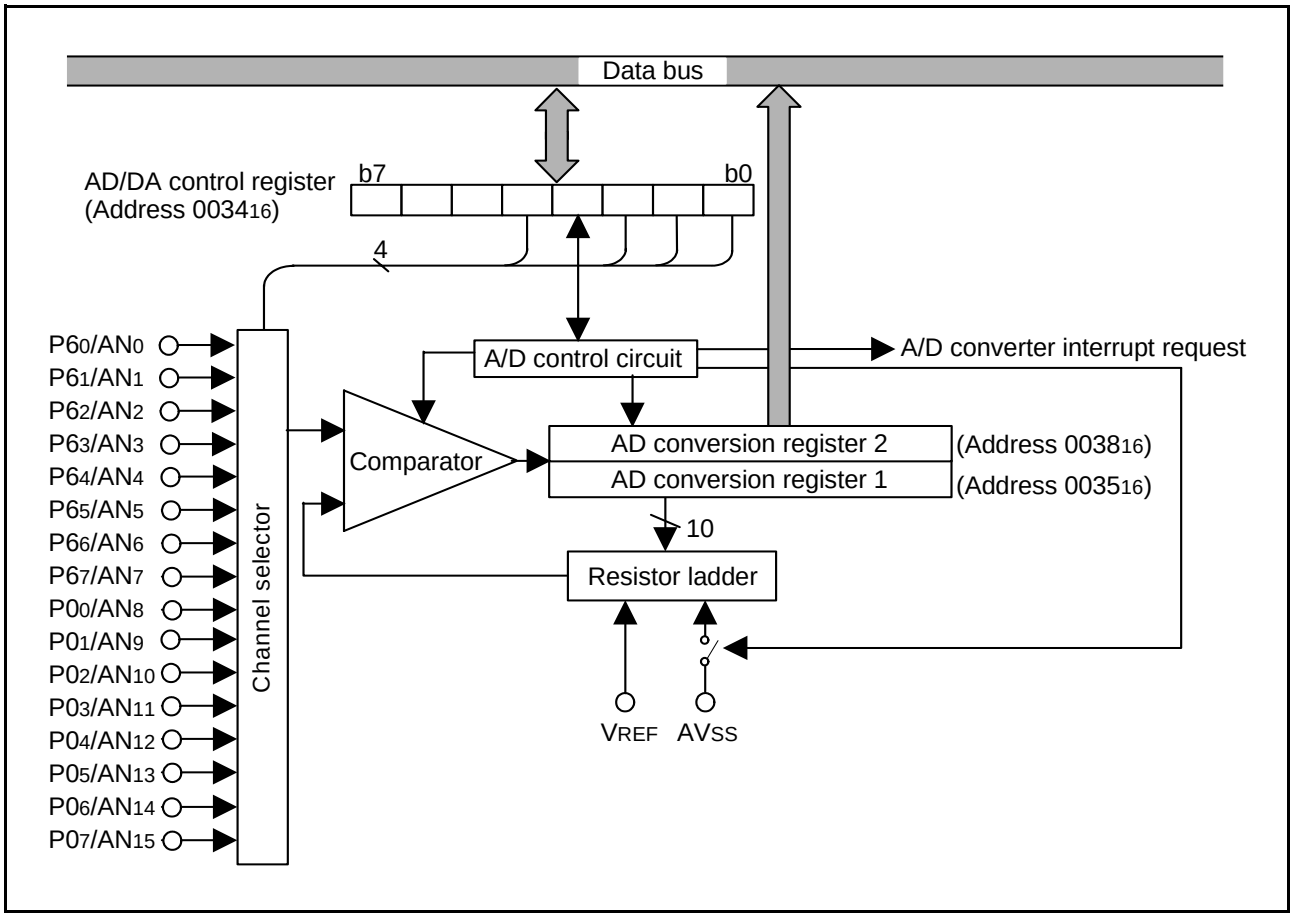


Fig 56. Block diagram of A/D converter

D/A CONVERTER

The 3803 group (Spec.H QzROM version) has two internal D/A converters (DA_1 and DA_2) with 8-bit resolution.
The D/A conversion is performed by setting the value in each DAi conversion register (i = 1 or 2). The result of D/A conversion is output from the DA_1 or DA_2 pin by setting the DAi output enable bit (i = 1 or 2) to "1".
When using the D/A converter, the corresponding port direction register bit ($P3_0/DA_1$ or $P3_1/DA_2$) must be set to "0" (input status).
The output analog voltage V is determined by the value n (decimal notation) in the DAi conversion register (i = 1 or 2) as follows:

$V = V_{REF} \times n/256$ (n = 0 to 255)
Where V_{REF} is the reference voltage.

At reset, the DAi conversion register (i = 1 or 2) is cleared to "00_{16}", and the DAi output enable bit (i = 1 or 2) is cleared to "0", and the $P3_0/DA_1$ and $P3_1/DA_2$ pins become high impedance.
The DA output does not have buffers. Accordingly, connect an external buffer when driving a low-impedance load.

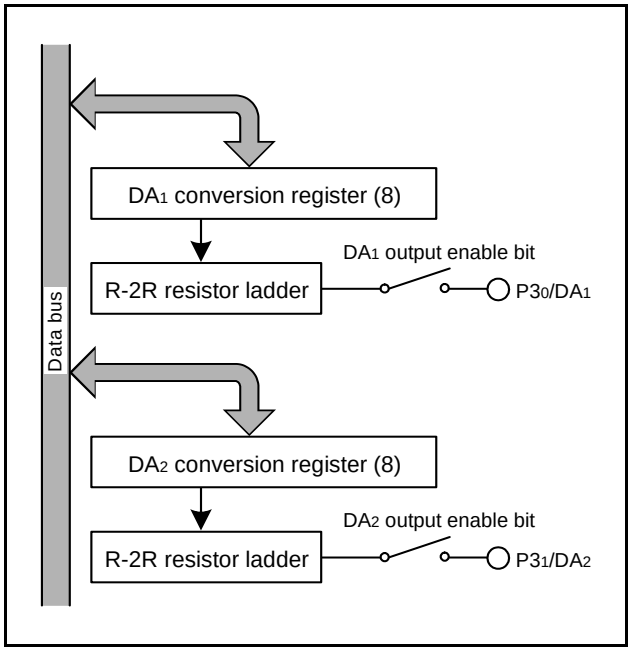


Fig 57. Block diagram of D/A converter

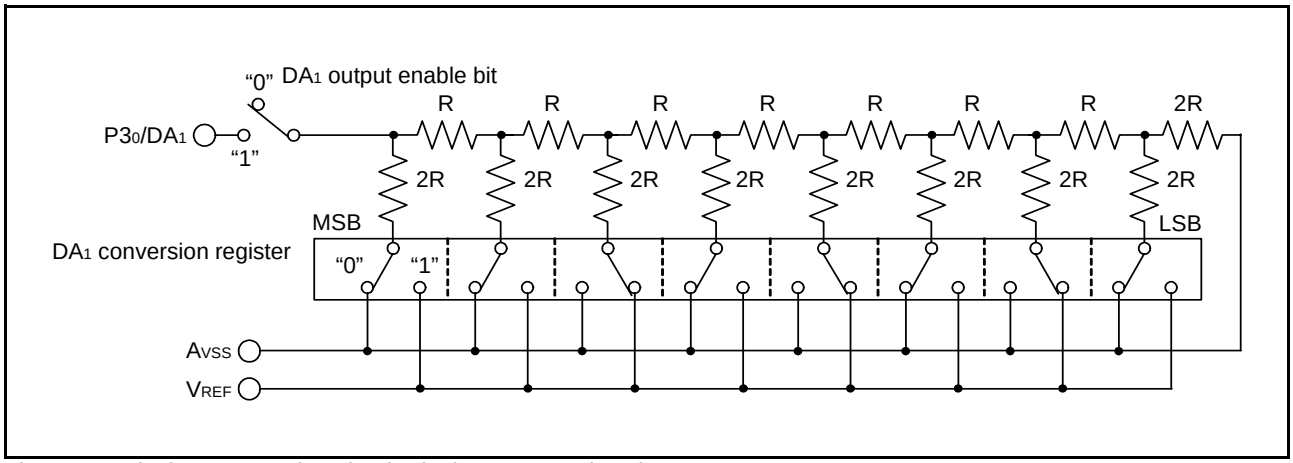


Fig 58. Equivalent connection circuit of D/A converter (DA1)

WATCHDOG TIMER

The watchdog timer gives a mean of returning to the reset status when a program cannot run on a normal loop (for example, because of a software run-away). The watchdog timer consists of an 8-bit watchdog timer L and an 8-bit watchdog timer H.

• Watchdog Timer Initial Value

Watchdog timer L is set to "FF16" and watchdog timer H is set to "FF16" by writing to the watchdog timer control register (address 001E16) or at a reset. Any write instruction that causes a write signal can be used, such as the STA, LDM, CLB, etc. Data can only be written to bits 6 and 7 of the watchdog timer control register. Regardless of the value written to bits 0 to 5, the above-mentioned value will be set to each timer.
Bit 6 can be written only once after releasing reset. After rewriting it is disable to write any data to this bit.

• Watchdog Timer Operations

The watchdog timer stops at reset and starts to count down by writing to the watchdog timer control register (address 001E16). An internal reset occurs at an underflow of the watchdog timer H. The reset is released after waiting for a reset release time and the program is processed from the reset vector address. Accordingly, programming is usually performed so that writing to the watchdog timer control register may be started before an underflow. If writing to the watchdog timer control register is not performed once, the watchdog timer does not function.

• Bit 6 of Watchdog Timer Control Register

- When bit 6 of the watchdog timer control register is "0", the MCU enters the stop mode by execution of STP instruction. Just after releasing the stop mode, the watchdog timer restarts counting(Note.). When executing the WIT instruction, the watchdog timer does not stop.
- When bit 6 is "1", execution of STP instruction causes an internal reset. When this bit is set to "1" once, it cannot be rewritten to "0" by program. Bit 6 is "0" at reset.

The following shows the period between the write execution to the watchdog timer control register and the underflow of watchdog timer H.

Bit 7 of the watchdog timer control register is "0":
when XCIN = 32.768 kHz; 32 s
when XIN = 16 MHz; 65.536 ms

Bit 7 of the watchdog timer control register is "1":
when XCIN = 32.768 kHz; 125 ms
when XIN = 16 MHz; 256 μs

Note. The watchdog timer continues to count even while waiting for a stop release. Therefore, make sure that watchdog timer H does not underflow during this period.

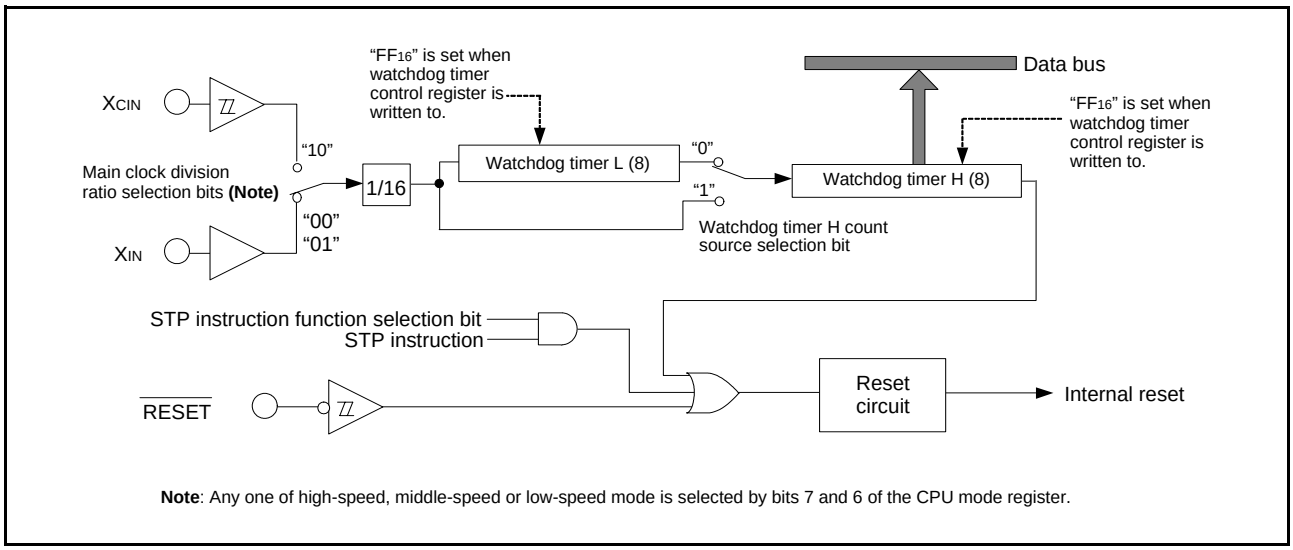


Fig 59. Block diagram of Watchdog timer

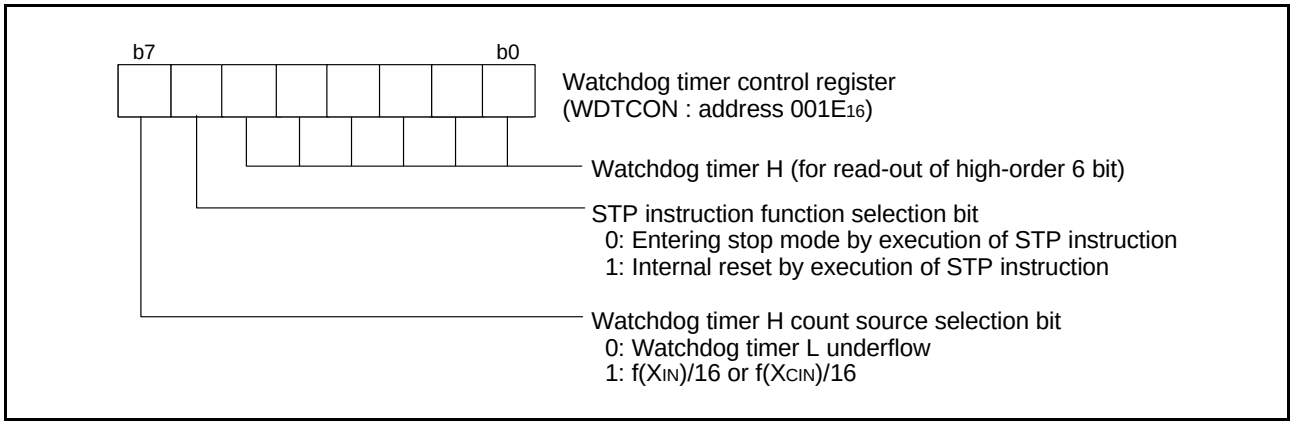


Fig 60. Structure of Watchdog timer control register

RESET CIRCUIT

To reset the microcomputer, $\overline{\text{RESET}}$ pin should be held at an "L" level for 16 cycles or more of XIN. Then the $\overline{\text{RESET}}$ pin is returned to an "H" level (the power source voltage should be between 1.8 V and 5.5 V, and the oscillation should be stable), reset is released. After the reset is completed, the program starts from the address contained in address FFFD16 (high-order byte) and address FFFC16 (low-order byte). Make sure that the reset input voltage is less than 0.29 V for VCC of 1.8 V.

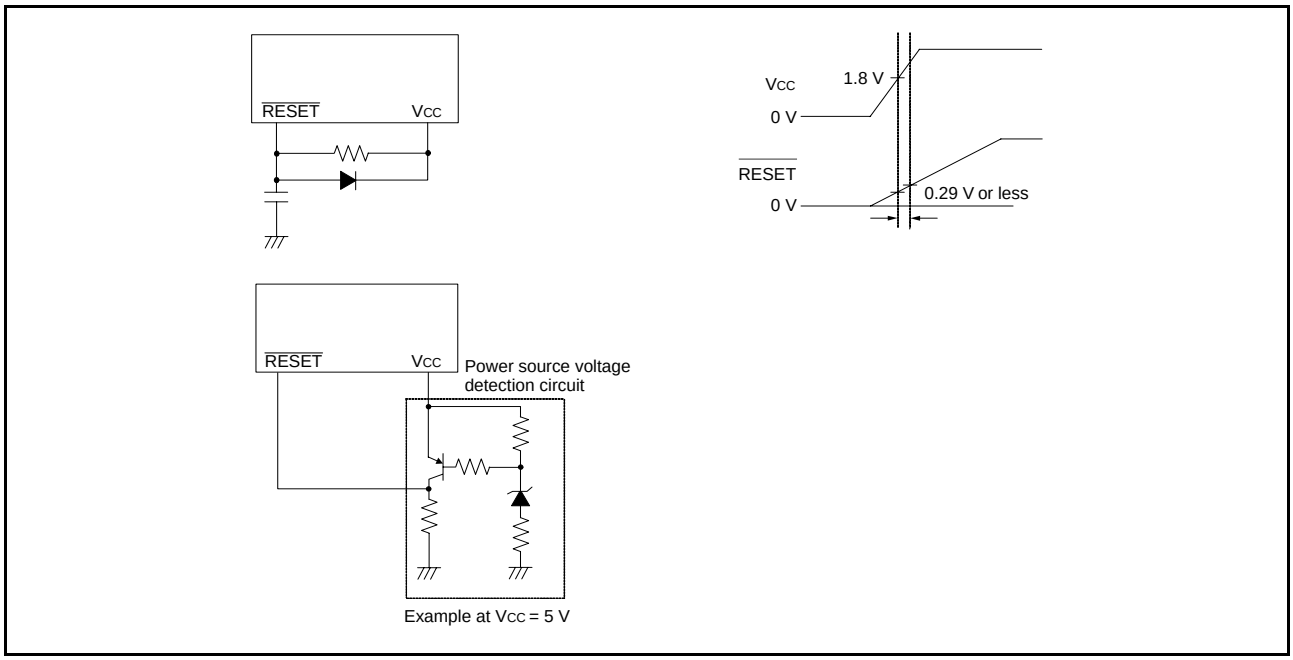
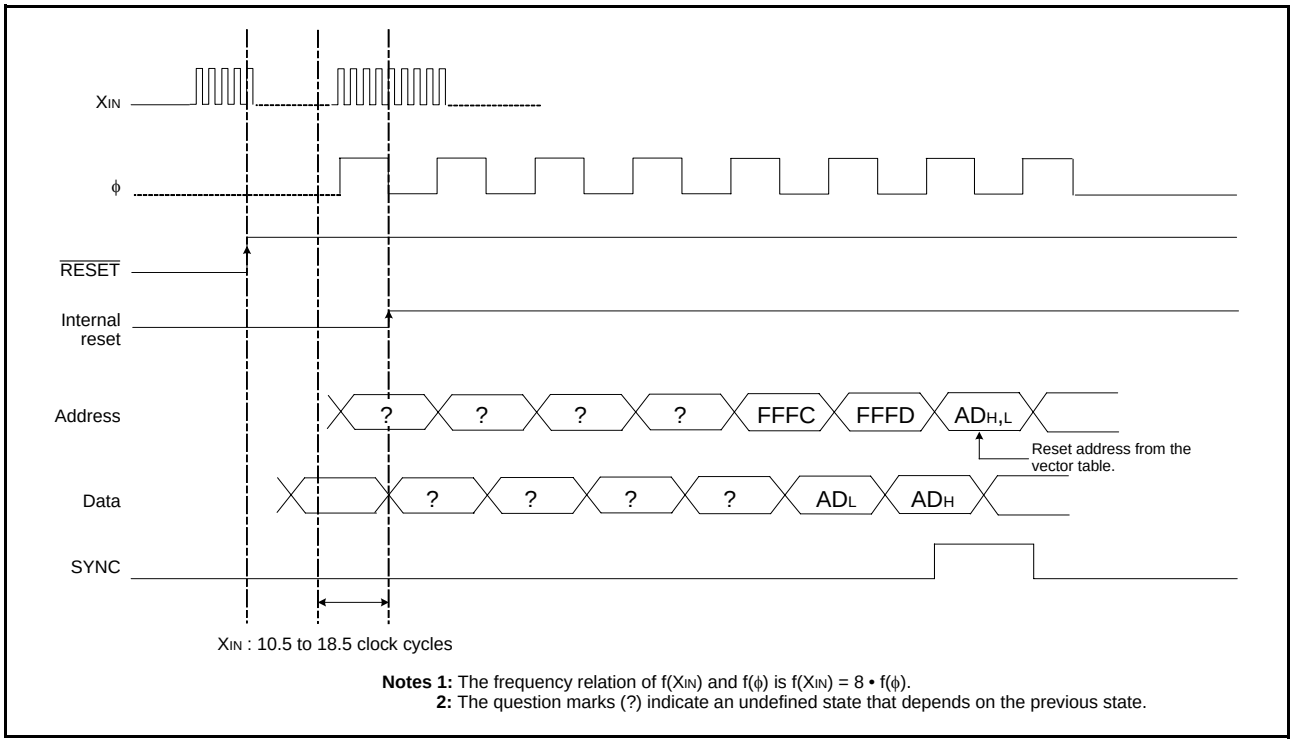


Fig 61. Reset circuit example



Notes 1: The frequency relation of f(XIN) and f(ϕ) is f(XIN) = 8 • f(ϕ).
2: The question marks (?) indicate an undefined state that depends on the previous state.

Fig 62. Reset sequence

		Address	Register contents
(1)	Port P0 (P0)	0000_{16}	00_{16}
(2)	Port P0 direction register (P0D)	0001_{16}	00_{16}
(3)	Port P1 (P1)	0002_{16}	00_{16}
(4)	Port P1 direction register (P1D)	0003_{16}	00_{16}
(5)	Port P2 (P2)	0004_{16}	00_{16}
(6)	Port P2 direction register (P2D)	0005_{16}	00_{16}
(7)	Port P3 (P3)	0006_{16}	00_{16}
(8)	Port P3 direction register (P3D)	0007_{16}	00_{16}
(9)	Port P4 (P4)	0008_{16}	00_{16}
(10)	Port P4 direction register (P4D)	0009_{16}	00_{16}
(11)	Port P5 (P5)	$000A_{16}$	00_{16}
(12)	Port P5 direction register (P5D)	$000B_{16}$	00_{16}
(13)	Port P6 (P6)	$000C_{16}$	00_{16}
(14)	Port P6 direction register (P6D)	$000D_{16}$	00_{16}
(15)	Timer 12, X count source selection register (T12XCSS)	$000E_{16}$	0 0 1 1 0 0 1 1
(16)	Timer Y, Z count source selection register (TYZCSS)	$000F_{16}$	0 0 1 1 0 0 1 1
(17)	MISRG	0010_{16}	00_{16}
(18)	Transmit/Receive buffer register 1 (TB1/RB1)	0018_{16}	X X X X X X X X
(19)	Serial I/O1 status register (SIO1STS)	0019_{16}	1 0 0 0 0 0 0 0
(20)	Serial I/O1 control register (SIO1CON)	$001A_{16}$	00_{16}
(21)	UART1 control register (UART1CON)	$001B_{16}$	1 1 1 0 0 0 0 0
(22)	Baud rate generator 1 (BRG1)	$001C_{16}$	X X X X X X X X
(23)	Serial I/O2 control register (SIO2CON)	$001D_{16}$	00_{16}
(24)	Watchdog timer control register (WDTCON)	$001E_{16}$	0 0 1 1 1 1 1 1
(25)	Serial I/O2 register (SIO2)	$001F_{16}$	X X X X X X X X
(26)	Prescaler 12 (PRE12)	0020_{16}	FF_{16}
(27)	Timer 1 (T1)	0021_{16}	01_{16}
(28)	Timer 2 (T2)	0022_{16}	FF_{16}
(29)	Timer XY mode register (TM)	0023_{16}	00_{16}
(30)	Prescaler X (PREX)	0024_{16}	FF_{16}
(31)	Timer X (TX)	0025_{16}	FF_{16}
(32)	Prescaler Y (PREY)	0026_{16}	FF_{16}
(33)	Timer Y (TY)	0027_{16}	FF_{16}

		Address	Register contents
(34)	Timer Z (low-order) (TZL)	0028_{16}	FF_{16}
(35)	Timer Z (high-order) (TZH)	0029_{16}	FF_{16}
(36)	Timer Z mode register (TZM)	$002A_{16}$	00_{16}
(37)	PWM control register (PWMCON)	$002B_{16}$	00_{16}
(38)	PWM prescaler (PREPWM)	$002C_{16}$	X X X X X X X X
(39)	PWM register (PWM)	$002D_{16}$	X X X X X X X X
(40)	Baud rate generator 3 (BRG3)	$002F_{16}$	X X X X X X X X
(41)	Transmit/Receive buffer register 3 (TB3/RB3)	0030_{16}	X X X X X X X X
(42)	Serial I/O3 status register (SIO3STS)	0031_{16}	1 0 0 0 0 0 0 0
(43)	Serial I/O3 control register (SIO3CON)	0032_{16}	00_{16}
(44)	UART3 control register (UART3CON)	0033_{16}	1 1 1 0 0 0 0 0
(45)	AD/DA control register (ADCON)	0034_{16}	0 0 0 0 1 0 0 0
(46)	AD conversion register 1 (AD1)	0035_{16}	X X X X X X X X
(47)	DA1 conversion register (DA1)	0036_{16}	00_{16}
(48)	DA2 conversion register (DA2)	0037_{16}	00_{16}
(49)	AD conversion register 2 (AD2)	0038_{16}	0 0 0 0 0 0 X X
(50)	Interrupt source selection register (INTSEL)	0039_{16}	00_{16}
(51)	Interrupt edge selection register (INTEDGE)	$003A_{16}$	00_{16}
(52)	CPU mode register (CPUM)	$003B_{16}$	0 1 0 0 1 0 0 0
(53)	Interrupt request register 1 (IREQ1)	$003C_{16}$	00_{16}
(54)	Interrupt request register 2 (IREQ2)	$003D_{16}$	00_{16}
(55)	Interrupt control register 1 (ICON1)	$003E_{16}$	00_{16}
(56)	Interrupt control register 2 (ICON2)	$003F_{16}$	00_{16}
(57)	Port P0 pull-up control register (PULL0)	$0FF0_{16}$	00_{16}
(58)	Port P1 pull-up control register (PULL1)	$0FF1_{16}$	00_{16}
(59)	Port P2 pull-up control register (PULL2)	$0FF2_{16}$	00_{16}
(60)	Port P3 pull-up control register (PULL3)	$0FF3_{16}$	00_{16}
(61)	Port P4 pull-up control register (PULL4)	$0FF4_{16}$	00_{16}
(62)	Port P5 pull-up control register (PULL5)	$0FF5_{16}$	00_{16}
(63)	Port P6 pull-up control register (PULL6)	$0FF6_{16}$	00_{16}
(64)	Processor status register	(PS)	X X X X X 1 X X
(65)	Program counter	(PC_H)	$FFFD_{16}$ contents
		(PC_L)	$FFFC_{16}$ contents

Note : X: Not fixed.
Since the initial values for other than above mentioned registers and RAM contents are indefinite at reset, they must be set.

Fig 63. Internal status at reset

CLOCK GENERATING CIRCUIT

The 3803 group (Spec.H QzROM version) has two built-in oscillation circuits: main clock XIN-XOUT oscillation circuit and sub clock XCIN-XCOUT oscillation circuit. An oscillation circuit can be formed by connecting a resonator between XIN and XOUT (XCIN and XCOUT). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip.(An external feed-back resistor may be needed depending on conditions.) However, an external feed-back resistor is needed between XCIN and XCOUT.
Immediately after power on, only the XIN oscillation circuit starts oscillating, and XCIN and XCOUT pins function as I/O ports.

• Frequency Control

(1) Middle-speed mode

The internal clock ϕ is the frequency of XIN divided by 8. After reset is released, this mode is selected.

(2) High-speed mode

The internal clock ϕ is half the frequency of XIN.

(3) Low-speed mode

The internal clock ϕ is half the frequency of XCIN.

(4) Low power dissipation mode

The low power consumption operation can be realized by stopping the main clock XIN in low-speed mode. To stop the main clock, set bit 5 of the CPU mode register to "1". When the main clock XIN is restarted (by setting the main clock stop bit to "0"), set sufficient time for oscillation to stabilize.
The sub-clock XCIN-XCOUT oscillating circuit can not directly input clocks that are generated externally. Accordingly, make sure to cause an external resonator to oscillate.

Oscillation Control

(1) Stop mode

If the STP instruction is executed, the internal clock ϕ stops at an "H" level, and XIN and XCIN oscillators stop. When the oscillation stabilizing time set after STP instruction released bit (bit 0 of address 0010_{16}) is "0", the prescaler 12 is set to "FF_{16}" and timer 1 is set to "01_{16}". When the oscillation stabilizing time set after STP instruction released bit is "1", set the sufficient time for oscillation of used oscillator to stabilize since nothing is set to the prescaler 12 and timer 1.
After STP instruction is released, the input of the prescaler 12 is connected to count source which had set at executing the STP instruction, and the output of the prescaler 12 is connected to timer 1. Oscillator restarts when an external interrupt is received, but the internal clock ϕ is not supplied to the CPU (remains at "H") until timer 1 underflows. The internal clock ϕ is supplied for the first time, when timer 1 underflows. This ensures time for the clock oscillation using the ceramic resonators to be stabilized. When the oscillator is restarted by reset, apply "L" level to the $\overline{\text{RESET}}$ pin until the oscillation is stable since a wait time will not be generated.

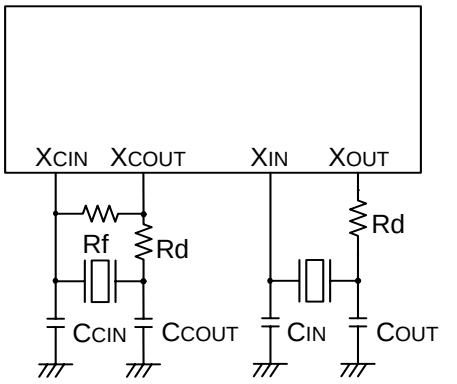
(2) Wait mode

If the WIT instruction is executed, the internal clock ϕ stops at an "H" level, but the oscillator does not stop. The internal clock ϕ restarts at reset or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

To ensure that the interrupts will be received to release the STP or WIT state, their interrupt enable bits must be set to "1" before executing of the STP or WIT instruction.
When releasing the STP state, the prescaler 12 and timer 1 will start counting the clock XIN divided by 16. Accordingly, set the timer 1 interrupt enable bit to "0" before executing the STP instruction.

<Notes>

- If you switch the mode between middle/high-speed and low-speed, stabilize both XIN and XCIN oscillations. The sufficient time is required for the sub clock to stabilize, especially immediately after power on and at returning from stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency on condition that f(XIN) > 3×f(XCIN).
- When using the quartz-crystal oscillator of high frequency, such as 16 MHz etc., it may be necessary to select a specific oscillator with the specification demanded.
- When using the oscillation stabilizing time set after STP instruction released bit set to "1", evaluate time to stabilize oscillation of the used oscillator and set the value to the timer 1 and prescaler 12.



Notes : Insert a damping resistor if required.
The resistance will vary depending on the oscillator and the oscillation drive capacity setting.
Use the value recommended by the maker of the oscillator.
Also, if the oscillator manufacturer's data sheet specifies to add a feedback resistor externally to the chip though a feedback resistor exists on-chip, insert a feedback resistor between XIN and XOUT following the instruction.

Fig 64. Ceramic resonator circuit

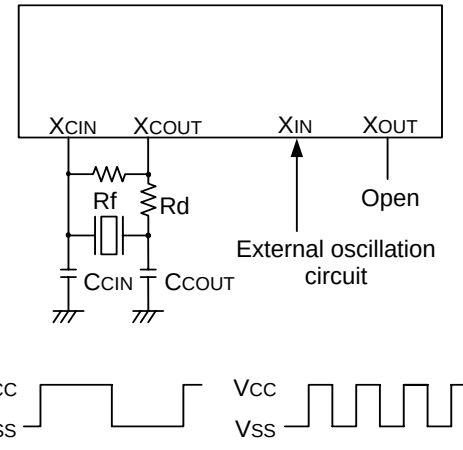
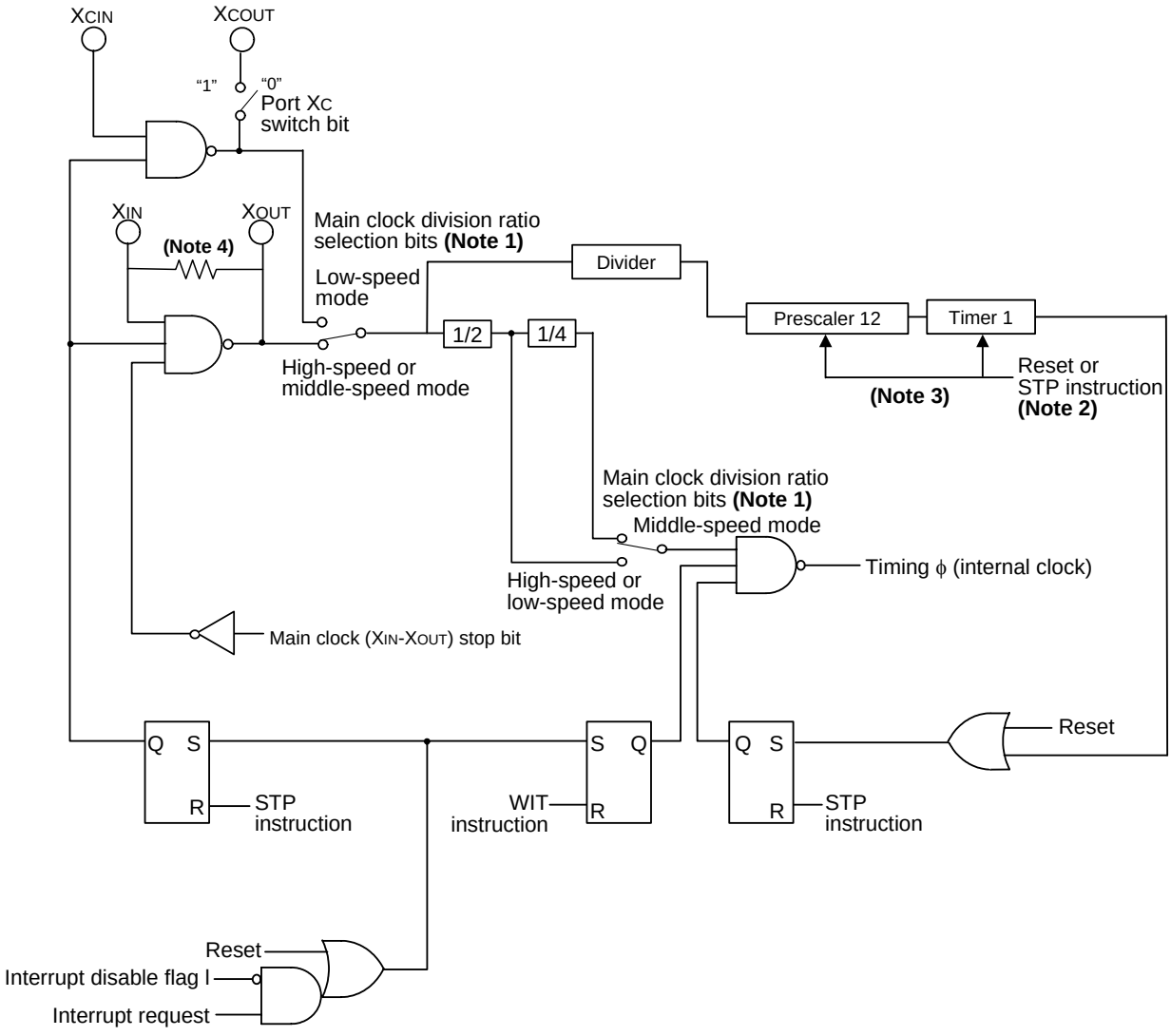


Fig 65. External clock input circuit



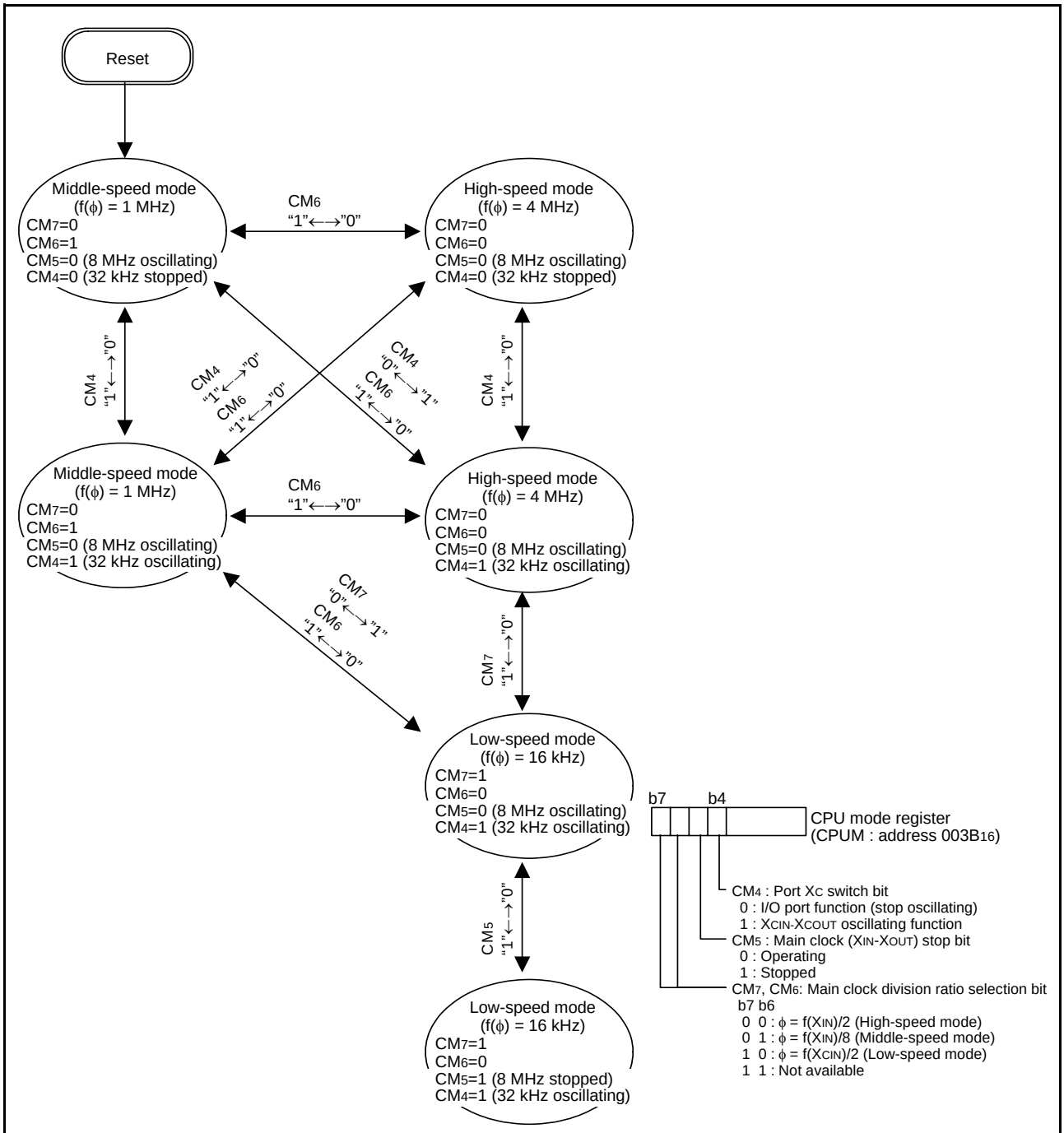
Notes 1: Either high-speed, middle-speed or low-speed mode is selected by bits 7 and 6 of the CPU mode register. When low-speed mode is selected, set port X_C switch bit (b4) to "1".

2: f(X_{IN})/16 is supplied as the count source to the prescaler 12 at reset, the count source before executing the STP instruction is supplied as the count source at executing STP instruction.

3: When bit 0 of MISRG is "0", timer 1 is set "01_{16}" and prescaler 12 is set "FF_{16}" automatically. When bit 0 of MISRG is "1" , set the appropriate value to them in accordance with oscillation stabilizing time required by the using oscillator because nothing is automatically set into timer 1 and prescaler 12.

4: Although a feed-back resistor exists on-chip, an external feed-back resistor may be needed depending on conditions.

Fig 66. System clock generating circuit block diagram (Single-chip mode)



Notes1: Switch the mode by the allows shown between the mode blocks. (Do not switch between the modes directly without an allow.)
2: The all modes can be switched to the stop mode or the wait mode and return to the source mode when the stop mode or the wait mode is ended.
3: Timer operates in the wait mode.
4: When the stop mode is ended, a delay of approximately 1 ms occurs by connecting prescaler 12 and Timer 1 in middle/high-speed mode.
5: When the stop mode is ended, a delay of approximately 0.25 s occurs by Timer 1 and Timer 2 in low-speed mode.
6: Wait until oscillation stabilizes after oscillating the main clock XIN before the switching from the low-speed mode to middle/high-speed mode.
7: The example assumes that 8 MHz is being applied to the XIN pin and 32 kHz to the XCIN pin. ϕ indicates the internal clock.

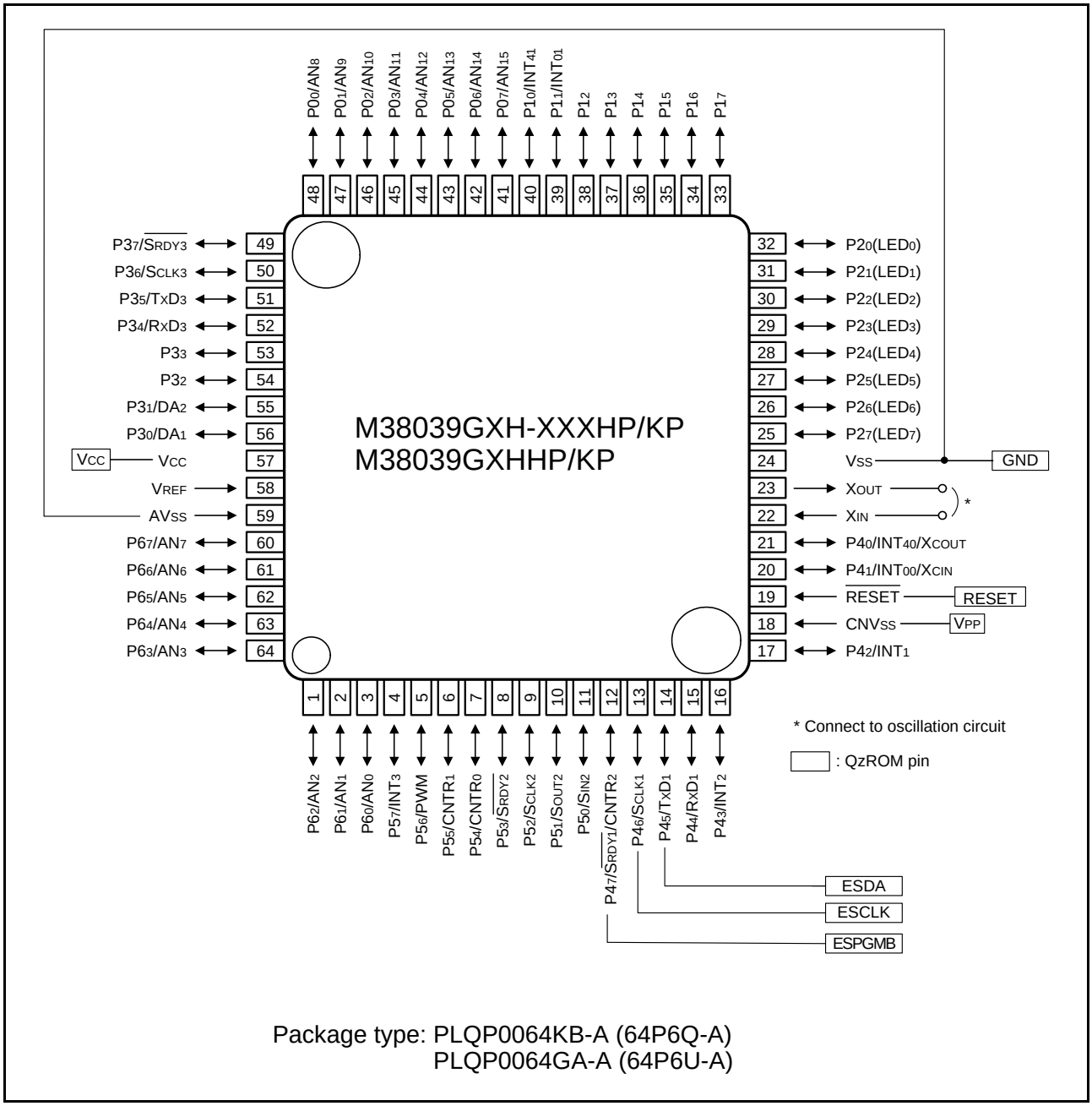
Fig 67. State transitions of system clock

QzROM Writing Mode

In the QzROM writing mode, the user ROM area can be rewritten while the microcomputer is mounted on-board by using a serial programmer which is applicable for this microcomputer.
Table 9 lists the pin description (QzROM writing mode) and Figure 68 to Figure 70 show the pin connections.
Refer to Figure 71 and Figure 72 for examples of a connection with a serial programmer.
Contact the manufacturer of your serial programmer for serial programmer. Refer to the user's manual of your serial programmer for details on how to use it.

Table 9 Pin description (QzROM writing mode)

Pin	Name	I/O	Function
V_{CC}, V_{SS}	Power source	Input	Apply 2.7 to 5.5 V to V_{CC}, and 0 V to V_{SS}.
CNVss	V_{PP} input	Input	QzROM programmable power source pin.
V_{REF}	Analog reference voltage	Input	Input the reference voltage of A/D converter and D/A converter to V_{REF}.
AVss	Analog power source	Input	Connect AVss to Vss.
$\overline{\text{RESET}}$	Reset input	Input	Reset input pin for active "L". Reset occurs when $\overline{\text{RESET}}$ pin is held at an "L" level for 16 cycles or more of X_{IN}.
X_{IN}	Clock input	Input	Set the same termination as the single-chip mode.
X_{OUT}	Clock output	Output	
$P0_0$–$P0_7$ $P1_0$–$P1_7$ $P2_0$–$P2_7$ $P3_3$–$P3_7$ $P4_0$, $P4_4$ $P5_0$–$P5_7$ $P6_0$–$P6_7$	I/O port	I/O	Input "H" or "L" level signal or leave the pin open.
$P4_5$	ESDA input/output	I/O	Serial data I/O pin.
$P4_6$	ESCLK input	Input	Serial clock input pin.
$P4_7$	ESPGMB input	Input	Read/program pulse input pin.



Package type: PLQP0064KB-A (64P6Q-A)
PLQP0064GA-A (64P6U-A)

Fig. 68 Pin connection diagram (M38039GXH-XXXHP/KP, M38039GXHHP/KP)

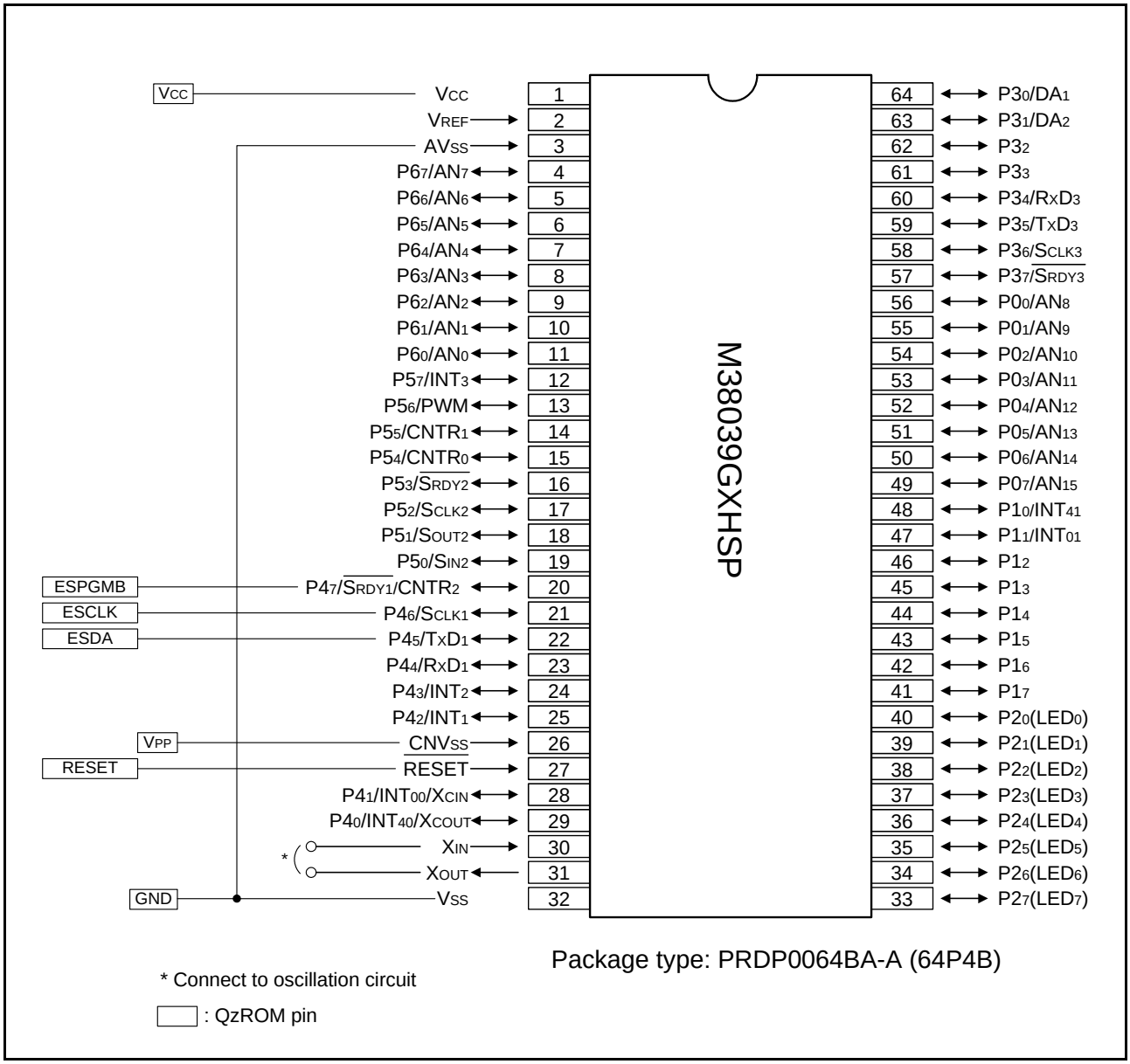
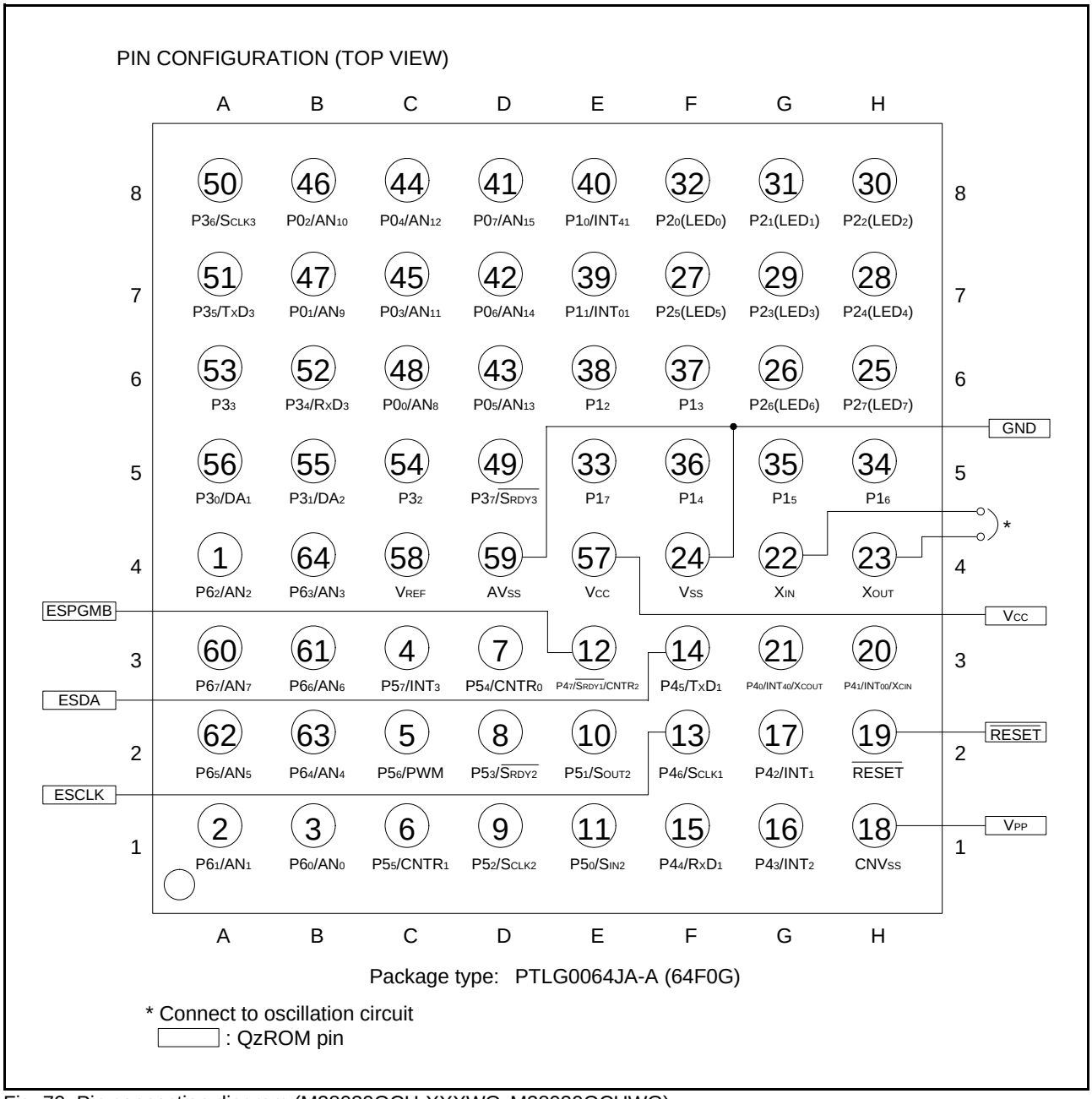


Fig. 69 Pin connection diagram (M38039GXHSP)

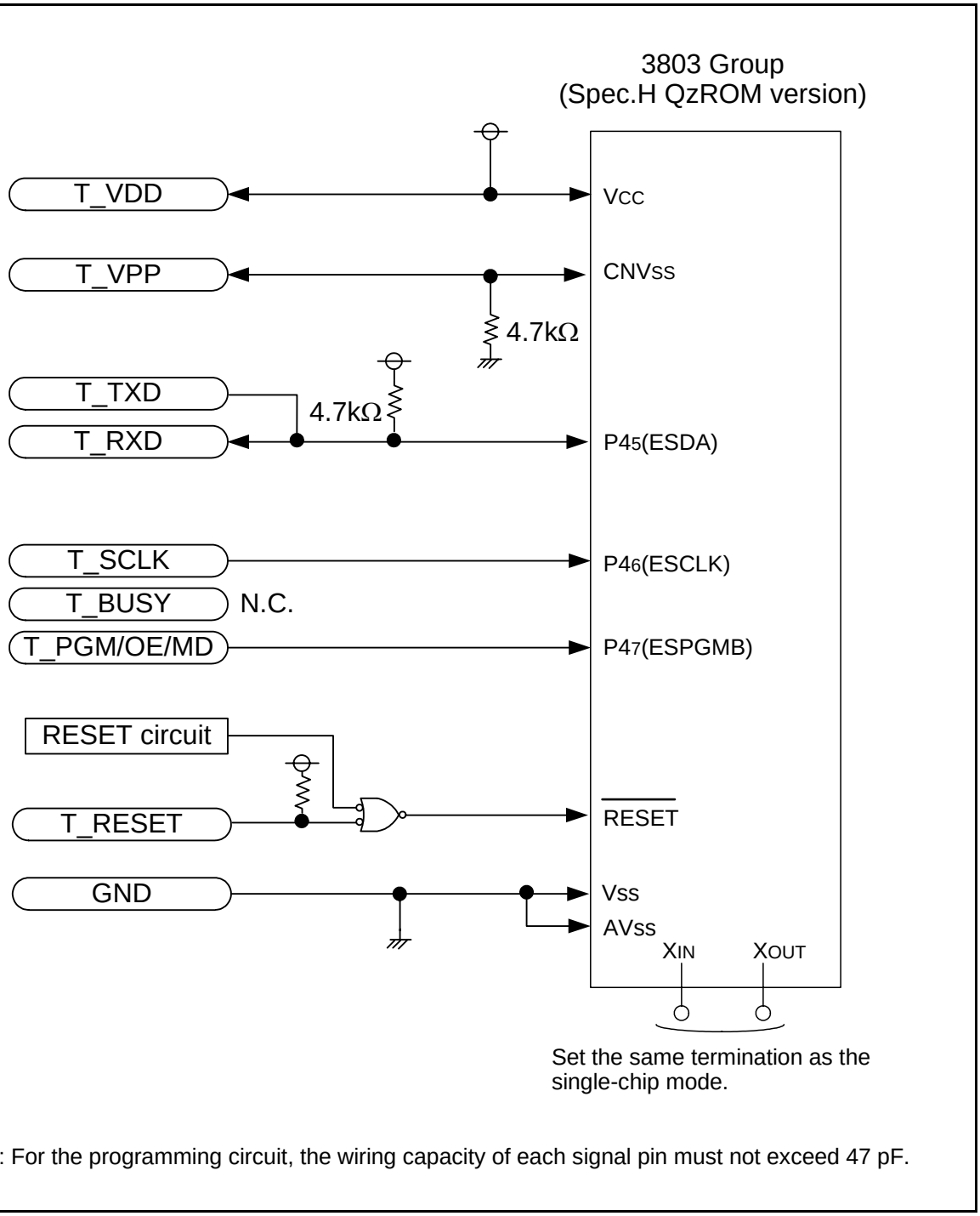


Package type: PTLG0064JA-A (64F0G)

* Connect to oscillation circuit

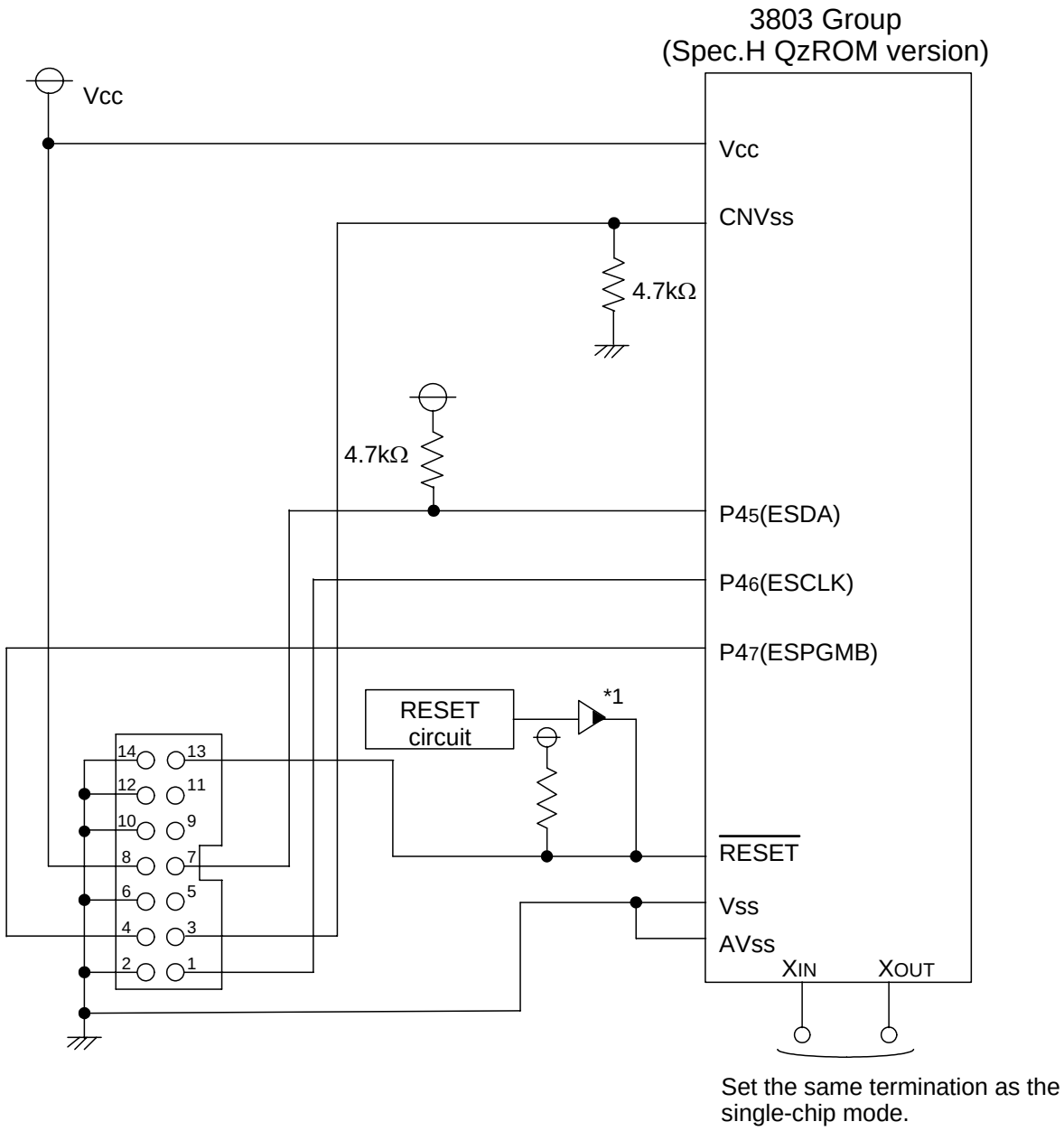
□ : QzROM pin

Fig. 70 Pin connection diagram (M38039GCH-XXXWG, M38039GCHWG)



Note: For the programming circuit, the wiring capacity of each signal pin must not exceed 47 pF.

Fig. 71 When using programmer of Suisei Electronics System Co., LTD, connection example



*1: Open-collector buffer

Note: For the programming circuit, the wiring capacity of each signal pin must not exceed 47 pF.

Fig. 72 When using E8 programmer connection example

NOTES

NOTES ON PROGRAMMING

1. Processor Status Register

(1) Initializing of processor status register

Flags which affect program execution must be initialized after a reset. In particular, it is essential to initialize the T and D flags because they have an important effect on calculations. Initialize these flags at beginning of the program.

<Reason>

After a reset, the contents of the processor status register (PS) are undefined except for the I flag which is "1".

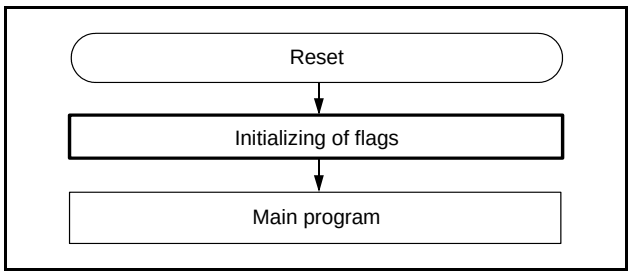


Fig 73. Initialization of processor status register

(2) How to reference the processor status register

To reference the contents of the processor status register (PS), execute the PHP instruction once then read the contents of (S+1). If necessary, execute the PLP instruction to return the PS to its original status.

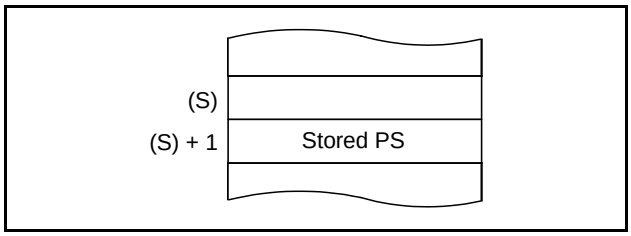


Fig 74. Stack memory contents after PHP instruction execution

2. Decimal calculations

(1) Execution of decimal calculations

The ADC and SBC are the only instructions which will yield proper decimal notation, set the decimal mode flag (D) to "1" with the SED instruction. After executing the ADC or SBC instruction, execute another instruction before executing the SEC, CLC, or CLD instruction.

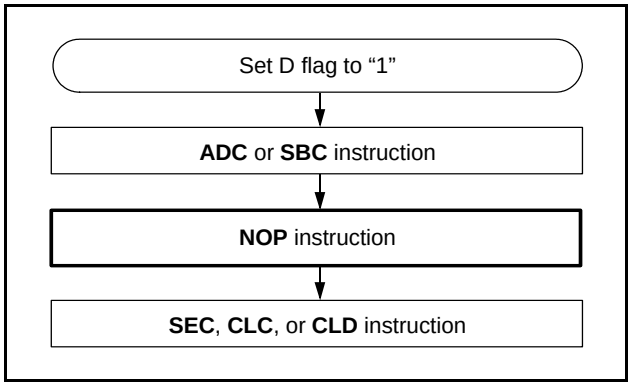


Fig 75. Execution of decimal calculations

(2) Notes on status flag in decimal mode

When decimal mode is selected, the values of three of the flags in the status register (the N, V, and Z flags) are invalid after a ADC or SBC instruction is executed.

The carry flag (C) is set to "1" if a carry is generated as a result of the calculation, or is cleared to "0" if a borrow is generated. To determine whether a calculation has generated a carry, the C flag must be initialized to "0" before each calculation. To check for a borrow, the C flag must be initialized to "1" before each calculation.

3. JMP instruction

When using the JMP instruction in indirect addressing mode, do not specify the last address on a page as an indirect address.

4. Multiplication and Division Instructions

- The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
- The execution of these instructions does not change the contents of the processor status register.

5. Read-Modify-Write Instruction

Do not execute any read-modify-write instruction to the read invalid (address) SFR.

The read-modify-write instruction reads 1-byte of data from memory, modifies the data, and writes 1-byte the data to the original memory.

In the 740 Family, the read-modify-write instructions are the following:

(1) Bit handling instructions:
CLB, SEB

(2) Shift and rotate instructions:
ASL, LSR, ROL, ROR, RRF

(3) Add and subtract instructions:
DEC, INC

(4) Logical operation instructions (1's complement):
COM

Although not the read-modify-write instructions, add and subtract/logical operation instructions (ADC, SBC, AND, EOR, and ORA) when T flag = "1" operate in the way as the read-modify-write instruction. Do not execute them to the read invalid SFR.

<Reason>

When the read-modify-write instruction is executed to the read invalid SFR, the following may result:

As reading is invalid, the read value is undefined. The instruction modifies this undefined value and writes it back, so the written value will be indeterminate.

6. Serial Interface

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the SRDY signal, set the transmit enable bit, the receive enable bit, and the SRDY output enable bit to "1".
Serial I/O1 continues to output the final bit from the TxD1 pin after transmission is completed. SOUT2 pin for serial I/O2 goes to high impedance after transfer is completed.
When in serial I/Os 1 and 3 (clock-synchronous mode) or in serial I/O2, an external clock is used as synchronous clock, write transmission data to the transmit buffer register or serial I/O2 register, during transfer clock is "H".

7. A/D Converter

The comparator uses capacitive coupling amplifier whose charge will be lost if the clock frequency is too low.
Therefore, make sure that f(XIN) in the middle/high-speed mode is at least on 500 kHz during an A/D conversion.
Do not execute the STP instruction during an A/D conversion.

8. D/A Converter

The accuracy of the D/A converter becomes rapidly poor under the VCC = 4.0 V or less condition; a supply voltage of VCC ≥ 4.0 V is recommended. When a D/A converter is not used, set all values of DAi conversion registers (i=1, 2) to "0016".

9. Instruction Execution Time

The instruction execution time is obtained by multiplying the period of the internal clock ϕ by the number of cycles needed to execute an instruction.
The number of cycles required to execute an instruction is shown in the list of machine instructions.
The period of the internal clock ϕ is double of the XIN period in high-speed mode.

10.Reserved Area, Reserved Bit

Do not write any data to the reserved area in the SFR area and the special page. (Do not change the contents after reset.)

11.CPU Mode Register

Be sure to fix bit 3 of the CPU mode register (address 003B16) to "1".

COUNTERMEASURES AGAINST NOISE

(1) Shortest wiring length

1. Wiring for $\overline{\text{RESET}}$ pin
   Make the length of wiring which is connected to the $\overline{\text{RESET}}$ pin as short as possible. Especially, connect a capacitor across the $\overline{\text{RESET}}$ pin and the VSS pin with the shortest possible wiring (within 20 mm).

• Reason
The width of a pulse input into the $\overline{\text{RESET}}$ pin is determined by the timing necessary conditions. If noise having a shorter pulse width than the standard is input to the $\overline{\text{RESET}}$ pin, the reset is released before the internal state of the microcomputer is completely initialized. This may cause a program runaway.

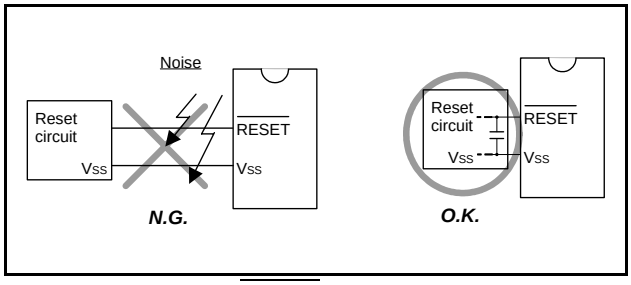


Fig. 76 Wiring for the $\overline{\text{RESET}}$ pin

2. Wiring for clock input/output pins
   - Make the length of wiring which is connected to clock I/O pins as short as possible.
   - Make the length of wiring (within 20 mm) across the grounding lead of a capacitor which is connected to an oscillator and the VSS pin of a microcomputer as short as possible.
   - Separate the VSS pattern only for oscillation from other VSS patterns.

• Reason
If noise enters clock I/O pins, clock waveforms may be deformed.
This may cause a program failure or program runaway. Also, if a potential difference is caused by the noise between the VSS level of a microcomputer and the VSS level of an oscillator, the correct clock will not be input in the microcomputer.

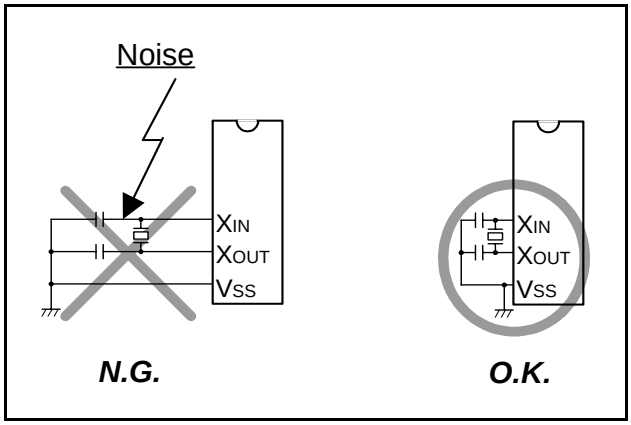


Fig. 77 Wiring for clock I/O pins

(2) Connection of bypass capacitor across VSS line and VCC line

In order to stabilize the system operation and avoid the latch-up, connect an approximately 0.1 µF bypass capacitor across the VSS line and the VCC line as follows:

- Connect a bypass capacitor across the VSS pin and the VCC pin at equal length.
- Connect a bypass capacitor across the VSS pin and the VCC pin with the shortest possible wiring.
- Use lines with a larger diameter than other signal lines for VSS line and VCC line.
- Connect the power source wiring via a bypass capacitor to the VSS pin and the VCC pin.

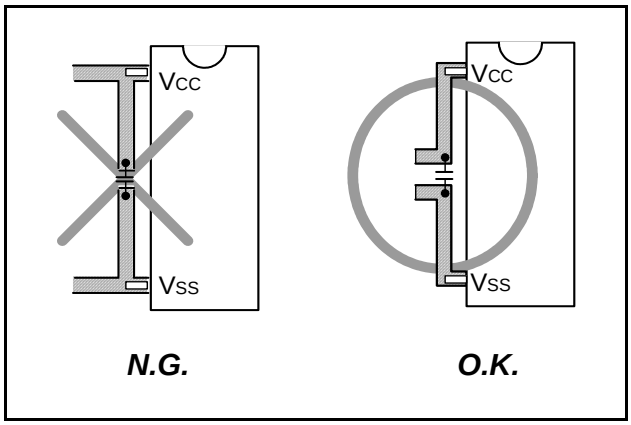


Fig. 78 Bypass capacitor across the VSS line and the VCC line

(3) Oscillator concerns

In order to obtain the stabilized operation clock on the user system and its condition, contact the oscillator manufacturer and select the oscillator and oscillation circuit constants. Be careful especially when range of voltage and temperature is wide.
Also, take care to prevent an oscillator that generates clocks for a microcomputer operation from being affected by other signals.

1. Keeping oscillator away from large current signal lines
   Install a microcomputer (and especially an oscillator) as far as possible from signal lines where a current larger than the tolerance of current value flows.

• Reason

In the system using a microcomputer, there are signal lines for controlling motors, LEDs, and thermal heads or others. When a large current flows through those signal lines, strong noise occurs because of mutual inductance.

2. Installing oscillator away from signal lines where potential levels change frequently
   Install an oscillator and a connecting pattern of an oscillator away from signal lines where potential levels change frequently. Also, do not cross such signal lines over the clock lines or the signal lines which are sensitive to noise.

• Reason

Signal lines where potential levels change frequently (such as the CNTR pin signal line) may affect other lines at signal rising edge or falling edge. If such lines cross over a clock line, clock waveforms may be deformed, which causes a microcomputer failure or a program runaway.

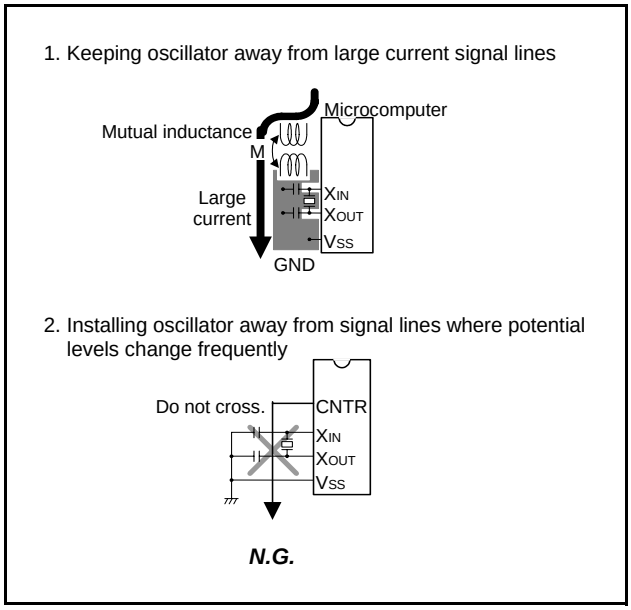


Fig. 79 Wiring for a large current signal line/Wiring of signal lines where potential levels change frequently

(4) Analog input

The analog input pin is connected to the capacitor of a voltage comparator. Accordingly, sufficient accuracy may not be obtained by the charge/discharge current at the time of A/D conversion when the analog signal source of high-impedance is connected to an analog input pin. In order to obtain the A/D conversion result stabilized more, please lower the impedance of an analog signal source, or add the smoothing capacitor to an analog input pin.

(5) Difference of memory size

When memory size differ in one group, actual values such as an electrical characteristics, A/D conversion accuracy, and the amount of proof of noise incorrect operation may differ from the ideal values.
When these products are used switching, perform system evaluation for each product of every after confirming product specification.

NOTES ON PERIPHERAL FUNCTIONS

Notes on Input and Output Ports

1. Use in Stand-By State

When using the MCU in stand-by state*1 for low-power consumption, do not leave the input level of an I/O port undefined. Be especially careful to the I/O ports for the N-channel open-drain.
In this case, pull-up (connect to Vcc) or pull-down (connect to Vss) these ports through a resistor.
When determining a resistance value, note the following:

- External circuit
- Variation in the output level during ordinary operation

When using a built-in pull-up resistor, note variations in current values:

- When setting as an input port: Fix the input level
- When setting as an output port: Prevent current from flowing out externally.

<Reason>
Even if a port is set to output by the direction register, when the content of the port latch is "1", the transistor becomes the OFF state, which allows the port to be in the high-impedance state. This may cause the level to be undefined depending on external circuits.
As described above, if the input level of an I/O port is left undefined, the power source current may flow because the potential applied to the input buffer in the MCU will be unstable.

*1 Stand-by state: Stop mode by executing the STP instruction
Wait mode by executing the WIT instruction

2. Modifying Output Data with Bit Handling Instruction

When the port latch of an I/O port is modified with the bit handling instruction*1, the value of an unspecified bit may change.
<Reason>
I/O ports can be set to input mode or output mode in byte units.
When the port register is read or written, the following will be operated:

- Port as input mode
  Read: Read the pin level
  Write: Write to the port latch
- Port as output mode
  Read: Read the port latch or peripheral function output (specifications vary depending on the port)
  Write: Write to the port latch (output the content of the port latch from the pin)

Meanwhile, the bit handling instructions are the read-modify-write instructions*2. Executing the bit handling instruction to the port register allows reading and writing a bit unspecified with the instruction at the same time.
If an unspecified bit is set to input mode, the pin level is read and the value is written to the port latch. At this time, if the original content of the port latch and the pin level do not match, the content of the port latch changes.
If an unspecified bit is set to output mode, the port latch is normally read, but the peripheral function output is read in some ports and the value is written to the port latch. At this time, if the original content of the port latch and the peripheral function output do not match, the content of the port latch changes.

*1 Bit handling instructions: CLB, SEB
*2 Read-modify-write instruction: Reads 1-byte of data from memory, modifies the data, and writes 1-byte of the data to the original memory.

3. Direction Registers

The values of the port direction registers cannot be read. This means, it is impossible to use the LDA instruction, memory operation instruction when the T flag is "1", addressing mode using direction register values as qualifiers, and bit test instructions such as BBC and BBS. It is also impossible to use bit operation instructions such as CLB and SEB, and read-modify-write instructions to direction registers, including calculations such as ROR. To set the direction registers, use instructions such as LDM or STA.

Termination of Unused Pins

1. Terminate unused pins

(1) Output ports: Open

(2) I/O ports:
Set the ports to input mode and connect each pin to VCC or VSS through a resistor of 1 k to 10 kΩ. An internal pull-up resistor can also be used for the port where the internal pull-up resister is selectable.
To set the ports to output mode, leave open at "L" or "H" output.

- When setting the ports to output mode and leave open, input mode in the initial state remains until the mode of the ports are switched to output mode by a program after a reset. This may cause the voltage level of the pins to be undefined and the power source current to increase while the ports remains in input mode. For any effects on the system, careful system evaluations should be implemented on the user side.
- The direction registers may be changed due to a program runaway or noise, so reset the registers periodically by a program to increase the program reliability.

(3) The AVSS pin when not using the A/D converter:

- When not using the A/D converter, handle a power source pin for the A/D converter, AVSS pin as follows:
  AVSS: Connect to the VSS pin.

2. Termination remarks

(1) When setting I/O ports to input mode
[1] Do not leave open
<Reason>

- The power source current may increase depending on the first-stage circuit.
- The ports are more likely affected by noise when compared with the termination shown on the above "1. (2) I/O ports"

[2] Do not connect to VCC or VSS directly
<Reason>
If the direction registers are changed to output mode due to a program runaway or noise, a short circuit may occur.

[3] Do not connect multiple ports in a lump to VCC or VSS through a resistor.
<Reason>
If the direction registers are changed to output mode due to a program runaway or noise, a short circuit may occur between the ports.

Notes on Interrupts

1. Change of relevant register settings

When the setting of the following registers or bits is changed, the interrupt request bit may be set to "1". When not requiring the interrupt occurrence synchronized with these setting, take the following sequence.

- Interrupt edge selection register (address 003A16)
- Timer XY mode register (address 002316)
- Timer Z mode register (address 002A16)

Set the above listed registers or bits as the following sequence.

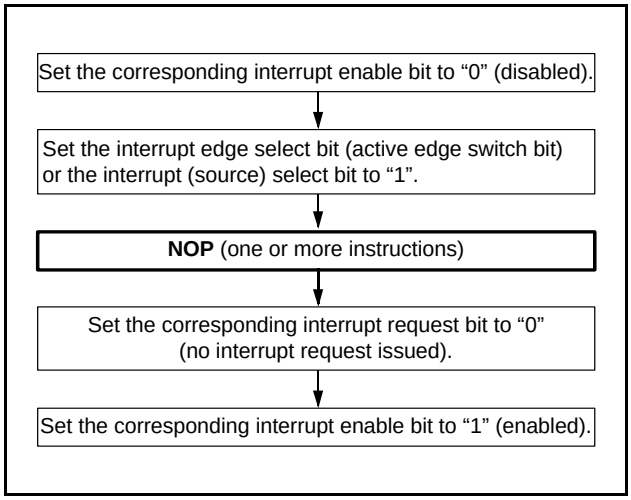


Fig 80. Sequence of changing relevant register

<Reason>
The interrupt request bit may be set to "1" in the following cases.

- When setting the external interrupt active edge
  Related bits:
  INT0 interrupt edge selection bit
  (bit 0 of interrupt edge selection register (address 003A16))
  INT1 interrupt edge selection bit
  (bit 1 of interrupt edge selection register (address 003A16))
  INT2 interrupt edge selection bit
  (bit 3 of interrupt edge selection register (address 003A16))
  INT3 interrupt edge selection bit
  (bit 4 of interrupt edge selection register (address 003A16))
  INT4 interrupt edge selection bit
  (bit 5 of interrupt edge selection register (address 003A16))
  CNTR0 activate edge switch bit
  (bit 2 of timer XY mode register (address 002316))
  CNTR1 activate edge switch bit
  (bits 6 of timer XY mode register (address 002316))
  CNTR2 activate edge switch bit
  (bits 5 of timer Z mode register (address 002A16))
- When switching the interrupt sources of an interrupt vector address where two or more interrupt sources are assigned
  Related bits:
  INT0, INT4 interrupt switch bit
  (bit 6 of interrupt edge selection register (address 003A16))
  INT0/Timer Z interrupt source selection bit
  (bit 0 of interrupt source selection register (address 003916))
  Serial I/O2/Timer Z interrupt source selection bit
  (bit 1 of interrupt source selection register (address 003916))
  INT4/CNTR2 interrupt source selection bit
  (bit 4 of interrupt source selection register (address 003916))
  CNTR1/Serial I/O3 receive interrupt source selection bit
  (bit 6 of interrupt source selection register (address 003916))
  AD conversion/Serial I/O3 transmit interrupt source selection bit
  (bit 6 of interrupt source selection register (address 003916))

2. Check of interrupt request bit

When executing the BBC or BBS instruction to an interrupt request bit of an interrupt request register immediately after this bit is set to "0", execute one or more instructions before executing the BBC or BBS instruction.

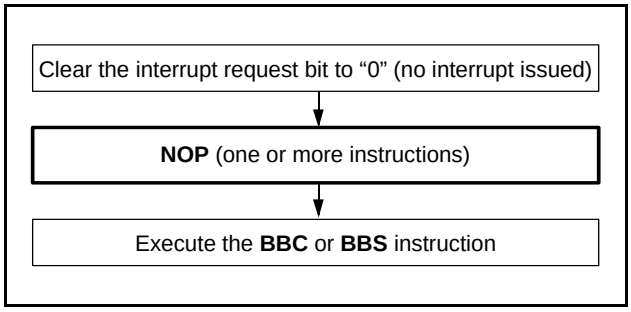


Fig 81. Sequence of check of interrupt request bit

<Reason>
If the BBC or BBS instruction is executed immediately after an interrupt request bit of an interrupt request register is cleared to "0", the value of the interrupt request bit before being cleared to "0" is read.

Notes on 8-bit Timer (timer 1, 2, X, Y)

- If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is 1/(n+1).
- When switching the count source by the timer 12, X and Y count source selection bits, the value of timer count is altered in unconsiderable amount owing to generating of thin pulses in the count input signals.
  Therefore, select the timer count source before set the value to the prescaler and the timer.
- Set the double-function port of the CNTR0/CNTR1 pin and port P54/P55 to output in the pulse output mode.
- Set the double-function port of CNTR0/CNTR1 pin and port P54/P55 to input in the event counter mode and the pulse width measurement mode.

Notes on 16-bit Timer (timer Z)

1. Pulse output mode

- Set the double-function port of the CNTR2 pin and port P47 to output.

2. Pulse period measurement mode

- Set the double-function port of the CNTR2 pin and port P47 to input.
- A read-out of timer value is impossible in this mode. The timer can be written to only during timer stop (no measurement of pulse period).
- Since the timer latch in this mode is specialized for the read-out of measured values, do not perform any write operation during measurement.
- "FFFF16" is set to the timer when the timer underflows or when the valid edge of measurement start/completion is detected.
  Consequently, the timer value at start of pulse period measurement depends on the timer value just before measurement start.

3. Pulse width measurement mode

- Set the double-function port of the CNTR2 pin and port P47 to input.
- A read-out of timer value is impossible in this mode. The timer can be written to only during timer stop (no measurement of pulse period).
- Since the timer latch in this mode is specialized for the read-out of measured values, do not perform any write operation during measurement.
- "FFFF16" is set to the timer when the timer underflows or when the valid edge of measurement start/completion is detected.
  Consequently, the timer value at start of pulse width measurement depends on the timer value just before measurement start.

4. Programmable waveform generating mode

- Set the double-function port of the CNTR2 pin and port P47 to output.

5. Programmable one-shot generating mode

- Set the double-function port of CNTR2 pin and port P47 to output, and of INT1 pin and port P42 to input in this mode.
- This mode cannot be used in low-speed mode.
- If the value of the CNTR2 active edge switch bit is changed during one-shot generating enabled or generating one-shot pulse, then the output level from CNTR2 pin changes.

6. All modes

- Timer Z write control

Which write control can be selected by the timer Z write control bit (bit 3) of the timer Z mode register (address 002A16), writing data to both the latch and the timer at the same time or writing data only to the latch.
When the operation "writing data only to the latch" is selected, the value is set to the timer latch by writing data to the address of timer Z and the timer is updated at next underflow. After reset release, the operation "writing data to both the latch and the timer at the same time" is selected, and the value is set to both the latch and the timer at the same time by writing data to the address of timer Z.
In the case of writing data only to the latch, if writing data to the latch and an underflow are performed almost at the same time, the timer value may become undefined.

- Timer Z read control

A read-out of timer value is impossible in pulse period measurement mode and pulse width measurement mode. In the other modes, a read-out of timer value is possible regardless of count operating or stopped.
However, a read-out of timer latch value is impossible.

- Switch of interrupt active edge of CNTR2 and INT1

Each interrupt active edge depends on setting of the CNTR2 active edge switch bit and the INT1 active edge selection bit.

- Switch of count source

When switching the count source by the timer Z count source selection bits, the value of timer count is altered in inconsiderable amount owing to generating of thin pulses on the count input signals.
Therefore, select the timer count source before setting the value to the prescaler and the timer.

Notes on Serial Interface

1. Notes when selecting clock synchronous serial I/O

(1) Stop of transmission operation

As for serial I/Oi (i = 1, 3) that can be used as either a clock synchronous or an asynchronous (UART) serial I/O, clear the serial I/Oi enable bit and the transmit enable bit to "0" (serial I/Oi and transmit disabled).
<Reason>
Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/Oi enable bit is cleared to "0" (serial I/Oi disabled), the internal transmission is running (in this case, since pins TxDi, RxDi, SCLKi, and SRDYi function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register i in this state, data starts to be shifted to the transmit shift register i. When the serial I/Oi enable bit is set to "1" at this time, the data during internally shifting is output to the TxDi pin and an operation failure occurs.

(2) Stop of receive operation

As for serial I/Oi (i = 1, 3) that can be used as either a clock synchronous or an asynchronous (UART) serial I/O, clear the receive enable bit to "0" (receive disabled), or clear the serial I/Oi enable bit to "0" (serial I/Oi disabled).

(3) Stop of transmit/receive operation

As for serial I/Oi (i = 1, 3) that can be used as either a clock synchronous or an asynchronous (UART) serial I/O, clear both the transmit enable bit and receive enable bit to "0" (transmit and receive disabled).
(when data is transmitted and received in the clock synchronous serial I/O mode, any one of data transmission and reception cannot be stopped.)
<Reason>
In the clock synchronous serial I/O mode, the same clock is used for transmission and reception. If any one of transmission and reception is disabled, a bit error occurs because transmission and reception cannot be synchronized.
In this mode, the clock circuit of the transmission circuit also operates for data reception. Accordingly, the transmission circuit does not stop by clearing only the transmit enable bit to "0" (transmit disabled). Also, the transmission circuit is not initialized by clearing the serial I/Oi enable bit to "0" (serial I/Oi disabled) (refer to (1) in 1.).

2. Notes when selecting clock asynchronous serial I/O

(1) Stop of transmission operation

Clear the transmit enable bit to "0" (transmit disabled). The transmission operation does not stop by clearing the serial I/Oi enable bit (i = 1, 3) to "0".

<Reason>

This is the same as (1) in 1.

(2) Stop of receive operation

Clear the receive enable bit to "0" (receive disabled).

(3) Stop of transmit/receive operation

Only transmission operation is stopped.

Clear the transmit enable bit to "0" (transmit disabled). The transmission operation does not stop by clearing the serial I/Oi enable bit (i = 1, 3) to "0".

<Reason>

This is the same as (1) in 1.

Only receive operation is stopped.

Clear the receive enable bit to "0" (receive disabled).

3. $\overline{\text{SRDY}}$i (i = 1, 3) output of reception side

When signals are output from the $\overline{\text{SRDY}}$i pin on the reception side by using an external clock in the clock synchronous serial I/O mode, set all of the receive enable bit, the $\overline{\text{SRDY}}$i output enable bit, and the transmit enable bit to "1" (transmit enabled).

4. Setting serial I/Oi (i = 1, 3) control register again

Set the serial I/Oi control register again after the transmission and the reception circuits are reset by clearing both the transmit enable bit and the receive enable bit to "0."

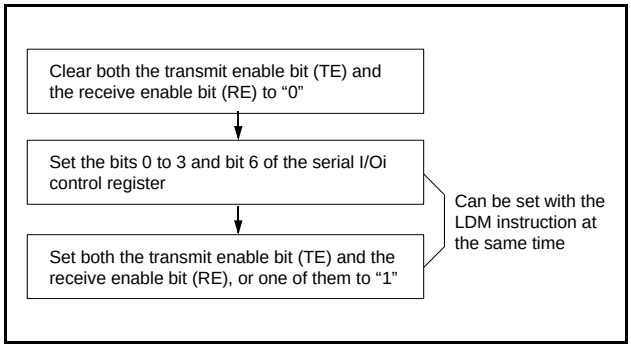


Fig 82. Sequence of setting serial I/Oi (i = 1, 3) control register again

5. Data transmission control with referring to transmit shift register completion flag

After the transmit data is written to the transmit buffer register, the transmit shift register completion flag changes from "1" to "0" with a delay of 0.5 to 1.5 shift clocks. When data transmission is controlled with referring to the flag after writing the data to the transmit buffer register, note the delay.

6. Transmission control when external clock is selected

When an external clock is used as the synchronous clock for data transmission, set the transmit enable bit to "1" at "H" of the SCLKi (i = 1, 3) input level. Also, write the transmit data to the transmit buffer register at "H" of the SCLKi input level.

7. Transmit interrupt request when transmit enable bit is set

When using the transmit interrupt, take the following sequence.

(1) Set the serial I/Oi transmit interrupt enable bit (i = 1, 3) to "0" (disabled).

(2) Set the transmit enable bit to "1".

(3) Set the serial I/Oi transmit interrupt request bit (i = 1, 3) to "0" after 1 or more instruction has executed.

(4) Set the serial I/Oi transmit interrupt enable bit (i = 1, 3) to "1" (enabled).

<Reason>

When the transmission enable bit is set to "1", the transmit buffer empty flag and transmit shift register shift completion flag are also set to "1".

Therefore, regardless of selecting which timing for the generating of transmit interrupts, the interrupt request is generated and the transmit interrupt request bit is set at this point.

8. Writing to baud rate generator i (BRGi) (i = 1, 3)

Write data to the baud rate generator i (BRGi) (i = 1, 3) while the transmission/reception operation is stopped.

Notes on PWM

The PWM starts from "H" level after the PWM enable bit is set to enable and "L" level is temporarily output from the PWM pin. The length of this "L" level output is as follows:

$$\frac{n+1}{2 \times f(X_{IN})} \quad (s) \quad \text{(Count source selection bit = "0", where n is the value set in the prescaler)}$$

$$\frac{n+1}{f(X_{IN})} \quad (s) \quad \text{(Count source selection bit = "1", where n is the value set in the prescaler)}$$

Notes on A/D Converter

1. Analog input pin

Make the signal source impedance for analog input low, or equip an analog input pin with an external capacitor of 0.01 μF to 1 μF. Further, be sure to verify the operation of application products on the user side.

<Reason>

An analog input pin includes the capacitor for analog voltage comparison. Accordingly, when signals from signal source with high impedance are input to an analog input pin, charge and discharge noise generates. This may cause the A/D conversion precision to be worse.

2. A/D converter power source pin

The AVSS pin is A/D converter power source pins. Regardless of using the A/D conversion function or not, connect it as following:

- AVSS: Connect to the VSS line

<Reason>

If the AVSS pin is opened, the microcomputer may have a failure because of noise or others.

3. Clock frequency during A/D conversion

The comparator consists of a capacity coupling, and a charge of the capacity will be lost if the clock frequency is too low. Thus, make sure the following during an A/D conversion.

- f(XIN) is 500 kHz or more
- Do not execute the STP instruction

4. Difference between at 8-bit reading in 10-bit A/D mode and at 8-bit A/D mode

At 8-bit reading in the 10-bit A/D mode, "–1/2 LSB" correction is not performed to the A/D conversion result.
In the 8-bit A/D mode, the A/D conversion characteristics is the same as 3802 group's characteristics because "–1/2 LSB" correction is performed.

Notes on D/A Converter

1. VCC when using D/A converter

The D/A converter accuracy when VCC is 4.0 V or less differs from that of when VCC is 4.0 V or more. When using the D/A converter, we recommend using a VCC of 4.0 V or more.

2. D/Ai conversion register when not using D/A converter

When a D/A converter is not used, set all values of the D/Ai conversion registers (i = 1, 2) to "00$_{16}$". The initial value after reset is "00$_{16}$".

Notes on Watchdog Timer

- Make sure that the watchdog timer H does not underflow while waiting Stop release, because the watchdog timer keeps counting during that term.
- When the STP instruction function selection bit has been set to "1", it is impossible to switch it to "0" by a program.

Notes on $\overline{\text{RESET}}$ Pin

Connecting capacitor
In case where the $\overline{\text{RESET}}$ signal rise time is long, connect a ceramic capacitor or others across the $\overline{\text{RESET}}$ pin and the VSS pin.
Use a 1000 pF or more capacitor for high frequency use. When connecting the capacitor, note the following:

- Make the length of the wiring which is connected to a capacitor as short as possible.
- Be sure to verify the operation of application products on the user side.

<Reason>
If the several nanosecond or several ten nanosecond impulse noise enters the $\overline{\text{RESET}}$ pin, it may cause a microcomputer failure.

Notes on Low-speed Operation Mode

1. Using sub-clock

To use a sub-clock, fix bit 3 of the CPU mode register to "1" or control the Rd (refer to Figure 83) resistance value to a certain level to stabilize an oscillation. For resistance value of Rd, consult the oscillator manufacturer.

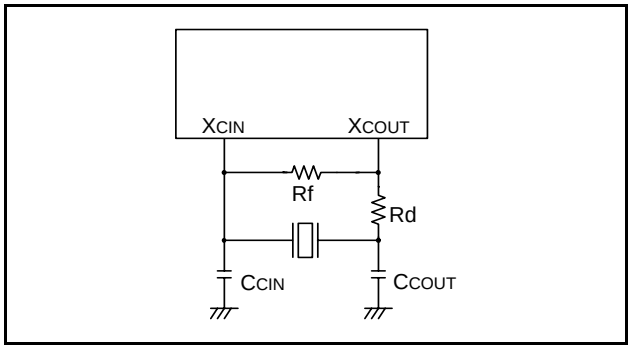


Fig 83. Ceramic resonator circuit

<Reason>
When bit 3 of the CPU mode register is set to "0", the sub-clock oscillation may stop.

2. Switch between middle/high-speed mode and low-speed mode

If you switch the mode between middle/high-speed and low-speed, stabilize both XIN and XCIN oscillations. The sufficient time is required for the sub clock to stabilize, especially immediately after power on and at returning from stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency on condition that f(XIN) > 3×f(XCIN).

Quartz-Crystal Oscillator

When using the quartz-crystal oscillator of high frequency, such as 16 MHz etc., it may be necessary to select a specific oscillator with the specification demanded.

Notes on Restarting Oscillation

- Restarting oscillation

Usually, when the MCU stops the clock oscillation by STP instruction and the STP instruction has been released by an external interrupt source, the fixed values of Timer 1 and Prescaler 12 (Timer 1 = "01$_{16}$", Prescaler 12 = "FF$_{16}$") are automatically reloaded in order for the oscillation to stabilize. The user can inhibit the automatic setting by writing "1" to bit 0 of MISRG (address 0010$_{16}$).
However, by setting this bit to "1", the previous values, set just before the STP instruction was executed, will remain in Timer 1 and Prescaler 12. Therefore, you will need to set an appropriate value to each register, in accordance with the oscillation stabilizing time, before executing the STP instruction.
<Reason>
Oscillation will restart when an external interrupt is received. However, internal clock ϕ is supplied to the CPU only when Timer 1 starts to underflow. This ensures time for the clock oscillation using the ceramic resonators to be stabilized.

Notes on Using Stop Mode

• Register setting

Since values of the prescaler 12 and Timer 1 are automatically reloaded when returning from the stop mode, set them again, respectively. (When the oscillation stabilizing time set after STP instruction released bit is "0")

• Clock restoration

After restoration from the stop mode to the normal mode by an interrupt request, the contents of the CPU mode register previous to the STP instruction execution are retained. Accordingly, if both main clock and sub clock were oscillating before execution of the STP instruction, the oscillation of both clocks is resumed at restoration.

In the above case, when the main clock side is set as a system clock, the oscillation stabilizing time for approximately 8,000 cycles of the XIN input is reserved at restoration from the stop mode. At this time, note that the oscillation on the sub clock side may not be stabilized even after the lapse of the oscillation stabilizing time of the main clock side.

Notes on Wait Mode

• Clock restoration

If the wait mode is released by a reset when XCIN is set as the system clock and XIN oscillation is stopped during execution of the WIT instruction, XCIN oscillation stops, XIN oscillations starts, and XIN is set as the system clock.

In the above case, the $\overline{\text{RESET}}$ pin should be held at "L" until the oscillation is stabilized.

Notes on Handling of Power Source Pins

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (VCC pin) and GND pin (VSS pin), and between power source pin (VCC pin) and analog power source input pin (AVSS pin). Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic capacitor of 0.01 μF–0.1 μF is recommended.

Notes on Power Source Voltage

When the power source voltage value of a microcomputer is less than the value which is indicated as the recommended operating conditions, the microcomputer does not operate normally and may perform unstable operation.

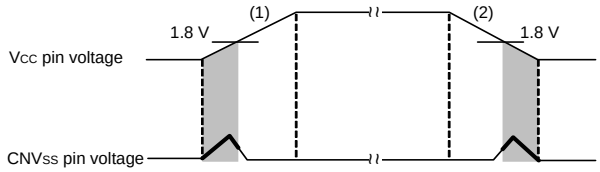
In a system where the power source voltage drops slowly when the power source voltage drops or the power supply is turned off, reset a microcomputer when the power source voltage is less than the recommended operating conditions and design a system not to cause errors to the system by this unstable operation.

Notes on Product Shipped in Blank

As for the product shipped in blank, Renesas does not perform the writing test to user ROM area after the assembly process though the QzROM writing test is performed enough before the assembly process. Therefore, a writing error of approx.0.1 % may occur. Moreover, please note the contact of cables and foreign bodies on a socket, etc. because a writing environment may cause some writing errors.

Precautions Regarding Overvoltage in QzROM Version

Make sure that voltage exceeding the VCC pin voltage is not applied to other pins. In particular, ensure that the state indicated by bold lines in figure below does not occur for CNVSS pin (VPP power source pin for QzROM) during power-on or power-off. Otherwise the contents of QzROM could be rewritten.



(1) The input voltage to other MCU pins rises before the VCC pin voltage rises.
(2) The input voltage to other MCU pins falls before the VCC pin voltage falls.
Note: If VCC falls below the minimum value 1.8 V (shaded areas), the internal circuit becomes unstable. Take additional care to prevent overvoltage.

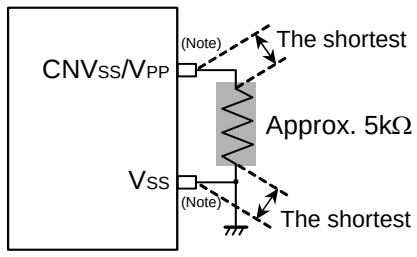
Fig 84. Timing Diagram (bold-lined periods are applicable)

Notes on QzROM Version

Connect the CNVSS/VPP pin the shortest possible to the GND pattern which is supplied to the VSS pin of the microcomputer. In addition connecting an approximately 5 kΩ resistor in series to the GND could improve noise immunity. In this case as well as the above mention, connect the pin the shortest possible to the GND pattern which is supplied to the VSS pin of the microcomputer.

• Reason

The CNVSS/VPP pin is the power source input pin for the built-in QzROM. When programming in the QzROM, the impedance of the VPP pin is low to allow the electric current for writing to flow into the built-in QzROM. Because of this, noise can enter easily. If noise enters the VPP pin, abnormal instruction codes or data are read from the QzROM, which may cause a program runaway.



Note. Shows the microcomputer's pin.

Fig 85. Wiring for the CNVSS/VPP

Notes On QzROM Writing Orders

When ordering the QzROM product shipped after writing, submit the mask file (extension: .msk) which is made by the mask file converter MM.

- Be sure to set the ROM option data* setup when making the mask file by using the mask file converter MM. The ROM code protect is specified according to the ROM option data* in the mask file which is submitted at ordering. Note that the mask file which has nothing at the ROM option data* or has the data other than "00_{16}", "FE_{16}" and "FF_{16}" can not be accepted.
- Set "FF_{16}" to the ROM code protect address in ROM data regardless of the presence or absence of a protect. When data other than "FF_{16}" is set, we may ask that the ROM data be submitted again.

* ROM option data: mask option noted in MM

Data Required for QzROM Writing Orders

The following are necessary when ordering a QzROM product shipped after writing:

1. QzROM Writing Confirmation Form*
2. Mark Specification Form*
3. ROM data.....Mask file

* For the QzROM writing confirmation form and the mark specification form, refer to the "Renesas Technology Corp." Homepage (http://www.renesas.com/homepage.jsp).
Note that we cannot deal with special font marking (customer's trademark etc.) in QzROM microcomputer.

QzROM Receive Flow

When writing to QzROM is performed by user side, the receiving inspection by the following flow is necessary.

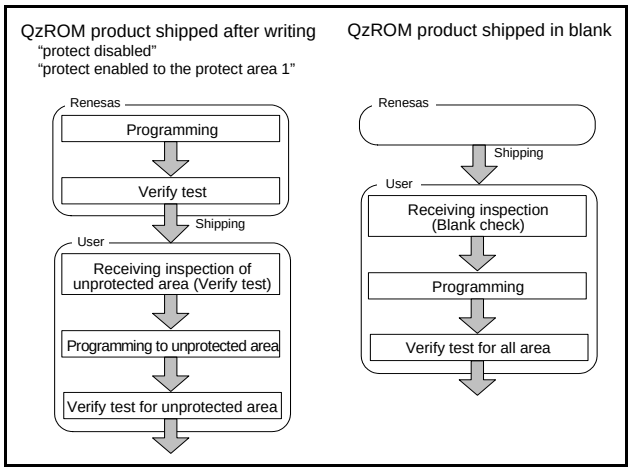


Fig. 86 QzROM receive flow

ELECTRICAL CHARACTERISTICS

Absolute maximum ratings

Table 10 Absolute maximum ratings

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Power source voltages		All voltages are based on V_{SS}. When an input voltage is measured, output transistors are cut off.	–0.3 to 6.5	V
V_I	Input voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$, $P3_1$, $P3_4$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, V_{REF}		–0.3 to V_{CC} + 0.3	V
V_I	Input voltage	$P3_2$, $P3_3$		–0.3 to 5.8	V
V_I	Input voltage	$\overline{RESET}$, X_{IN}		–0.3 to V_{CC} + 0.3	V
V_I	Input voltage	CNV_{SS}		–0.3 to 8.0	V
V_O	Output voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$, $P3_1$, $P3_4$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, X_{OUT}		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage	$P3_2$, $P3_3$		–0.3 to 5.8	V
P_d	Power dissipation		Ta=25 °C	1000(1)	mW
T_{opr}	Operating temperature		–	–20 to 85	°C
T_{stg}	Storage temperature		–	–65 to 125	°C

NOTES:
1. This value is 300 mW except SP package.

Recommended operating conditions

Table 11 Recommended operating conditions (1)
(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{CC}	Power source voltage(1)	When start oscillating(2)		2.2	5.0	5.5	V
		High-speed mode $f(\phi) = f(X_{IN})/2$	$f(X_{IN}) \le 2.1$ MHz	2.0	5.0	5.5	V
			$f(X_{IN}) \le 4.2$ MHz	2.2	5.0	5.5	
			$f(X_{IN}) \le 8.4$ MHz	2.7	5.0	5.5	
			$f(X_{IN}) \le 12.5$ MHz	4.0	5.0	5.5	
			$f(X_{IN}) \le 16.8$ MHz	4.5	5.0	5.5	
		Middle-speed mode $f(\phi) = f(X_{IN})/8$	$f(X_{IN}) \le 6.3$ MHz	1.8	5.0	5.5	V
			$f(X_{IN}) \le 8.4$ MHz	2.2	5.0	5.5	
			$f(X_{IN}) \le 12.5$ MHz	2.7	5.0	5.5	
			$f(X_{IN}) \le 16.8$ MHz	4.5	5.0	5.5	
V_{SS}	Power source voltage				0		V
V_{IH}	"H" input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$, $P3_1$, $P3_4$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	$1.8 \le V_{CC} < 2.7$ V		0.85 V_{CC}		V_{CC}	V
		$2.7 \le V_{CC} \le 5.5$ V		0.8 V_{CC}		V_{CC}	
V_{IH}	"H" input voltage $P3_2$, $P3_3$	$1.8 \le V_{CC} < 2.7$ V		0.85 V_{CC}		5.5	V
		$2.7 \le V_{CC} \le 5.5$ V		0.8 V_{CC}		5.5	
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}, X_{CIN}, CNV_{SS}	$1.8 \le V_{CC} < 2.7$ V		0.85 V_{CC}		V_{CC}	V
		$2.7 \le V_{CC} \le 5.5$ V		0.8 V_{CC}		V_{CC}	
V_{IL}	"L" input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	$1.8 \le V_{CC} < 2.7$ V		0		0.16 V_{CC}	V
		$2.7 \le V_{CC} \le 5.5$ V		0		0.2 V_{CC}	
V_{IL}	"L" input voltage $\overline{RESET}$, CNV_{SS}	$1.8 \le V_{CC} < 2.7$ V		0		0.16 V_{CC}	V
		$2.7 \le V_{CC} \le 5.5$ V		0		0.2 V_{CC}	
V_{IL}	"L" input voltage X_{IN}, X_{CIN}	$1.8 \le V_{CC} \le 5.5$ V		0		0.16 V_{CC}	V
$f(X_{IN})$	Main clock input oscillation frequency(3)	High-speed mode $f(\phi) = f(X_{IN})/2$	$2.0 \le V_{CC} < 2.2$ V			$\frac{(20 \times V_{CC} - 36) \times 1.05}{2}$	MHz
			$2.2 \le V_{CC} < 2.7$ V			$\frac{(24 \times V_{CC} - 40.8) \times 1.05}{3}$	MHz
			$2.7 \le V_{CC} < 4.0$ V			$\frac{(9 \times V_{CC} - 0.3) \times 1.05}{3}$	MHz
			$4.0 \le V_{CC} < 4.5$ V			$\frac{(24 \times V_{CC} - 60) \times 1.05}{3}$	MHz
			$4.5 \le V_{CC} \le 5.5$ V			16.8	MHz
		Middle-speed mode $f(\phi) = f(X_{IN})/8$	$1.8 \le V_{CC} < 2.2$ V			$\frac{(15 \times V_{CC} - 9) \times 1.05}{3}$	MHz
			$2.2 \le V_{CC} < 2.7$ V			$\frac{(24 \times V_{CC} - 28.8) \times 1.05}{3}$	MHz
			$2.7 \le V_{CC} < 4.5$ V			$\frac{(15 \times V_{CC} + 39) \times 1.1}{7}$	MHz
			$4.5 \le V_{CC} \le 5.5$ V			16.8	MHz
$f(X_{CIN})$	Sub-clock input oscillation frequency(3, 4)				32.768	50	kHz

NOTES:
1. When using A/D converter, see A/D converter recommended operating conditions.
2. The start voltage and the start time for oscillation depend on the using oscillator, oscillation circuit constant value and operating temperature range, etc.. Particularly a high-frequency oscillator might require some notes in the low voltage operation.
3. When the oscillation frequency has a duty cycle of 50%.
4. When using the microcomputer in low-speed mode, set the sub-clock input oscillation frequency on condition that $f(X_{CIN}) < f(X_{IN})/3$.

Table 12 Recommended operating conditions (2)
(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$\Sigma I_{OH(peak)}$	"H" total peak output current(1)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$, $P3_1$, $P3_4$-$P3_7$			–80	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current(1)	$P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			–80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current(1)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P3_0$-$P3_7$			80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current(1)	$P2_0$-$P2_7$			80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current(1)	$P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			80	mA
$\Sigma I_{OH(avg)}$	"H" total average output current(1)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$, $P3_1$, $P3_4$-$P3_7$			–40	mA
$\Sigma I_{OH(avg)}$	"H" total average output current(1)	$P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			–40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current(1)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P3_0$-$P3_7$			40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current(1)	$P2_0$-$P2_7$			40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current(1)	$P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			40	mA
$I_{OH(peak)}$	"H" peak output current(2)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$, $P3_1$, $P3_4$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			–10	mA
$I_{OL(peak)}$	"L" peak output current(2)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			10	mA
$I_{OL(peak)}$	"L" peak output current(2)	$P2_0$-$P2_7$			20	mA
$I_{OH(avg)}$	"H" average output current(3)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$, $P3_1$, $P3_4$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			–5	mA
$I_{OL(avg)}$	"L" average output current(3)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			5	mA
$I_{OL(avg)}$	"L" average output current(3)	$P2_0$-$P2_7$			10	mA

NOTES:
1. The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.
2. The peak output current is the peak current flowing in each port.
3. The average output current I_{OL}(avg), I_{OH}(avg) are average value measured over 100 ms.

Electrical characteristics

Table 13 Electrical characteristics (1)
(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage(1) $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$, $P3_1$, $P3_4$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	I_{OH} = –10 mA V_{CC} = 4.0 to 5.5 V	V_{CC} – 2.0			V
		I_{OH} = –1.0 mA V_{CC} = 1.8 to 5.5 V	V_{CC} – 1.0			
V_{OL}	"L" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	I_{OL} = 10 mA V_{CC} = 4.0 to 5.5 V			2.0	V
		I_{OL} = 1.6 mA V_{CC} = 1.8 to 5.5 V			1.0	
V_{OL}	"L" output voltage $P2_0$-$P2_7$	I_{OL} = 20 mA V_{CC} = 4.0 to 5.5 V			2.0	V
		I_{OL} = 1.6 mA V_{CC} = 1.8 to 5.5 V			0.4	
$V_{T+} - V_{T-}$	Hysteresis $CNTR_0$, $CNTR_1$, $CNTR_2$, INT_0-INT_4			0.4		V
$V_{T+} - V_{T-}$	Hysteresis RxD_1, $SCLK_1$, SIN_2, $SCLK_2$, RxD_3, $SCLK_3$			0.5		V
$V_{T+} - V_{T-}$	Hysteresis $\overline{RESET}$			0.5		V
I_{IH}	"H" input current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	V_I = V_{CC} (Pin floating, Pull-up transistor "off")			5.0	µA
I_{IH}	"H" input current $\overline{RESET}$, CNV_{SS}	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current X_{IN}	V_I = V_{CC}		4.0		µA
I_{IL}	"L" input current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	V_I = V_{SS} (Pin floating, Pull-up transistor "off")			–5.0	µA
I_{IL}	"L" input current $\overline{RESET}$, CNV_{SS}	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current X_{IN}	V_I = V_{SS}		–4.0		µA
I_{IL}	"L" input current (at Pull-up) $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$, $P3_1$, $P3_4$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	V_I = V_{SS} V_{CC} = 5.0 V	–80	–210	–420	µA
		V_I = V_{SS} V_{CC} = 3.0 V	–30	–70	–140	
V_{RAM}	RAM hold voltage	When clock stopped	1.8		V_{CC}	V

NOTES:
1. $P3_5$ is measured when the $P3_5/TxD_3$ P-channel output disable bit of the UART3 control register (bit 4 of address 0033_{16}) is "0".
$P4_5$ is measured when the $P4_5/TxD_1$ P-channel output disable bit of the UART1 control register (bit 4 of address $001B_{16}$) is "0".

Table 14 Electrical characteristics (2)
(V_{CC} = 1.8 to 5.5 V, Ta = –20 to 85 °C, f(X_{CIN})=32.768kHz (Stopped in middle-speed mode), Output transistors “off”, AD converter not operated)

Symbol	Parameter	Test conditions			Limits			Unit
					Min.	Typ.	Max.	
I_{CC}	Power source current	High-speed mode	V_{CC} = 5.0 V	f(X_{IN}) = 16.8 MHz		8.0	15.0	mA
				f(X_{IN}) = 12.5 MHz		6.5	12.0	
				f(X_{IN}) = 8.4 MHz		5.0	9.0	
				f(X_{IN}) = 4.2 MHz		2.5	5.0	
				f(X_{IN}) = 16.8 MHz (in WIT state)		2.0	3.6	
			V_{CC} = 3.0 V	f(X_{IN}) = 8.4 MHz		1.9	3.8	mA
				f(X_{IN}) = 4.2 MHz		1.0	2.0	
				f(X_{IN}) = 2.1 MHz		0.6	1.2	
		Middle-speed mode	V_{CC} = 5.0 V	f(X_{IN}) = 16.8 MHz		4.0	7.0	mA
				f(X_{IN}) = 12.5 MHz		3.0	6.0	
				f(X_{IN}) = 8.4 MHz		2.5	5.0	
				f(X_{IN}) = 16.8 MHz (in WIT state)		1.8	3.3	
			V_{CC} = 3.0 V	f(X_{IN}) = 12.5 MHz		1.5	3.0	mA
				f(X_{IN}) = 8.4 MHz		1.2	2.4	
				f(X_{IN}) = 6.3 MHz		1.0	2.0	
		Low-speed mode	V_{CC} = 5.0 V	f(X_{IN}) = stopped		55	200	µA
				In WIT state		40	70	
			V_{CC} = 3.0 V	f(X_{IN}) = stopped		15	40	µA
				In WIT state		8	15	
			V_{CC} = 2.0 V	f(X_{IN}) = stopped		6	15	µA
				In WIT state		3	6	
		In STP state (All oscillation stopped)		Ta = 25 °C		0.1	1.0	µA
				Ta = 85 °C			10	
		Increment when A/D conversion is executed		f(X_{IN}) = 16.8 MHz, V_{CC} = 5.0 V In Middle-, high-speed mode		500		µA

A/D converter characteristics

Table 15 A/D converter recommended operating conditions
(V_{CC} = 2.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage (When A/D converter is used)	8-bit A/D mode(1)	2.0	5.0	5.5	V
		10-bit A/D mode(2)	2.2	5.0	5.5	
V_{REF}	Analog convert reference voltage		2.0		V_{CC}	V
AV_{SS}	Analog power source voltage			0		V
V_{IA}	Analog input voltage AN_0-AN_{15}		0		V_{CC}	V
f(X_{IN})	Main clock input oscillation frequency (When A/D converter is used)	2.0 ≤ V_{CC} = V_{REF} < 2.2 V	0.5		$\frac{(20 \times V_{CC} - 36) \times 1.05}{2}$	MHz
		2.2 ≤ V_{CC} = V_{REF} < 2.7 V	0.5		$\frac{(24 \times V_{CC} - 40.8) \times 1.05}{3}$	
		2.7 ≤ V_{CC} = V_{REF} < 4.0 V	0.5		$\frac{(9 \times V_{CC} - 0.3) \times 1.05}{3}$	
		4.0 ≤ V_{CC} = V_{REF} < 4.5 V	0.5		$\frac{(24.6 \times V_{CC} - 62.7) \times 1.05}{3}$	
		4.5 ≤ V_{CC} = V_{REF} ≤ 5.5 V	0.5		16.8	

NOTES:
1. 8-bit A/D mode: When the conversion mode selection bit (bit 7 of address 0038_{16}) is “1”.
2. 10-bit A/D mode: When the conversion mode selection bit (bit 7 of address 0038_{16}) is “0”.

Table 16 A/D converter characteristics
(V_{CC} = 2.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min.	Typ.	Max.	
–	Resolution		8-bit A/D mode(1)				8	bit
			10-bit A/D mode(2)				10	
–	Absolute accuracy (excluding quantization error)		8-bit A/D mode(1)	2.0 ≤ V_{REF} < 2.2 V			±3	LSB
				2.2 ≤ V_{REF} ≤ 5.5 V			±2	
			10-bit A/D mode(2)	2.2 ≤ V_{REF} < 2.7 V			±5	LSB
				2.7 ≤ V_{REF} ≤ 5.5 V			±4	
t_{CONV}	Conversion time		8-bit A/D mode(1)				50	2tc(X_{IN})
			10-bit A/D mode(2)				61	
R_{LADDER}	Ladder resistor				12	35	100	kΩ
I_{VREF}	Reference power source input current	at A/D converter operated	V_{REF} = 5.0 V		50	150	200	µA
		at A/D converter stopped	V_{REF} = 5.0 V				5.0	µA
$I_{I(AD)}$	A/D port input current						5.0	µA

NOTES:
1. 8-bit A/D mode: When the conversion mode selection bit (bit 7 of address 0038_{16}) is “1”.
2. 10-bit A/D mode: When the conversion mode selection bit (bit 7 of address 0038_{16}) is “0”.

D/A converter characteristics

Table 17 D/A converter characteristics
(V_{CC} = 2.7 to 5.5 V, V_{REF} = 2.7 V to V_{CC}, V_{SS} = AV_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
–	Resolution				8	bit
–	Absolute accuracy	4.0 ≤ V_{REF} ≤ 5.5 V			1.0	%
		2.7 ≤ V_{REF} < 4.0 V			2.5	
tsu	Setting time				3	µs
RO	Output resistor		2	3.5	5	kΩ
I_{VREF}	Reference power source input current(1)				3.2	mA

NOTES:
1. Using one D/A converter, with the value in the other DAi conversion register (i=1, 2) being “00_{16}”.

Timing requirements and switching characteristics

Table 18 Timing requirements (1)
(V_{CC} = 2.0 to 5.5 V, V_{SS} = 0V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$t_W(\overline{RESET})$	Reset input “L” pulse width		16			X_{IN} cycle
$t_C(X_{IN})$	Main clock X_{IN} input cycle time	4.5 ≤ V_{CC} ≤ 5.5 V	59.5			ns
		4.0 ≤ V_{CC} < 4.5 V	10000/(86 V_{CC} – 219)			
		2.7 ≤ V_{CC} < 4.0 V	26 × 10^3/(82 V_{CC} - 3)			
		2.2 ≤ V_{CC} < 2.7 V	10000/(84 V_{CC} – 143)			
		2.0 ≤ V_{CC} < 2.2 V	10000/(105 V_{CC} – 189)			
$t_{WH}(X_{IN})$	Main clock X_{IN} input “H” pulse width	4.5 ≤ V_{CC} ≤ 5.5 V	25			ns
		4.0 ≤ V_{CC} < 4.5 V	4000/(86 V_{CC} – 219)			
		2.7 ≤ V_{CC} < 4.0 V	10000/(82 V_{CC} – 3)			
		2.2 ≤ V_{CC} < 2.7 V	4000/(84 V_{CC} – 143)			
		2.0 ≤ V_{CC} < 2.2 V	4000/(105 V_{CC} – 189)			
$t_{WL}(X_{IN})$	Main clock X_{IN} input “L” pulse width	4.5 ≤ V_{CC} ≤ 5.5 V	25			ns
		4.0 ≤ V_{CC} < 4.5 V	4000/(86 V_{CC} – 219)			
		2.7 ≤ V_{CC} < 4.0 V	10000/(82 V_{CC} – 3)			
		2.2 ≤ V_{CC} < 2.7 V	4000/(84 V_{CC} – 143)			
		2.0 ≤ V_{CC} < 2.2 V	4000/(105 V_{CC} – 189)			
$t_C(X_{CIN})$	Sub-clock X_{CIN} input cycle time		20			μs
$t_{WH}(X_{CIN})$	Sub-clock X_{CIN} input “H” pulse width		5			μs
$t_{WL}(X_{CIN})$	Sub-clock X_{CIN} input “L” pulse width		5			μs
t_C(CNTR)	$CNTR_0$–$CNTR_2$ input cycle time	4.5 ≤ V_{CC} ≤ 5.5 V	120			ns
		4.0 ≤ V_{CC} < 4.5 V	160			
		2.7 ≤ V_{CC} < 4.0 V	250			
		2.2 ≤ V_{CC} < 2.7 V	500			
		2.0 ≤ V_{CC} < 2.2 V	1000			
t_{WH}(CNTR)	$CNTR_0$–$CNTR_2$ input “H” pulse width	4.5 ≤ V_{CC} ≤ 5.5 V	48			ns
		4.0 ≤ V_{CC} < 4.5 V	64			
		2.7 ≤ V_{CC} < 4.0 V	115			
		2.2 ≤ V_{CC} < 2.7 V	230			
		2.0 ≤ V_{CC} < 2.2 V	460			
t_{WL}(CNTR)	$CNTR_0$–$CNTR_2$ input “L” pulse width	4.5 ≤ V_{CC} ≤ 5.5 V	48			ns
		4.0 ≤ V_{CC} < 4.5 V	64			
		2.7 ≤ V_{CC} < 4.0 V	115			
		2.2 ≤ V_{CC} < 2.7 V	230			
		2.0 ≤ V_{CC} < 2.2 V	460			
t_{WH}(INT)	INT_{00}, INT_{01}, INT_1, INT_2, INT_3, INT_{40}, INT_{41} input “H” pulse width	4.5 ≤ V_{CC} ≤ 5.5 V	48			ns
		4.0 ≤ V_{CC} < 4.5 V	64			
		2.7 ≤ V_{CC} < 4.0 V	115			
		2.2 ≤ V_{CC} < 2.7 V	230			
		2.0 ≤ V_{CC} < 2.2 V	460			
t_{WL}(INT)	INT_{00}, INT_{01}, INT_1, INT_2, INT_3, INT_{40}, INT_{41} input “L” pulse width	4.5 ≤ V_{CC} ≤ 5.5 V	48			ns
		4.0 ≤ V_{CC} < 4.5 V	64			
		2.7 ≤ V_{CC} < 4.0 V	115			
		2.2 ≤ V_{CC} < 2.7 V	230			
		2.0 ≤ V_{CC} < 2.2 V	460			

Table 19 Timing requirements (2)
(V_{CC} = 2.0 to 5.5 V, V_{SS} = 0V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$t_{C(SCLK1)}$ $t_{C(SCLK3)}$	Serial I/O1, serial I/O3 clock input cycle time(1)	4.5 ≤ Vcc ≤ 5.5 V	250			ns
		4.0 ≤ Vcc < 4.5 V	320			
		2.7 ≤ Vcc < 4.0 V	500			
		2.2 ≤ Vcc < 2.7 V	1000			
		2.0 ≤ Vcc < 2.2 V	2000			
$t_{WH(SCLK1)}$ $t_{WH(SCLK3)}$	Serial I/O1, serial I/O3 clock input “H” pulse width(1)	4.5 ≤ Vcc ≤ 5.5 V	120			ns
		4.0 ≤ Vcc < 4.5 V	150			
		2.7 ≤ Vcc < 4.0 V	240			
		2.2 ≤ Vcc < 2.7 V	480			
		2.0 ≤ Vcc < 2.2 V	950			
$t_{WL(SCLK1)}$ $t_{WL(SCLK3)}$	Serial I/O1, serial I/O3 clock input “L” pulse width(1)	4.5 ≤ Vcc ≤ 5.5 V	120			ns
		4.0 ≤ Vcc < 4.5 V	150			
		2.7 ≤ Vcc < 4.0 V	240			
		2.2 ≤ Vcc < 2.7 V	480			
		2.0 ≤ Vcc < 2.2 V	950			
$t_{su(RxD1-SCLK1)}$ $t_{su(RxD3-SCLK3)}$	Serial I/O1, serial I/O3 clock input setup time	4.5 ≤ Vcc ≤ 5.5 V	70			ns
		4.0 ≤ Vcc < 4.5 V	90			
		2.7 ≤ Vcc < 4.0 V	100			
		2.2 ≤ Vcc < 2.7 V	200			
		2.0 ≤ Vcc < 2.2 V	400			
$t_{h(SCLK1-RxD1)}$ $t_{h(SCLK3-RxD3)}$	Serial I/O1, serial I/O3 clock input hold time	4.5 ≤ Vcc ≤ 5.5 V	32			ns
		4.0 ≤ Vcc < 4.5 V	40			
		2.7 ≤ Vcc < 4.0 V	50			
		2.2 ≤ Vcc < 2.7 V	100			
		2.0 ≤ Vcc < 2.2 V	200			
$t_{C(SCLK2)}$	Serial I/O2 clock input cycle time	4.5 ≤ Vcc ≤ 5.5 V	500			ns
		4.0 ≤ Vcc < 4.5 V	650			
		2.7 ≤ Vcc < 4.0 V	1000			
		2.2 ≤ Vcc < 2.7 V	2000			
		2.0 ≤ Vcc < 2.2 V	4000			
$t_{WH(SCLK2)}$	Serial I/O2 clock input “H” pulse width	4.5 ≤ Vcc ≤ 5.5 V	200			ns
		4.0 ≤ Vcc < 4.5 V	260			
		2.7 ≤ Vcc < 4.0 V	400			
		2.2 ≤ Vcc < 2.7 V	950			
		2.0 ≤ Vcc < 2.2 V	2000			
$t_{WL(SCLK2)}$	Serial I/O2 clock input “L” pulse width	4.5 ≤ Vcc ≤ 5.5 V	200			ns
		4.0 ≤ Vcc < 4.5 V	260			
		2.7 ≤ Vcc < 4.0 V	400			
		2.2 ≤ Vcc < 2.7 V	950			
		2.0 ≤ Vcc < 2.2 V	2000			
$t_{su(SIN2-SCLK2)}$	Serial I/O2 clock input setup time	4.5 ≤ Vcc ≤ 5.5 V	100			ns
		4.0 ≤ Vcc < 4.5 V	130			
		2.7 ≤ Vcc < 4.0 V	200			
		2.2 ≤ Vcc < 2.7 V	400			
		2.0 ≤ Vcc < 2.2 V	800			
$t_{h(SCLK2-SIN2)}$	Serial I/O2 clock input hold time	4.5 ≤ Vcc ≤ 5.5 V	100			ns
		4.0 ≤ Vcc < 4.5 V	130			
		2.7 ≤ Vcc < 4.0 V	150			
		2.2 ≤ Vcc < 2.7 V	300			
		2.0 ≤ Vcc < 2.2 V	600			

NOTES:
1. When bit 6 of address $001A_{16}$ and bit 6 of address 0032_{16} are “1” (clock synchronous).
Divide this value by four when bit 6 of address $001A_{16}$ and bit 6 of address 0032_{16} are “0” (UART).

Table 20 Switching characteristics (1)
(V_{CC} = 2.0 to 5.5 V, V_{SS} = 0V, Ta = −20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
$t_{WH}(S_{CLK1})$ $t_{WH}(S_{CLK3})$	Serial I/O1, serial I/O3 clock output “H” pulse width	4.5 ≤ V_{CC} ≤ 5.5 V	Fig.87	$t_C(S_{CLK1})$/2-30, $t_C(S_{CLK3})$/2-30			ns
		4.0 ≤ V_{CC} < 4.5 V		$t_C(S_{CLK1})$/2-35, $t_C(S_{CLK3})$/2-35			
		2.7 ≤ V_{CC} < 4.0 V		$t_C(S_{CLK1})$/2-40, $t_C(S_{CLK3})$/2-40			
		2.2 ≤ V_{CC} < 2.7 V		$t_C(S_{CLK1})$/2-45, $t_C(S_{CLK3})$/2-45			
		2.0 ≤ V_{CC} < 2.2 V		$t_C(S_{CLK1})$/2-50, $t_C(S_{CLK3})$/2-50			
$t_{WL}(S_{CLK1})$ $t_{WL}(S_{CLK3})$	Serial I/O1, serial I/O3 clock output “L” pulse width	4.5 ≤ V_{CC} ≤ 5.5 V		$t_C(S_{CLK1})$/2-30, $t_C(S_{CLK3})$/2-30			ns
		4.0 ≤ V_{CC} < 4.5 V		$t_C(S_{CLK1})$/2-35, $t_C(S_{CLK3})$/2-35			
		2.7 ≤ V_{CC} < 4.0 V		$t_C(S_{CLK1})$/2-40, $t_C(S_{CLK3})$/2-40			
		2.2 ≤ V_{CC} < 2.7 V		$t_C(S_{CLK1})$/2-45, $t_C(S_{CLK3})$/2-45			
		2.0 ≤ V_{CC} < 2.2 V		$t_C(S_{CLK1})$/2-50, $t_C(S_{CLK3})$/2-50			
$t_d(S_{CLK1}\text{-}T_xD_1)$ $t_d(S_{CLK3}\text{-}T_xD_3)$	Serial I/O1, serial I/O3 output delay time(1)	4.5 ≤ V_{CC} ≤ 5.5 V				140	ns
		4.0 ≤ V_{CC} < 4.5 V				200	
		2.7 ≤ V_{CC} < 4.0 V				350	
		2.2 ≤ V_{CC} < 2.7 V				400	
		2.0 ≤ V_{CC} < 2.2 V				420	
$t_v(S_{CLK1}\text{-}T_xD_1)$ $t_v(S_{CLK3}\text{-}T_xD_3)$	Serial I/O1, serial I/O3 output valid time(1)	4.5 ≤ V_{CC} ≤ 5.5 V		−30			ns
		4.0 ≤ V_{CC} < 4.5 V		−30			
		2.7 ≤ V_{CC} < 4.0 V		−30			
		2.2 ≤ V_{CC} < 2.7 V		−30			
		2.0 ≤ V_{CC} < 2.2 V		−30			
$t_r(S_{CLK1})$ $t_r(S_{CLK3})$	Serial I/O1, serial I/O3 rise time of clock output	4.5 ≤ V_{CC} ≤ 5.5 V				30	ns
		4.0 ≤ V_{CC} < 4.5 V				35	
		2.7 ≤ V_{CC} < 4.0 V				40	
		2.2 ≤ V_{CC} < 2.7 V				45	
		2.0 ≤ V_{CC} < 2.2 V				50	
$t_f(S_{CLK1})$ $t_f(S_{CLK3})$	Serial I/O1, serial I/O3 fall time of clock output	4.5 ≤ V_{CC} ≤ 5.5 V				30	ns
		4.0 ≤ V_{CC} < 4.5 V				35	
		2.7 ≤ V_{CC} < 4.0 V				40	
		2.2 ≤ V_{CC} < 2.7 V				45	
		2.0 ≤ V_{CC} < 2.2 V				50	
$t_{WH}(S_{CLK2})$	Serial I/O2 clock output “H” pulse width	4.5 ≤ V_{CC} ≤ 5.5 V		$t_C(S_{CLK2})$/2-160			ns
		4.0 ≤ V_{CC} < 4.5 V		$t_C(S_{CLK2})$/2-200			
		2.7 ≤ V_{CC} < 4.0 V		$t_C(S_{CLK2})$/2-240			
		2.2 ≤ V_{CC} < 2.7 V		$t_C(S_{CLK2})$/2-260			
		2.0 ≤ V_{CC} < 2.2 V		$t_C(S_{CLK2})$/2-280			
$t_{WL}(S_{CLK2})$	Serial I/O2 clock output “L” pulse width	4.5 ≤ V_{CC} ≤ 5.5 V		$t_C(S_{CLK2})$/2-160			ns
		4.0 ≤ V_{CC} < 4.5 V		$t_C(S_{CLK2})$/2-200			
		2.7 ≤ V_{CC} < 4.0 V		$t_C(S_{CLK2})$/2-240			
		2.2 ≤ V_{CC} < 2.7 V		$t_C(S_{CLK2})$/2-260			
		2.0 ≤ V_{CC} < 2.2 V		$t_C(S_{CLK2})$/2-280			
$t_d(S_{CLK2}\text{-}S_{OUT2})$	Serial I/O2 output delay time	4.5 ≤ V_{CC} ≤ 5.5 V				200	ns
		4.0 ≤ V_{CC} < 4.5 V				250	
		2.7 ≤ V_{CC} < 4.0 V				300	
		2.2 ≤ V_{CC} < 2.7 V				350	
		2.0 ≤ V_{CC} < 2.2 V				400	
$t_v(S_{CLK2}\text{-}S_{OUT2})$	Serial I/O2 output valid time	4.5 ≤ V_{CC} ≤ 5.5 V			0		ns
		4.0 ≤ V_{CC} < 4.5 V			0		
		2.7 ≤ V_{CC} < 4.0 V			0		
		2.2 ≤ V_{CC} < 2.7 V			0		
		2.0 ≤ V_{CC} < 2.2 V			0		

NOTES:
1. When the $P4_5/T_xD_1$ P-channel output disable bit of the UART1 control register (bit 4 of address $001B_{16}$) is “0”.

Table 21 Switching characteristics (2)
(V_{CC} = 2.0 to 5.5 V, V_{SS} = 0V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
t_f(SCLK2)	Serial I/O2 fall time of clock output	4.5 ≤ Vcc ≤ 5.5 V	Fig.87			30	ns
		4.0 ≤ Vcc < 4.5 V				35	
		2.7 ≤ Vcc < 4.0 V				40	
		2.2 ≤ Vcc < 2.7 V				45	
		2.0 ≤ Vcc < 2.2 V				50	
t_r(CMOS)	CMOS rise time of output(1)	4.5 ≤ Vcc ≤ 5.5 V			10	30	ns
		4.0 ≤ Vcc < 4.5 V			12	35	
		2.7 ≤ Vcc < 4.0 V			15	40	
		2.2 ≤ Vcc < 2.7 V			17	45	
		2.0 ≤ Vcc < 2.2 V			20	50	
t_f(CMOS)	CMOS fall time of output(1)	4.5 ≤ Vcc ≤ 5.5 V			10	30	ns
		4.0 ≤ Vcc < 4.5 V			12	35	
		2.7 ≤ Vcc < 4.0 V			15	40	
		2.2 ≤ Vcc < 2.7 V			17	45	
		2.0 ≤ Vcc < 2.2 V			20	50	

NOTES:
1. When the P35/TxD3 P4-channel output disable bit of the UART3 control register (bit 4 of address 003316) is “0”.

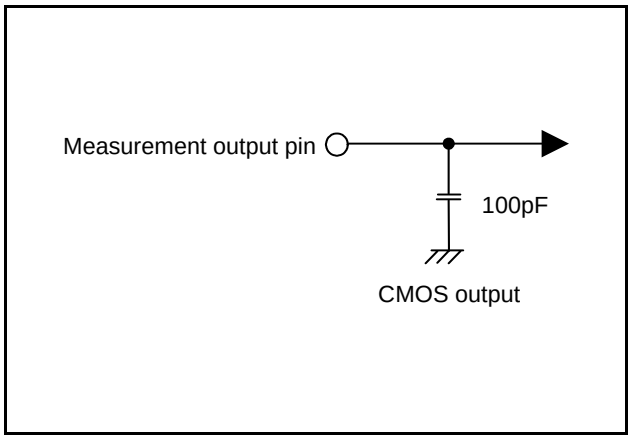


Fig 87. Circuit for measuring output switching characteristics (1)

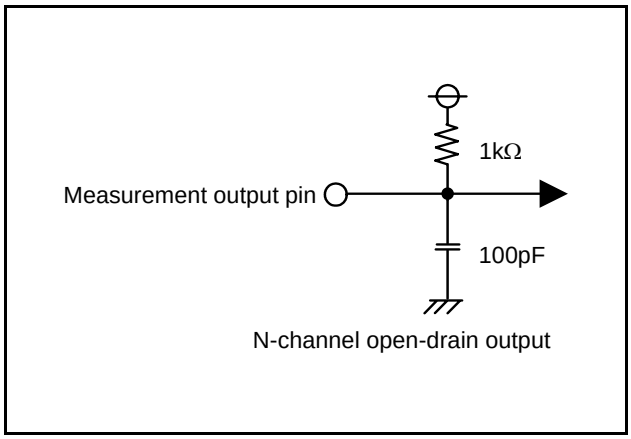


Fig 88. Circuit for measuring output switching characteristics (2)

Single-chip mode timing diagram

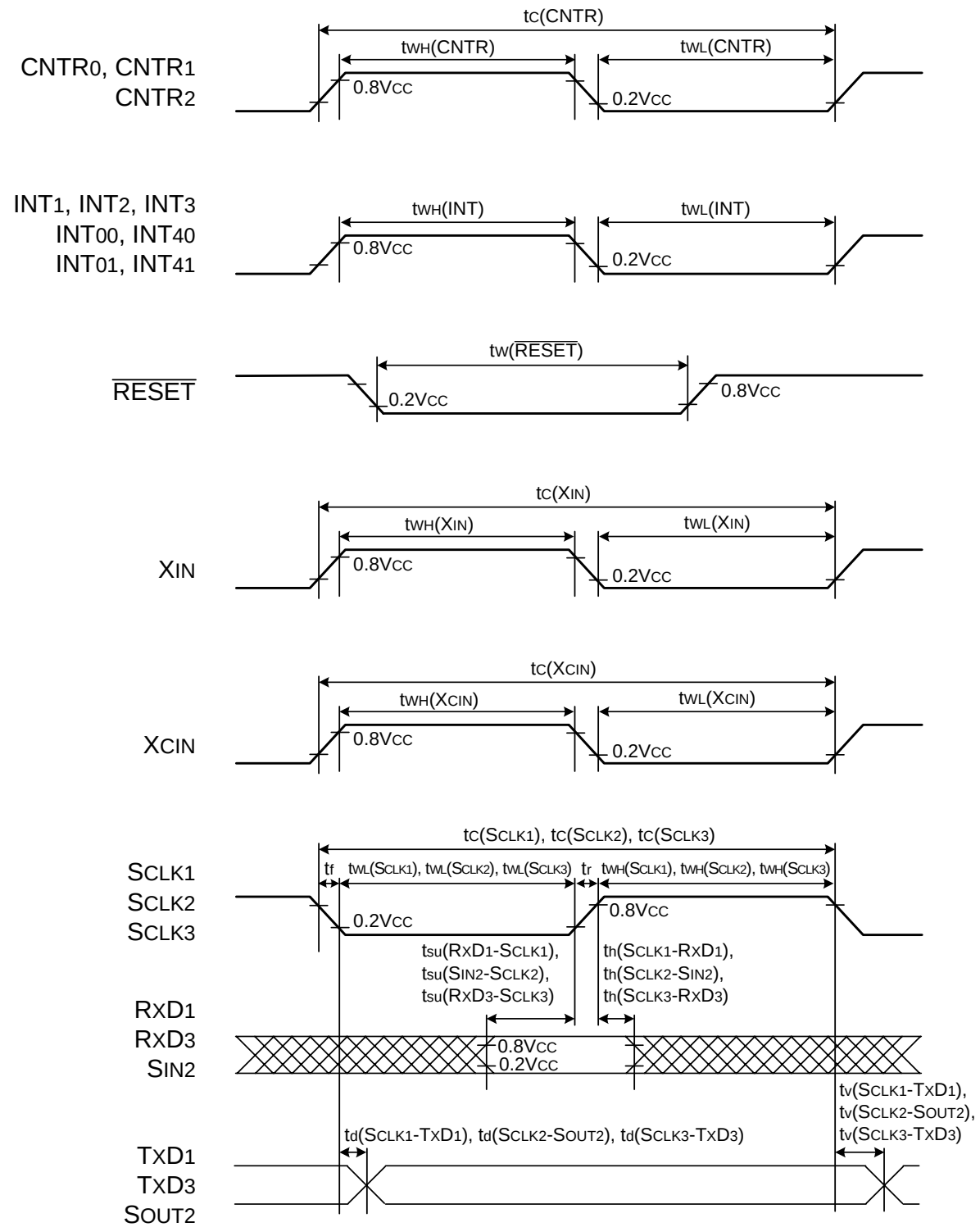
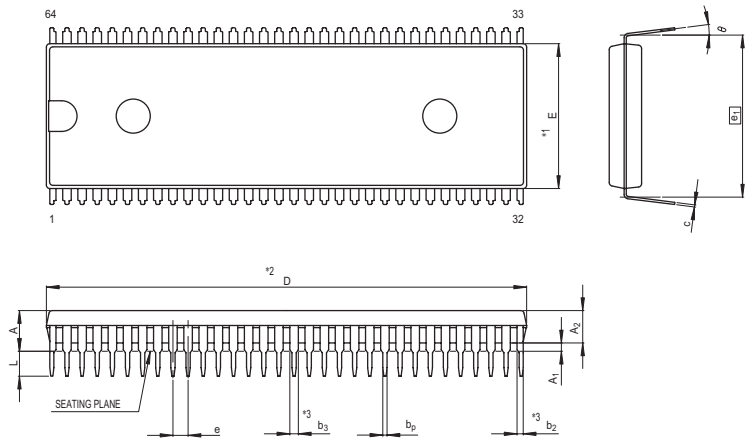


Fig 89. Timing diagram (in single-chip mode)

PACKAGE OUTLINE

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.

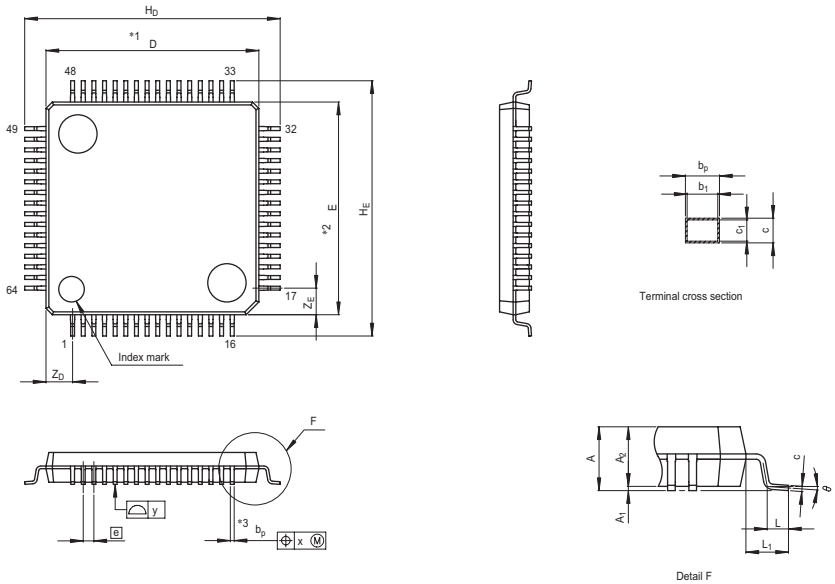
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SDIP64-17x56.4-1.78	PRDP0064BA-A	64P4B	7.9g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e1	18.75	19.05	19.35
D	56.2	56.4	56.6
E	16.85	17.0	17.15
A	—	—	5.08
A_1	0.38	—	—
A_2	—	3.8	—
b_p	0.4	0.5	0.6
b_2	0.65	0.75	1.05
b_3	0.9	1.0	1.3
c	0.2	0.25	0.32
θ	0°	—	15°
e	1.528	1.778	2.028
L	2.8	—	—

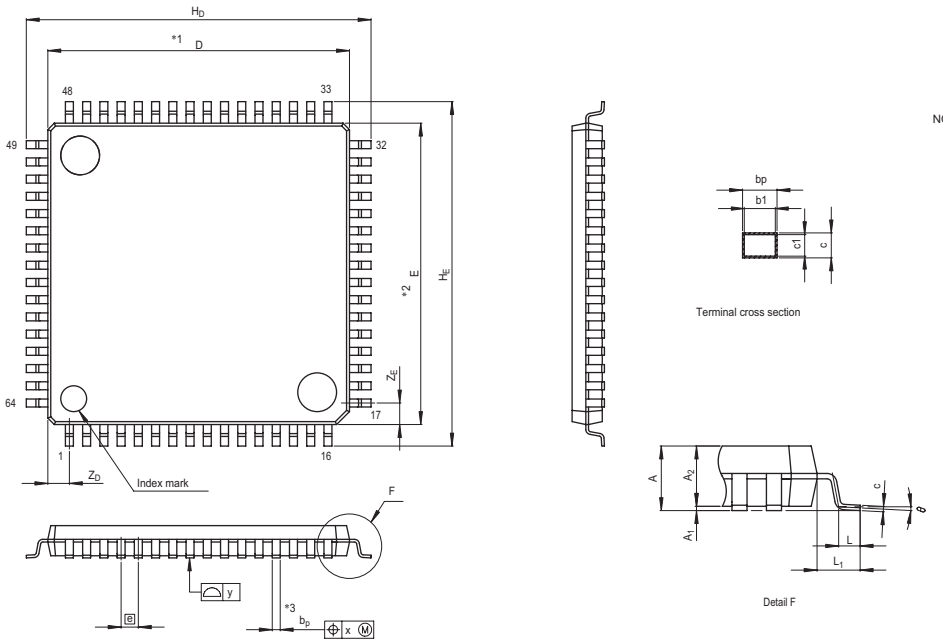
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

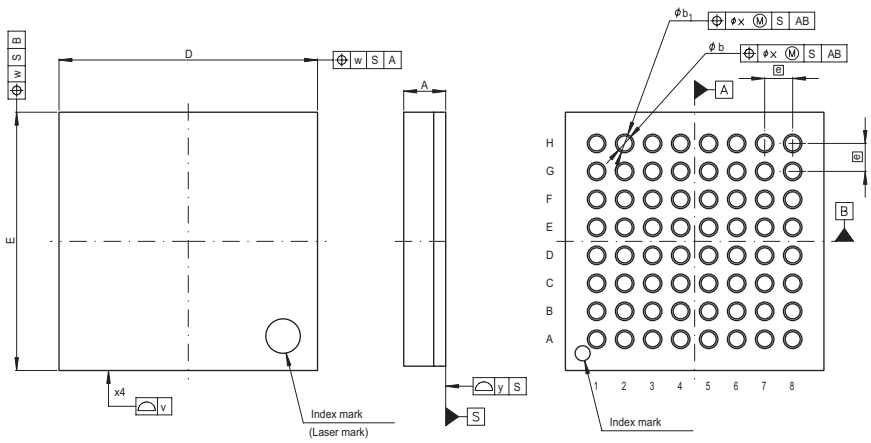
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-14x14-0.80	PLQP0064GA-A	64P6U-A	0.7g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.3	0.5	0.7
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA64-6x6-0.65	PTLG0064JA-A	64F0G	0.07g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	6.0	—
E	—	6.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.65	—
b	0.31	0.35	0.39
b_1	0.39	0.43	0.47
x	—	—	0.08
y	—	—	0.10

REVISION HISTORY	3803 Group (Spec.H QzROM version) Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Sep. 30, 200	–	First Edition issued
1.10	Nov. 14, 2005	20	Fig 14. Port block diagram (3) (18) Port P56 revised
		61	Fig 54. Block diagram of Watchdog timer; STP instruction disable bit → STP instruction function selection bit revised
		69	QzROM version; approximately 1 k to 5 kΩ resistor → approximately 5 kΩ resistor Fig 47. Wiring for the CNVSS/VPP added Notes On QzROM Writing Orders; (extension: .mask) → (extension: .msk) revised
		82 to 83	Package Outline revised
		84 to 91	Appendix added
1.13	Aug 21, 2009	1	FEATURES revised
		2	Table 1 moved Last Table 2 deleted
		3	Last Table 3 deleted
		4	Fig 3 added
		5	Table 1 added
		6	Fig 4 revised
		7	Table 2 revised
		8	Fig 5 revised
		9	Packages revised Fig 6 revised
		10	GROUP DESCRIPTION deleted Table 3 revised
		16	Fig 11 revised
		17	Fig 12 revised
		18	Table 6 revised
		21	Fig 15 revised
		26	Termination of unused pins added Table 7 added
		27 to 32	Chapter “INTERRUPTS” revised
		46	Fig 37 revised
		47	(2) Asynchronous Serial I/O (UART) Mode revised Fig 39 revised
		48	[Serial I/O1 Status Register (SIO1STS)] revised
		50	<Notes concerning serial I/O1> revised
		51	6. Transmission control when external clock is selected revised Reason revised
		53	Fig 43 revised
		54	(1) Clock Synchronous Serial I/O Mode revised Fig 45 revised

REVISION HISTORY	3803 Group (Spec.H QzROM version) Datasheet

Rev.	Date	Description	
		Page	Summary
1.13	Aug 21, 2009	55	(2) Asynchronous Serial I/O (UART) Mode revised Fig 47 revised
		56	[Serial I/O3 Status Register (SIO3STS)] revised
		58	<Notes concerning serial I/O3> revised
		59	6. Transmission control when external clock is selected revised 7. Transmit interrupt request when transmit enable bit is set revised
		60	PWM Operation revised
		62	[AD Conversion Register 1, 2] AD1, AD2 revised [AD/DA Control Register] ADCON revised [Comparator and Control Circuit]] revised Fig 54 added Fig 55 revised
		64	D/A CONVERTER revised
		65	Watchdog Timer Initial Value revised Fig 59 revised
		69	Fig 64 revised Fig 65 revised
		70	Fig 66 revised
		72	QzROM Writing Mode added Table 9 added
		73	Fig 68 added
		74	Fig 69 added
		75	Fig 70 added
		76	Fig 71 added
		77	Fig 72 added
		78 to 87	NOTES revised
		88	Table 10 revised
		91	Table 13 revised
		93	Table 15 revised Table 17 revised
		99	PACKAGE OUTLINE revised

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