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SEMICONDUCTOR TECHNICAL DATA

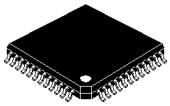
MCM10010

ImageMOS™

Advance Information

12-bit Image Capture Engine

with ADC / CDS / and digitally programmable PGA and DC offset voltage adjust



48 LQFP

Features:

- High precision12-bit version of MCM10009
- 15 MSPS (Million Samples Per Second) maximum throughput (1 MSPS to 15 MSPS operating range)
- 12-bit, pipelined algorithmic RSD ADC (DNL ± 0.8 LSB, INL ±2.0 LSB)
- 4 multiplexed analog inputs with individual DC restore circuitry
- CDS sample and hold aids suppression of low frequency noise and correlated reset noise
- 18 dB of variable gain, programmable by an 8-bit Digital Programmable Gain Amplifier (DPGA), optimizes dynamic range, and facilitates white balance and iris adjustment
- 6-bit programmable DC offset adjustment
- On-chip dark level calibration circuitry controlled by external pin
- Interfaces to CCD or CMOS imager signal levels (1 V_{pp} input)
- Fully differential analog signal processing pipeline for high noise immunity
- On-chip reference and bias voltages
- Three pin serial programming interface
- 175 mW average power @ 3.0 V supply voltage
- Standby power down mode and 3-state output enable
- Single supply, 3.0V - 3.6V range operation
- Commercial temperature operating range of 0˚C to 70˚C

Ordering Information	
Device	**Package**
MCM10010EB	48 LQFP

The MCM10010 is a fully integrated, high performance CMOS analog signal processing engine for color or monochrome digital imaging consumer applications, such as digital cameras, video conferencing and scanners. This part provides system designers a 12 bit ADC integrated together with the functional blocks required to build a complete analog signal processing pipeline.

Four multiplexed analog inputs, each with individually programmable digital gain registers, allows per pixel rate, gain balancing from user supplied data. These features combine to provide the user with a single chip solution to easily convert standard analog CCD and CMOS combined outputs to a twelve bit digital signal for subsequent signal processing.

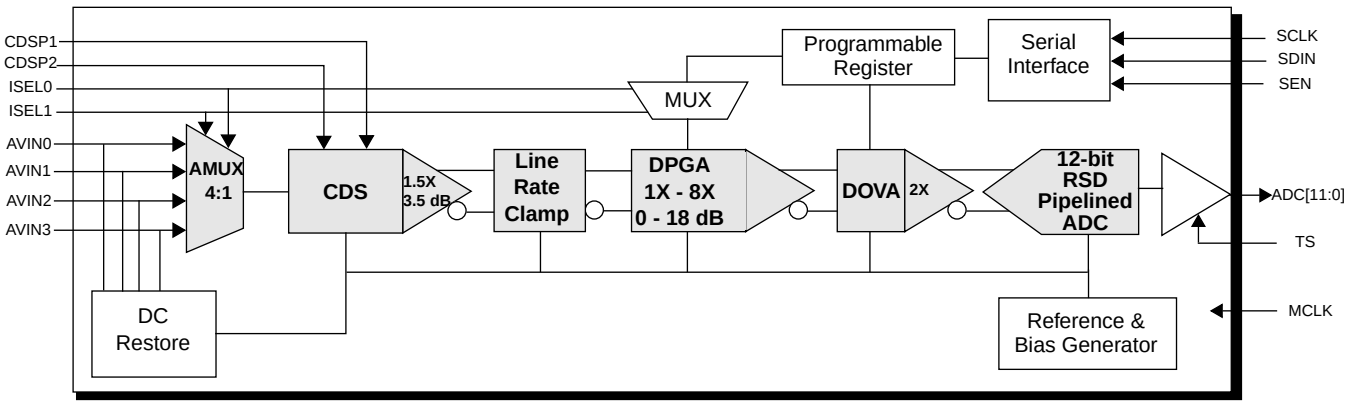


Figure 1. MCM10010 Simplified Block Diagram

This document contains information on a new product.
Specifications and information herein are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1] (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to 3.8	V
V_{in}	DC Input Voltage	-0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage	-0.5 to V_{DD} + 0.5	V
I	DC Current Drain per Pin, Any Single Input or Output	±50	mA
I	DC Current Drain, V_{DD} and V_{SS} Pins	±100	mA
T_{STG}	Storage Temperature Range	-65 to +150	˚C
T_L	Lead Temperature (10 second soldering)	300	˚C

[1] Maximum Ratings are those values beyond which damage to the device may occur.

$V_{SS} = AV_{SS} = DV_{SS} = V_{SSO}$ ($DV_{SS} = V_{SS}$ of Digital circuit, $AV_{SS} = V_{SS}$ of Analog Circuit)
$V_{DD} = AV_{DD} = DV_{DD} = V_{DDO}$ ($DV_{DD} = V_{DD}$ of Digital circuit, $AV_{DD} = V_{DD}$ of Analog Circuit)

RECOMMENDED OPERATING CONDITIONS (to guarantee functionality, voltage referenced to V_{SS})

Symbol	Parameter	Min	Max	Unit
V_{DD}	DC Supply Voltage, V_{DD} = 3.3V (Nominal)	3.0	3.6	V
T_A	Operating Ambient Temperature	0	70	˚C
T_J	Junction Temperature	0	125	˚C

Notes:
- All parameters are characterized for DC conditions after thermal equilibrium has been established.
- Unused inputs must always be tied to an appropriate logic level, e.g., either V_{SS} or V_{DD}.
- This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than the maximum rated voltages to this high impedance circuit.
- For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 3.3V ± 0.3V, V_{DD} referenced to V_{SS}

Symbol	Characteristic	Condition	T_A = 0˚C to 70˚C		Unit
			Min	Max	
V_{IH}	Input High Voltage		2.0	V_{DD}+0.3	V
V_{IL}	Input Low Voltage		-0.3	0.8	V
I_{in}	Input Leakage Current, No Pull-up Resistor	$V_{in} = V_{DD}$ or V_{SS}	-5	5	µA
I_{OH}	Output High Current	V_{DD} = Min, V_{OH} Min = 0.8 * V_{DD}	-3		mA
I_{OL}	Output Low Current	V_{DD} = Min, V_{OL} Max = 0.4 V	3		mA
V_{OH}	Output High Voltage	V_{DD} = Min, I_{OH} = -100µA	V_{DD} - 0.2		V
V_{OL}	Output Low Voltage	V_{DD} = Min, I_{OL} = 100µA		0.2	V
I_{OZ}	3-State Output Leakage Current	Output = High Impedance, $V_{out} = V_{DD}$ or V_{SS}	-10	10	µA
I_{DDO}	Supply Current	Operating Mode, I_{out} = 0mA, $V_{in} = V_{DD}$ or V_{SS}		100	mA
I_{DDS}	Standby Supply Current	Standby Mode, I_{out} = 0mA, $V_{in} = V_{DD}$ or V_{SS}		10	mA

POWER DISSIPATION (V_{DD} = 3.0V, V_{DD} referenced to V_{SS}, T_a = 25˚C)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
P_{DYN}	Dynamic Power	15 MSPS		275		mW
P_{STDBY}	Standby Power	STDBY Pin Logic High		25		mW
P_{AVG}	Average Power	15 MSPS Operation (using STDBY)		175		mW

ELECTRICAL CHARACTERISTICS

DC Restore Clamp (DCR)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{line}[2]	Required charging time				Line Rate	MHz
C_{AVIN}	AVIN External AC Coupling Capacitor			3300		pF

[2] $f_{line} = f_{pixel}$ x imager's width in pixels

Correlated Double Sampler (CDS)

V_{IN}	Input Voltage Range				1.0	V_{pp}
f_{max}	Maximum Input Pixel Frequency				15	MHz
A_V	Amplifier Output Gain (fixed)				3.5 1.5	dB Voltage
C_{IN}	AVSS Input Capacitance	Includes Pad Capacitance			5.0	pF
I_{IN}	AVSS Input Current	V(AVSS) = $V_{DD}/2$	0		20	nA
	Latency				1.5	clock cycles

Line Rate Clamp (LRC)

ΔV	Voltage Drop over Sample Period		0	-0.5	-0.8	LSB
f_{max}	Maximum Operational Frequency				f_{line}	MHz
	Charge Time	12-bit Accuracy			$16/f_{pixel}$	sec
C_{IN}	Input Capacitance				3.0	pF
	Latency				0.5	clock cycles
C_{LRC}	External LRC Holding Capacitor[3]			3300	5000	pF

[3] LRC Capacitance to V_{ss} - see section 1.4

Digitally Programmable Gain Amplifier (DPGA)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
A_{dB} A_V	Gain (8-bit Digitally Programmable)	Code = $00000000_2 = 0_{10}$	0 1X			dB Voltage
A_{dB} A_V		Code = $11111111_2 = 255_{10}$			18 8X	dB Voltage
V_{pp}	Peak to Peak Output Voltage				1.5	V
A_{LIN}	Gain Resolution		0.0273X			gain/step
A_{ERR}	Gain Error				±1.0	%
f_{max}	Maximum Input Pixel Frequency				15	MHz
	Digital Programming Code resolution		8			bits
	Latency				1	clock cycles
C_{IN}	Input Capacitance				3.0	pF

ELECTRICAL CHARACTERISTICS

DC Offset Adjust (DOVA)

V_{OS}	Offset Adjust Voltage (6-bit Digitally Programmable)[4]	Code = $011111_2 = 31_{10}$ Code = $111111_2 = -31_{10}$	-181.64		181.64	mV
V_{RES}	Resolution			5.86		mV
A_V	Amplifier Output Gain (fixed)				6 2X	dB Voltage
	Digital Programming Code Resolution		6			bits
	Latency				0.5	clock cycles
C_{IN}	Input Capacitance				3.0	pF

[4] MSB sign-bit (0 = positive, 1 = negative)

Analog to Digital Converter (ADC)

	Resolution		12			bits
V_{IN}	Input Dynamic Range[5]				3.0	V_{pp}
INL	Integral Non-Linearity				±2.0	LSB
DNL	Differential Non-Linearity				±0.8	LSB
	Missing Codes		Guaranteed Zero			
f_{max}	ADC Clock Rate				15	MHz
t_{pd}	ADC Clock to Output delay	Clock to D_n Output			0.75	ns
	Latency				7.5	clock cycles
C_{IN}	Input Capacitance				3.0	pF

[5] Effective differential signal dynamic range

SERIAL INTERFACE

f_{max}	SCLK			15	MHz
t_{suSEN}	SEN to SCLK setup time	1.0			ns
t_{hSEN}	SEN to SCLK hold time	0.5			ns
t_{suSDIN}	SDIN to SCLK setup time	1.0			ns
t_{hSDIN}	SDIN to SCLK hold time	0.5			ns

Table 1. MCM10010 Pin Listing

Pin No.	Pin Name	Description	Pin Type	Power
1	AVSS	Analog Ground	G	A
2	AVIN0	Analog Input	I	
3	AVIN1	Analog Input	I	
4	AVIN2	Analog Input	I	
5	AVSS	Analog Ground	G	A
6	AVIN3	Analog Input	I	
7	AVSS	Analog Ground	G	A
8	CLRCA	Line Rate Clamp Output	O	
9	CLRCB	Line Rate Clamp Output	O	
10	CVREFM	Bias Reference Low Output	O	
11	CVREFP	Bias Reference High Output	O	
12	AVSS	Analog Ground	G	A
13	AVDD	Analog Power	P	A
14	AVSS	Analog Ground	G	A
15	AVDD	Analog Power	P	A
16	CLMPE	Line Rate Clamp Enable	I	
17	STDBY	Power Down Standby Mode Enable	I	
18	INIT	Chip Reset	I	
19	N/C	Not Connected		
20	N/C	Not Connected		
21	N/C	Not Connected		
22	TS	Three State Output Enable	I	
23	DVSS	Digital Ground	G	D
24	DVDD	Digital Power	P	D

Pin No.	Pin Name	Description	Pin Type	Power
25	ADC0	Output-bit 0 = $2^0 = 1_{10}$ weight	O	
26	ADC1	Output-bit 1 = $2^1 = 2_{10}$ weight	O	
27	ADC2	Output-bit 2 = $2^2 = 4_{10}$ weight	O	
28	ADC3	Output-bit 3 = $2^3 = 8_{10}$ weight	O	
29	ADC4	Output-bit 4 = $2^4 = 16_{10}$ weight	O	
30	DVSS	Digital Ground	G	D
31	ADC5	Output-bit 5 = $2^5 = 32_{10}$ weight	O	
32	ADC6	Output-bit 6 = $2^6 = 64_{10}$ weight	O	
33	ADC7	Output-bit 7 = $2^7 = 128_{10}$ weight	O	
34	ADC8	Output-bit 8 = $2^8 = 256_{10}$ weight	O	
35	ADC9	Output-bit 9 = $2^9 = 512_{10}$ weight	O	
36	DVDD	Digital Power	P	D
37	DVSS	Digital Ground	G	D
38	ADC10	Output-bit 10 = $2^{10} = 1024_{10}$ weight	O	
39	ADC11	Output-bit 11 = $2^{11} = 2048_{10}$ weight	O	
40	ISEL1	Input and Gain MUX select “1”	I	
41	ISEL0	Input and Gain MUX select “0”	I	
42	SEN	Serial Programming Interface Enable	I	
43	SDIN	Serial Programming Interface Data	I	
44	SCLK	Serial Programming Interface Clock	I	
45	MCLK	Master Clock	I	
46	CDSP2	Sample&Hold Clock “signal”	I	
47	CDSP1	Sample&Hold Clock “reference”	I	
48	AVDD	Analog Power	P	A

Legend:
P = V_{DD}
G = V_{SS}
I = Input
O = Output
D = Digital
A = Analog

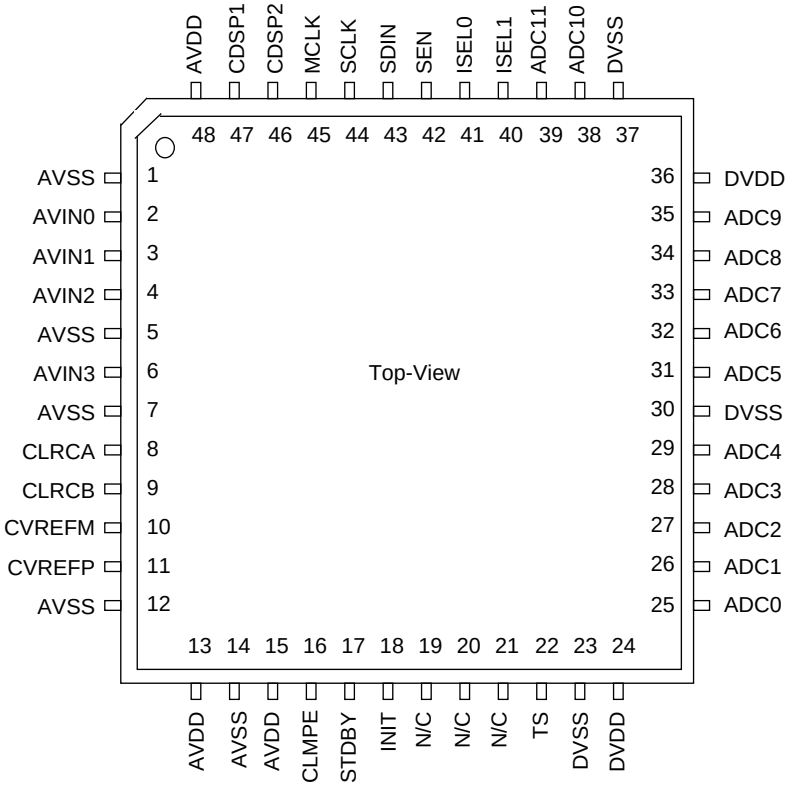


Figure 2. MCM10010 Pinout Diagram

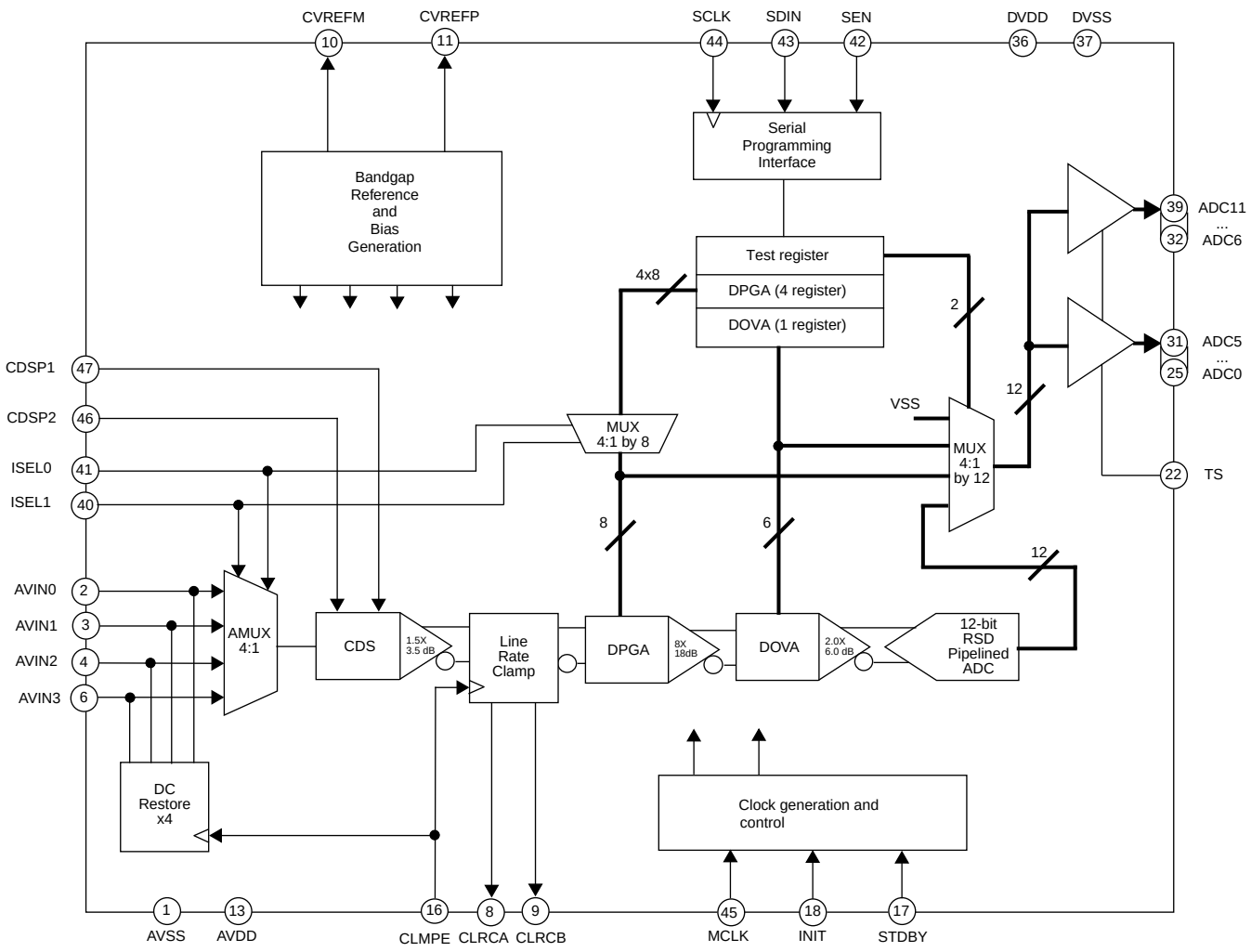
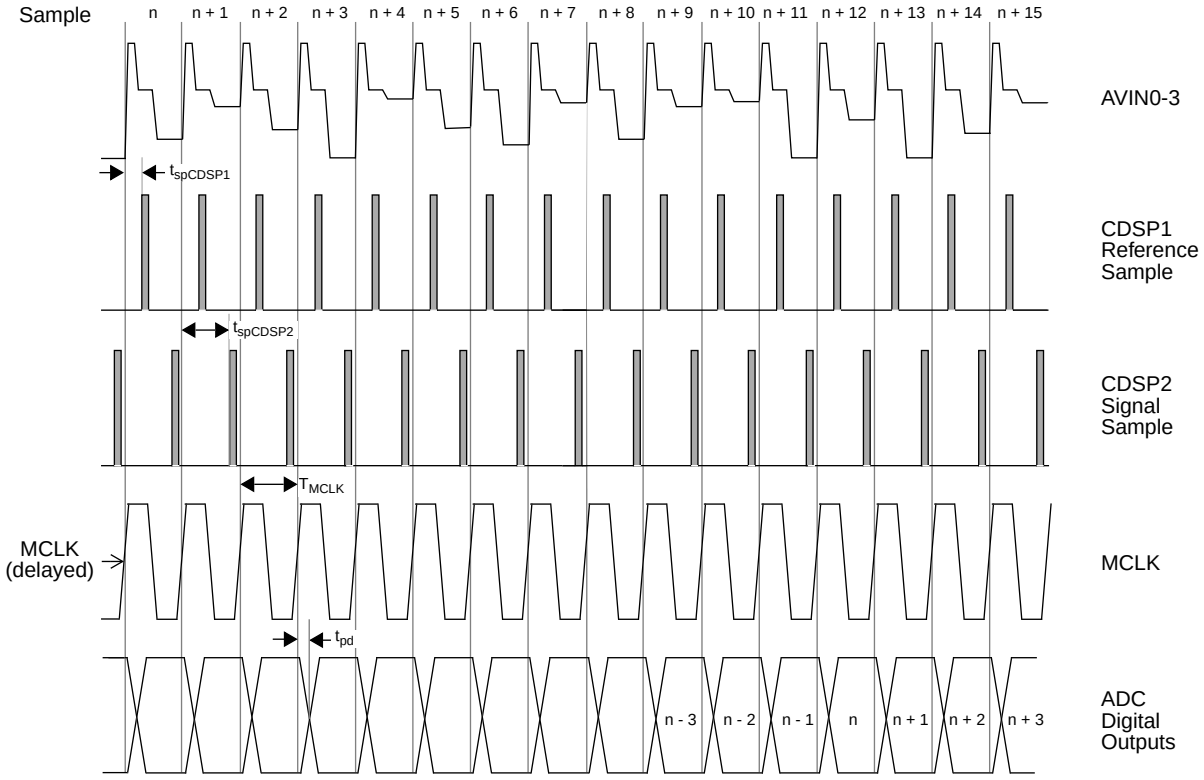


Figure 3. MCM10010 Detailed Block Diagram



Notes:

1.

Latency	= 12 Cycles
f_{MCLK} (max)	= 15 MSPS
T_{MCLK} (min)	= 66.7 ns
t_{pd} (MCLK to ADC_n)	= 0.75 ns
MCLK (delayed)	= MCLK + 4 ns (max. internal clock delay)

2. The CDS samples on the negative edge of CDSP1 and CDSP2.

3. AVIN0-3 are the video input signals from the image sensor. The system designer must provide the necessary skewing of AVIN0-3 to MCLK (delayed), as illustrated.

Figure 4. MCM10010 Timing Diagram

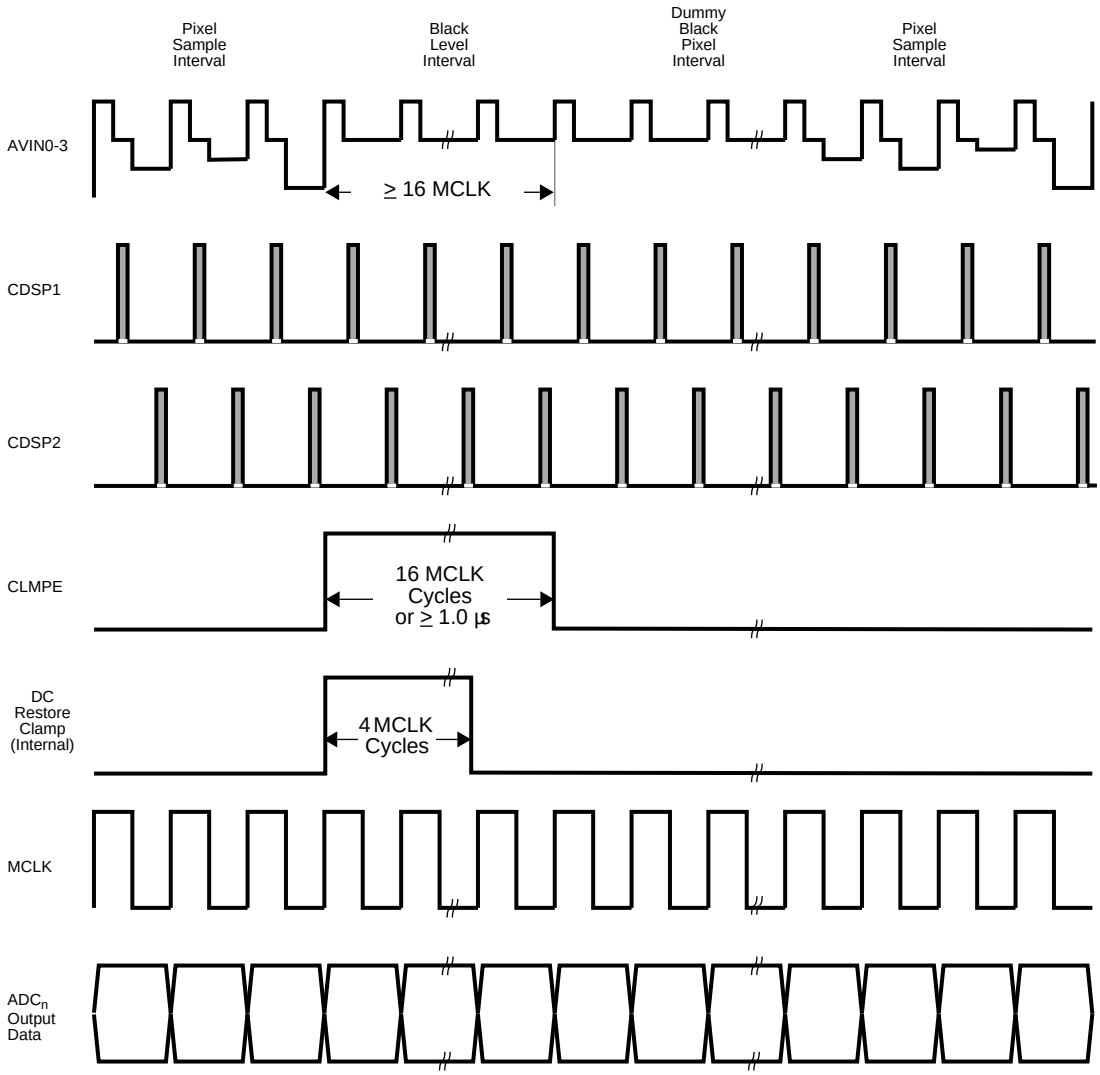
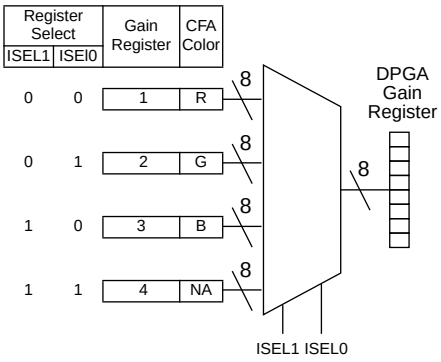
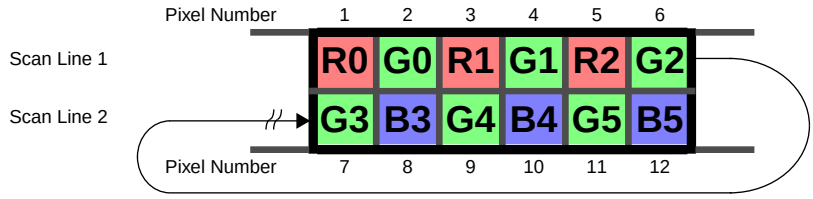


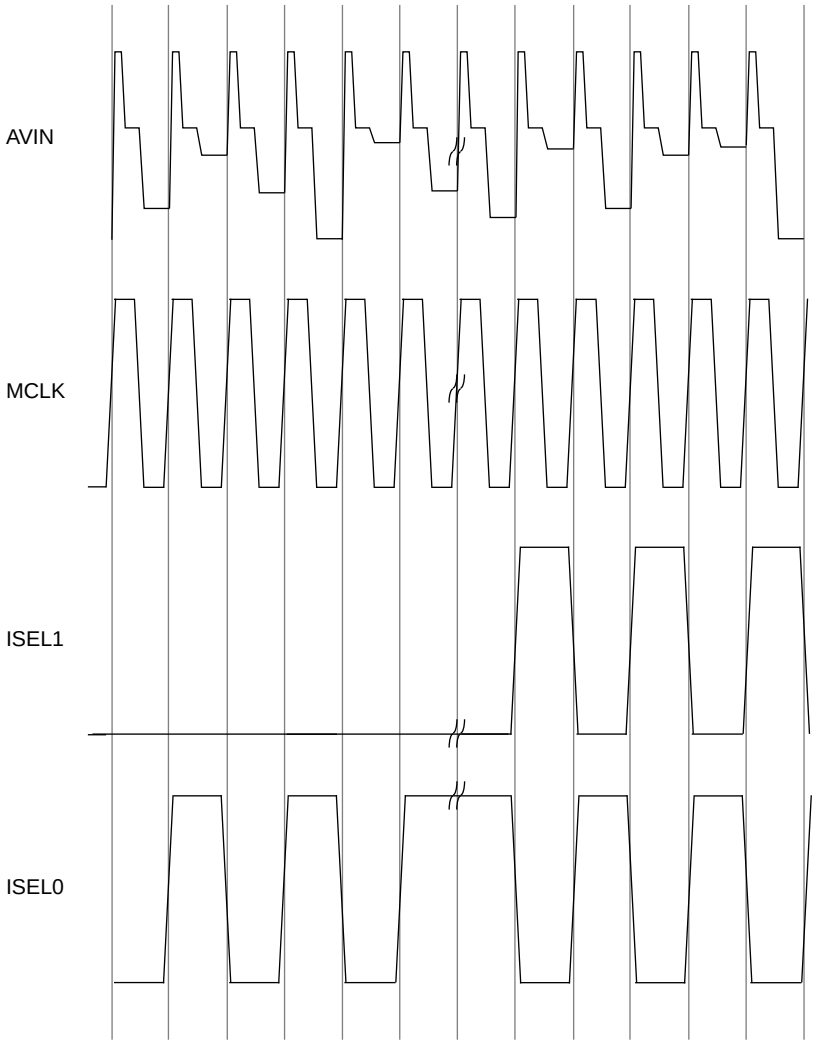
Figure 5. Typical Timing Diagram for Horizontally Blanked System



Pixel Rate Switching
Multiplexer Conceptual Diagram



Pixel Name	R0	G0	R1	G1	R2	G2	G3	B3	G4	B4	G5	B5
Pixel Number = MCLK Period	1	2	3	4	5	6	7	8	9	10	11	12



Pixel Number	1	2	3	4	5	6	7	8	9	10	11	12
Pixel Name	R0	G0	R1	G1	R2	G2	G3	B3	G4	B4	G5	B5
ISEL1Code	0	0	0	0	0	0	0	1	0	1	0	1
ISEL0 Code	0	1	0	1	0	1	1	0	1	0	1	0

The high speed, pixel rate processing capability of the MCM10010 is illustrated in the timing diagram.

The MCM10010 has four multiplexed sensor inputs. Each two bit input select address (ISEL0,ISEL1) is also selecting one Gain register associated with that input. In applications not using all four inputs, the MCM10010 offers the flexibility to trade off the number of inputs used vs. the number of Gain registers assigned to each input.

In this example three analog inputs (AVIN0..2) are connected together and driven from one sensor. The fourth input, with one Gain Register, can be used for an auxiliary function, time permitting. The ISEL0 and ISEL1 input code 0_{10} -2_{10} then becomes the Gain Register select according to the truth table above.

A simple representation of a common Color Filter Array (CFA) image sensor pixel pattern, which uses an RG/GB scan line pattern, (scan line 1 = RG, and scan line 2 = GB) is shown for the application.

Gain Register1,2 and 3 correspond to the R, G and B colors respectively, register 4 and input AVIN3 is unused in this example.

In the example, pixels 1 through 6 appear at the end of the first scan line, which consists of alternating R and G pixels R0, G0, R1, G1, R2 and G2. Pixels 7 through 12 appear at the beginning of the second scan line, which consists of alternating G and B pixels G3, B3, G4, B4, G5 and B5. In image sensors, a set of dark pixels are typically provided in each scan line. However, for ease of illustration, these pixels are omitted in the example. The discontinuity in the timing diagram between MCLK periods 6 and 7 is used to indicate the dark pixel area of operation.

The MCM10010 is designed to allow real time pixel color correction. Therefore, the R correction code, 00 (ISEL1, ISEL0) for pixel R0 should be selected for MCLK period 1, and the G correction code, 01 for pixel G0 in period 2. These codes should then alternate across scan line 1. Similarly, when processing of scan line 2 (GB) begins during MCLK period 7, the G code, 01, should be selected, followed by the B code, 10, in period 8. These codes should also alternate, until the end of scan line 2.

Figure 6. Real-Time CFA gain correction application example

MCM10010 Theory of Operation

The MCM10010 integrates a fully differential analog signal processing pipeline (for interface with solid state image sensors) onto a single chip.

Board-level component requirements are minimized by the integration of the many individual devices comprising the signal processing chain, principally a 4:1 analog input MUX driving the Correlated Double Sampler (CDS), Line Rate Clamp (LRC), Digitally Programmable Gain Amplifier (DPGA), DC Offset Voltage Adjust (DOVA), algorithmic, Redundant Signed Digit (RSD) Analog to Digital Converter (ADC) and timing and bias generation circuits. The result is an extremely flexible, single chip solution to the image sensing and capture to digital transformation process. This allows the system designer to achieve reduced component count, board space and system cost.

Because the chip is designed for 3.3V operation, a wide variety of low power, portable applications may be addressed for consumer applications.

1.0 Analog to Digital Conversion Pipeline

The MCM10010 incorporates a DCR, CDS, DPGA, LRC, DOVA and algorithmic, RSD ADC to digitize an analog signal to a 12-bit digital word for post-processing by additional circuitry (Figure 3).

1.1 Inputs (AVIN0, AVIN1, AVIN2, AVIN3)

Analog voltages from the image sensor are input to the MCM10010 via the AVIN0, AVIN1, AVIN2, and AVIN3 pins. The voltage range must be limited to a maximum of 1.0 volt, peak to peak.

The MCM10010 is designed to operate from a single 3.0 V to 3.6V voltage supply. An external AC coupling capacitor (C_{AVIN}) is required between the imager's output and the MCM10010's AVIN0, AVIN1, AVIN2, and AVIN3 pins to remove the large DC offset component of common CCD image sensors. The recommended capacitor value is approximately 3300 pF.

Other imagers, which utilize low voltage, CMOS-based processes, may be directly compatible with the MCM10010's analog inputs, allowing direct coupling techniques to be used.

Motorola's A-series of Image sensors (MCM20007, 20008) are compatible with the MCM10010 inputs and can be connected without any capacitor or buffering.

1.2 DC Restore (DCR)

The DCR function is provided to establish the DC operating point of the analog input at AVIN0, AVIN1, AVIN2, and AVIN3 relative to the MCM10010's supply voltage.

The DCR is clocked at the imager's line rate when pin CLMPE is active (logic high).

1.3 Correlated Double Sampler (CDS)

Typical CCD imagers provide an output at a pixel rate frequency, f_{pixel}, which contains reset, reference and image analog signal information.

An approximation of a typical CCD imager's output is presented in Figure 7. In the figure, the pixel's period T_{pixel}, is divided into four distinct regions.

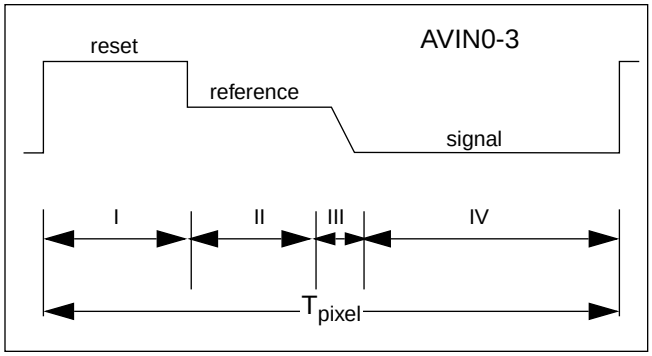


Figure 7. CCD Imager Input Waveform

Region I results from pixel reset, and contains no useful input information. Region II is the period during which the pixel outputs a "reference" level indicative of its intrinsic dark level noise. This point provides a baseline for measurement of the pixel's analog voltage signal.

Region III occurs as a result of the pixel's transition voltage during integration. Its exponential nature is caused by the photo junction's response to the incoming light, and integration of the resulting charge over time.

Region IV, referred to here as the "signal" region, represents the stabilized pixel output voltage which occurs when the pixel has integrated charge in response to the incoming light. The output voltage is the difference of this photoresponse plus the reference voltage.

The regions of interest for evaluation are reference and signal. The CDS circuitry (Figure 8) in the MCM10010 uses switched capacitor techniques to both Sample and Hold (S/H) the incoming analog signal voltage. CDS

sample timing is controlled by the CDSP1 and CDSP2 pulses (section 1.3.1), which are externally driven directly from the CDSP1 and CDSP2 pins

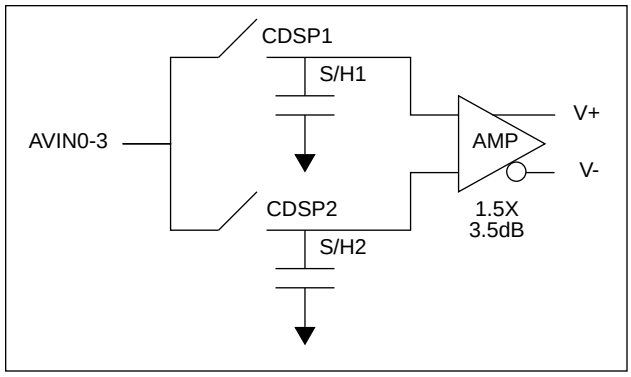


Figure 8. CDS Conceptual Block Diagram

The alternate S/H circuits each sample the pixel waveform, S/H1 in the reference region, and S/H2 in the signal region. The values are then compared against one another by the differential amplifier, thus removing the reference noise by subtraction, improving the accuracy of the measurement for subsequent signal processing.

The correlated nature of this measurement method reduces low frequency noise effects, as the reference and signal sampling points remain well correlated regardless of offset. This feature is illustrated in Figure 9. A cumulative error, ΔV, would normally result between the first and second signal samples without this feature. Reset noise is eliminated by sampling in the reference region.

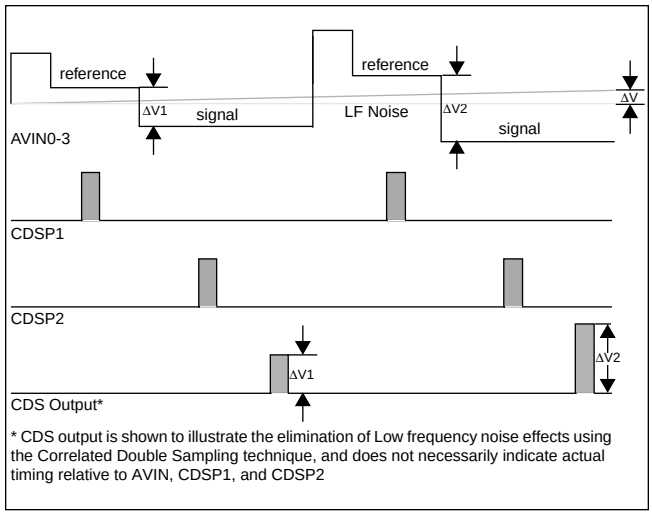


Figure 9. CDS Reduces LF Noise Effects

The amplifier takes the difference of the reference and signal levels, then converts the single-ended imager signal to a differential output. The amplifier also performs a fixed gain of 1.5X (3.5 dB). Together, these features improve accuracy, linearity, dynamic range and signal to noise ratio.

1.3.1 CDS Clocking Requirement

The CDSP1 and CDSP2 external pulses control the timing of the CDS S/H operations. The parameters used to define the CDSP1/2 waveforms are the period, T_{pixel}, aperture pulsewidth (t_{pw}) and placement (t_{sp}). An example of these terms are illustrated in Figure 10.

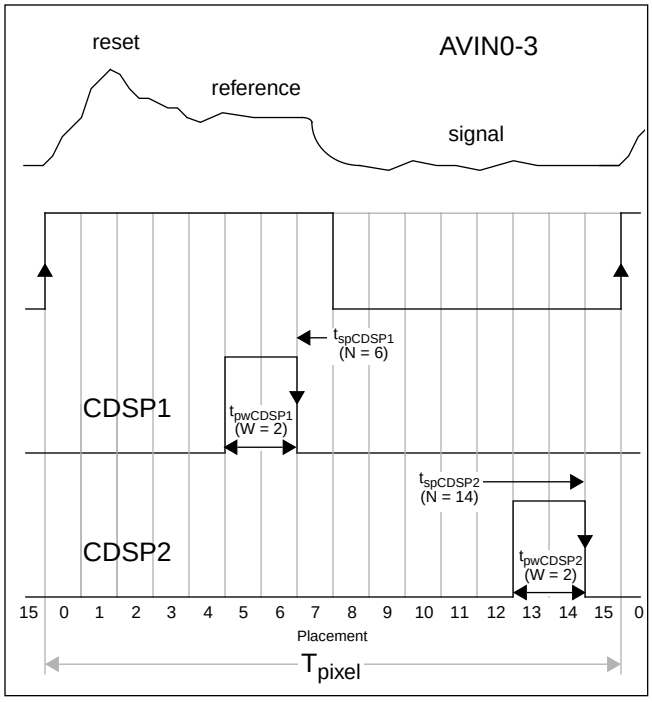


Figure 10. CDS Sampling Waveform Example

The CDS hold occurs on the negative edge of the CDSP clocks. The Minimum pulse width for the CDSP1/2 clocks are 7.5nS. The user must ensure the correct S&H clock timing relative to both the pixel rate clock and the Master clock (MCLK) to match incoming pixel data from the imager.

1.4 Line Rate Clamp (LRC)

The LRC (Figure 11) is designed to provide a feed forward dark level subtract reference level measurement technique. The optical black level reference is re-established each time the image sensor begins a new scan line. Commercially available image sensors provide optical black (dark) pixels to aid in establishing this reference.

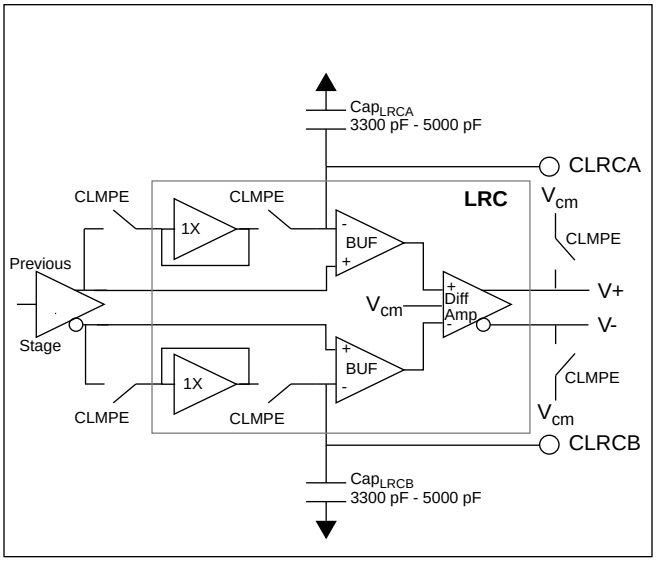


Figure 11. LRC Conceptual Block Diagram

On the MCM10010, dark pixel input signals should be sampled for a minimum of 1 µs to allow the two 3300 pF to 5000 pF capacitors at the CLRCA and CLRCB pins sufficient time to charge for 12-bit accuracy. This guarantees that the LRC's "droop" will be maintained at ≤293 µV**,** thus assuring the specified ADC 12-bit accuracy.

Therefore, at maximum operational frequency (15MHz), the MCM10010 would require sixteen dark pixel samples to establish the dark pixel reference for subsequent active pixel processing.

The dark pixel sample period is controlled through the CLMPE pin. When this pin is active (logic high), each dark pixel is processed and held to establish pixel reference level at the CLRCA and CLRCB pins. The DC Restore Circuit (DCRC) is also activated during this period, and the LRC's differential outputs (V+ and V- on the Diff Amp, Figure 11) are clamped to V_{cm}. Together, these actions help to eliminate the dark level offset, simultaneously establishing the desired zero code at the ADC output.

When the processing of active pixels begins, CLMPE is disabled, halting the charging of the Cap_{LRCA} and Cap_{LRCB} capacitors. The dark pixel reference voltage sampled and held on the capacitors, is then real-time subtracted from the active pixel voltage, yielding an analog signal which has been corrected relative to the desired ADC zero code. This process repeats for each new line scan.

1.5 Digitally Programmable Gain Amplifier (DPGA)

The DPGA circuit allows the user to program gain adjustment of the analog image data via the simple serial interface. The MCM10010 allows up to four gain registers to be individually programmed for a gain range of 0 - 18 dB (1X - 8X) for each register.

Gain is programmable via an 8-bit word.

Four independent registers (Gain Register 1 - 4) are provided to program desired gain coefficients, which are typically Red/Green/Blue (RGB) or Yellow/Cyan/Magenta/Green (Ye/Cy/Mg/G) for color image sensor applications (see Table 2 and the application example in Figure 6).

Each of the four registers can provide eight-bit, incremental gain control from 1X to 8X, in 256 linear increments of 0.0273X such that:

$G = 1 + 0.0273 * (DPGA\ code)_{10}$

of each register (Figure 12).

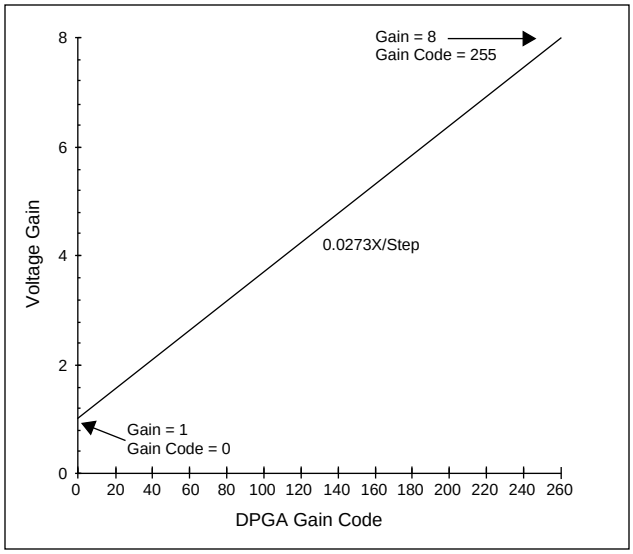


Figure 12. DPGA Gain Plot

Gain register programming information for the DPGA is loaded via the simple serial interface, MSB to LSB, with the register address preceding the 8-bit gain code. The programming summary is shown in Table 2.

Table 2. DPGA Gain Programming Reference

	DPGA Gain Register Code								Address			
	MSB D[7:0] LSB								MSB A[3:0] LSB			
Gain Register	D7	D6	D5	D4	D3	D2	D1	D0	A3	A2	A1	A0
1	X	X	X	X	X	X	X	X	0	0	0	0
2	X = 0 - 255 (0 - 11111111_2)								0	0	0	1
3	X = 0 results in a Gain of 1								0	0	1	0
4	X = 255 results in a Gain of 8								0	0	1	1

The Gain register used by the DPGA are selected via the ISEL0 and ISEL1 input pins as shown in Figure 13.

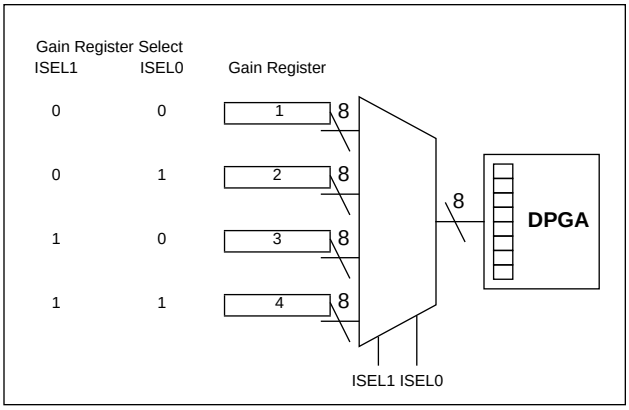


Figure 13. Gain Register Select Logic

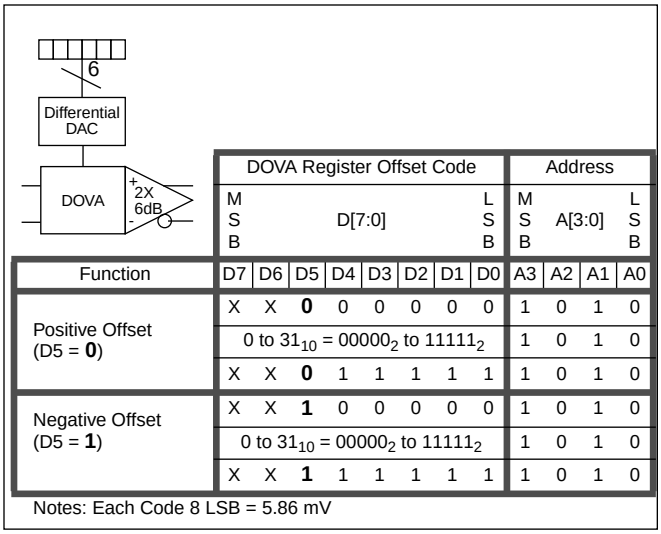
The user may perform real-time updates of any of the gain registers through the simple serial interface. However, a latency associated with the serial register clock rate should be anticipated before the new gain coefficient becomes updated into the DPGA gain register.

All of the DPGA's gain registers power up at a default gain of 1X (0 dB).

For applications which require only a single gain register and only one analog input, the ISEL0/1 pins can be hardwired to the appropriate levels.

1.6 DC Offset Voltage Adjust (DOVA)

The DOVA circuit (Figure 14) provides additional offset control fine-tuning to remove any additional residual error which may have accumulated in the analog signal path. This function may also be used to insert a desired offset of the zero code point in applications where this feature may be desirable, e.g., to adjust for a known system noise floor relative to AV_{SS}. This function is performed directly before analog to digital conversion. A 2.0X (6.0 dB) fixed gain is also introduced in this stage.



Function	DOVA Register Offset Code D7	D6	D5	D4	D3	D2	D1	D0	Address A3	A2	A1	A0
	MSB			D[7:0]				LSB	MSB	A[3:0]		LSB
Positive Offset (D5 = **0**)	X	X	**0**	0	0	0	0	0	1	0	1	0
	0 to 31_{10} = 00000_2 to 11111_2								1	0	1	0
	X	X	**0**	1	1	1	1	1	1	0	1	0
Negative Offset (D5 = **1**)	X	X	**1**	0	0	0	0	0	1	0	1	0
	0 to 31_{10} = 00000_2 to 11111_2								1	0	1	0
	X	X	**1**	1	1	1	1	1	1	0	1	0

Notes: Each Code 8 LSB = 5.86 mV

Figure 14. DOVA Concept Diagram/Programming

The DOVA allows the user to offset the analog signal's voltage via a 6-bit, signed magnitude programming code. The MSB of the six-bit "data" portion of the code represents the sign. A zero (logic low) indicates a positive offset, and a one (logic high) negative, relative to the default zero code point.

The remaining five-bits provide increments of ±5.86 mV (±8 LSB), yielding an effective range of ±181.6 mV (±248 LSB). Programming of the six-bit register is accessed through the simple serial interface.

The preset DOVA code is 000000_2. Adjustment of the voltage offset is real-time programmable, but latency in the simple serial interface is incurred before the new offset becomes valid.

1.7 Analog to Digital Converter (ADC)

The ADC is a 15 MHz, fully differential, twelve bit, low power circuit. A pipelined, Redundant Signed Digit (RSD) algorithmic technique incorporating digital error correction is used to yield an ADC with superior characteristics for imaging applications.

Integral Noise Linearity (INL) and Differential Noise Linearity (DNL) performance is specified at ±2.0 and ±0.8 LSB, respectively, with no missing codes. The input voltage resolution is 0.73 mV with a full-scale 3.0 V_{pp} input (3.0 $V_{pp}/2^{12}$). Two phase clocks are used to reduce ADC latency to 7.5 clock cycles, including latching of the D11:0 outputs to offer the user complete control of the data flow.

1.8 Clocking

Both the Sample&Hold clocks (CDSP1/2) and the Master Clock (MCLK) must be provided externally.

Care must be taken to insure the relative timing between these clocks in relation to the incoming analog data.

2.0 Utility Register Programming

The MCM10010 utilizes a simple serial interface (Figure 15) to program chip control codes for the utility registers, such as DPGA gain coefficients, via a twelve-bit data packet. Each packet consists of a four-bit address and eight additional control data-bits. All programmable features also have default coding or simple pin-level overrides to speed chip initialization, should the user choose to bypass any of them.

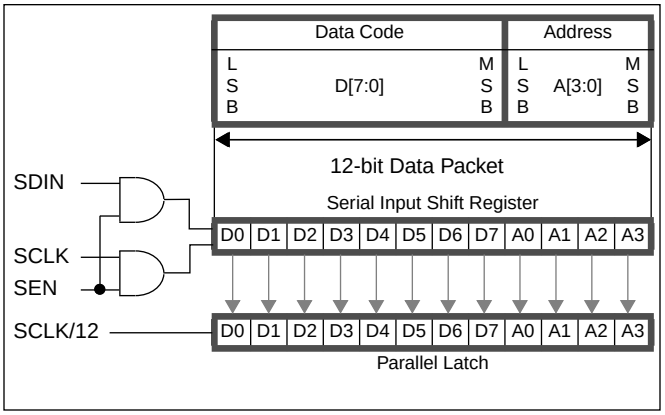


Figure 15. Simple Serial Interface Programming Conceptual Diagram

The interface is controlled by three pins, in which SEN (logic high) gates programming of the interface, SDIN is the serial data input port, and SCLK is the serial clock input (f_{max} = 15 MHz). Table 3 summarizes the program control addresses of the utility registers.

Table 3. Utility Register Programming Address Map

Number of data bits	Register Function								Address			
	MSB D[7:0] LSB								MSB A[3:0] LSB			
	D7	D6	D5	D4	D3	D2	D1	D0	A3	A2	A1	A0
8	DPGA Gain Register 1 Code								0	0	0	0
8	DPGA Gain Register 2 Code								0	0	0	1
8	DPGA Gain Register 3 Code								0	0	1	0
8	DPGA Gain Register 4 Code								0	0	1	1
-	Not used								0	1	0	0
-	Not used								0	1	0	1
-	Not used								0	1	1	0
-	Not used								0	1	1	1
-	Not used								1	0	0	0
-	Not used								1	0	0	1
6	DOVA Offset Voltage Adjust								1	0	1	0
8	Used for test at the factory								1	0	1	1
-	Not used								1	1	0	0
-	Not used								1	1	0	1
-	Not used								1	1	1	0
-	Not used								1	1	1	1

Programming through the simple serial interface is accomplished in three steps (Figure 16). First, the interface is enabled by a low to high transition of the SEN waveform. The SEN waveform must be logic high at least one setup time (t_{suSEN} = 1.0 ns) prior to the first SCLK low to high transition, and it must remain so throughout the data input operation. This action gates the serial interface to accept the SDIN and SCLK inputs.

In the second programming step, data is input in twelve-bit packets through the SDIN pin. Each-bit in the data packet must be valid at least one setup time (t_{suSDIN} = 1.0 ns) before the corresponding SCLK low to high transition. Each-bit must also meet the t_{hSDIN} requirement of 0.5 ns.

Programming codes are input as a four-bit address (A3:A0) input, MSB to LSB, followed by the data (control) code (D7:D0), also MSB to LSB. Any number of registers may be programmed, but data must continue to be input in the twelve-bit format.

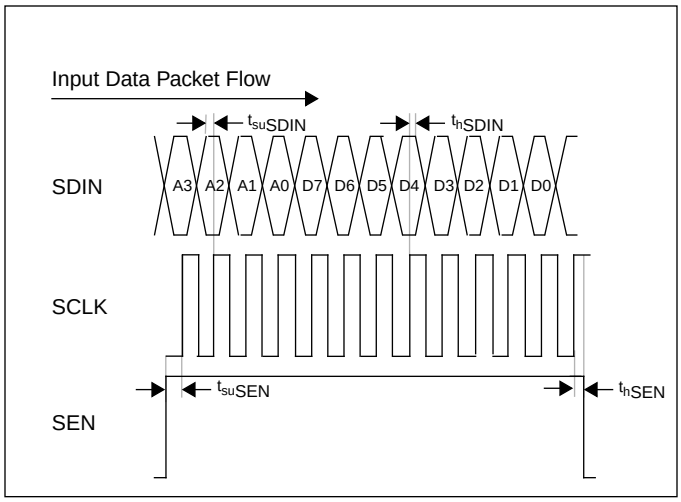


Figure 16. Simple Serial Interface Timing Diagram

The final step of the program register loading procedure terminates the sequence. This action requires that SEN remain high for at least one additional low to high transition of SCLK after the final data-bit has been entered. An additional hold time, t_{hSEN} = 0.5 ns, is also recommended.

Overall, then, SEN must remain high a minimum of (N * 12 + 1) SCLK periods, where N is the number of data packets input, to ensure valid programming of all registers.

The simple serial interface may be used to reprogram the utility registers at any point during operation of the MCM10010, but the user must recognize that all changes incur a latency associated with the serial register and the particular section which is being reprogrammed.

The simple serial interface is write-only. Therefore, utility register programming must be verified in the operating mode by observing the appropriate output characteristic of the MCM10010.

The Test Register at address 1011_2 (11_{10}) is used at the factory to reduce test time and improve fault coverage during device testing. It is loaded with the user mode default value (D[7:0] = 0_{10}) during initialization and should not be addressed in any application.

2.1 Initialization

The INIT input pin controls initialization of the MCM10010 to assure controlled chip and system start-up. Control is asserted via a logic high input. This state must be held a minimum of 1 ms to assure that the start-up routines within the MCM10010 have run properly to completion, as well as guarantee that all holding and bypass capacitors, have achieved their required steady state values.

Tasks which are accomplished during start-up include reset of the utility programming registers and initialization to their default values, reset of all internal counters and latches and setup of the analog signal processing chain.

The DPGA gain is set to 0 dB and the DOVA offset is set to 0 mV.

2.2 Standby Mode

The standby mode option is implemented to allow the user to reduce system power consumption during periods which do not require operation of the MCM10010 for image capture operations in the system. This feature allows the user to extend battery life in low power applications.

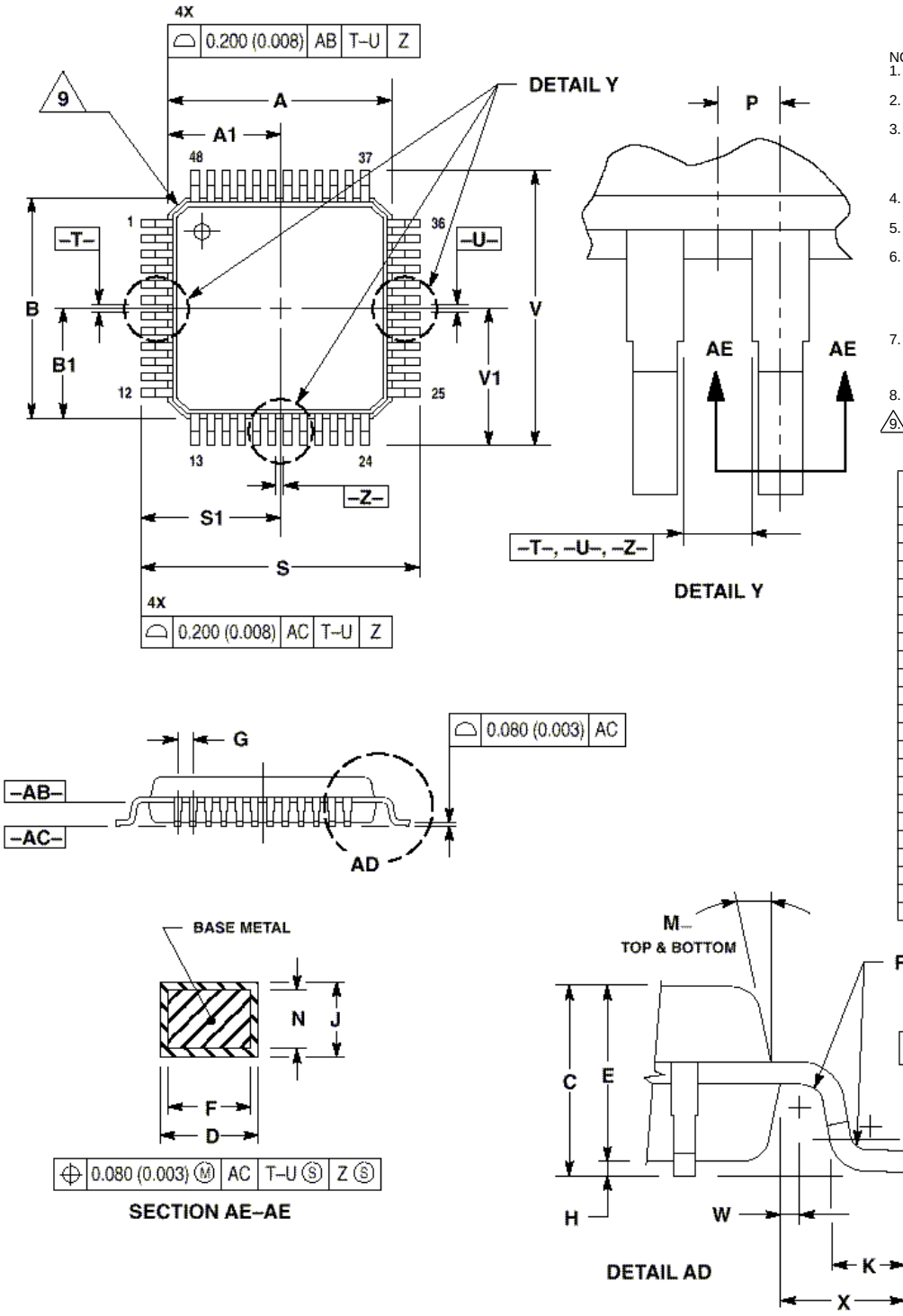
By utilizing this mode, the user may reduce dynamic power consumption from 275 mW, in the active processing, 15 MSPS mode, to ≤25 mW in the standby mode (note that dynamic power consumption is also reduced in slower conversion speed applications).

The standby mode is activated by applying an active high signal to the STDBY pin. This function places the ADC[11:0] outputs in the three-state mode.

The user may also reduce power consumption in the active processing mode by placing the MCM10010's outputs in the three-state mode. This action may be accomplished by placing the TS pin in the active high state.

2.3 References CVREFP,CVREFM

The ADC references, CVREFP and CVREFM, are available at package pins for external decoupling for added stability. A 1µF capacitor to ground, from each pin, is recommended.



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER
3. DATUM PLANE-AB-IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -T-, -U-, AND -Z- TO BE DETERMINED AT DATUM PLANE -AB-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -AC-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE, DIMENSIONS A AND B DO NOT INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -AB-.
7. DIMENSION O DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMNESION TO EXCEED 0.350 (0.014).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.170	0.270	0.007	0.011
E	1.350	1.450	0.053	0.057
F	0.170	0.230	0.007	0.009
G	0.500 BASIC		0.020 BASIC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.250 BASIC		0.010 BASIC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.060	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

Figure 17. 48 Lead LQFP (Case Outline 932-02)

Notes:

Note: For the most current information regarding this product, contact Motorola on the World Wide Web at http://sps.motorola.com/consumer-solutions/

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MFax™: RMFAX0@email.sps.mot.com -TOUCHTONE (602) 244-6609

HOME PAGE:http://motorola.com/sps/

JAPAN: Nippon Motorola Ltd.: SPD, Strategic Planning Office, 141, 4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan .81-3-5487-8488

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

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