Octal Ultrasound AFE with Digital Demodulator

Data Sheet

AD9674

FEATURES

- 8 channels of LNA, VGA, AAF, ADC, and digital RF decimator
  - Low power: 150 mW per channel, TGC mode, 40 MSPS; 65 mW per channel, CW mode; <30 mW at power-up
  - Time gain compensation (TGC) channel input-referred noise: 0.8 nV/√Hz, maximum gain
  - Flexible power-down modes
  - Fast recovery from low power standby mode: <2 µs
- Low noise preamplifier (LNA)
  - Input-referred noise voltage: 0.78 nV/√Hz, gain = 21.6 dB
  - Programmable gain: 15.6 dB/17.9 dB/21.6 dB
  - 0.1 dB compression: 1.00 V p-p/0.75 V p-p/0.45 V p-p
  - Flexible active input impedance matching
- Variable gain amplifier (VGA)
  - Attenuator range: 45 dB, linear-in-dB gain control
  - Postamp gain: 21 dB/24 dB/27 dB/30 dB
- Antialiasing filter (AAF)
  - Programmable second-order low-pass filter (LPF) from 8 MHz to 18 MHz or 13.5 MHz to 30 MHz and high-pass filter (HPF)
- Analog-to-digital converter (ADC)
  - Signal-to-noise ratio (SNR): 75 dB, 14 bits up to 125 MSPS
- Configurable serial low voltage differential signaling (LVDS)
- Continuous wave (CW) doppler mode harmonic rejection I/Q demodulator
  - Individual programmable phase rotation
  - Dynamic range per channel: >160 dBFS/√Hz
  - Close-in SNR: 156 dBc/√Hz, 1 kHz offset, −3 dBFS input
- RF digital HPF and decimation by 2
- 10 mm × 10 mm, 144-ball CSP_BGA

GENERAL DESCRIPTION

The AD9674 is designed for low cost, low power, small size, and ease of use for medical ultrasound. It contains eight channels of a VGA with an LNA, a CW harmonic rejection I/Q demodulator with programmable phase rotation, an AAF, an ADC, a digital HPF, and RF decimation by 2.

Each channel features a maximum gain of up to 52 dB, a fully differential signal path, and an active input preamplifier termination. The channel is optimized for high dynamic performance and low power in applications where a small package size is critical.

The LNA has a single-ended-to-differential gain that is selectable through the serial port interface (SPI). Assuming a 15 MHz noise bandwidth (NBW) and a 21.6 dB LNA gain, the LNA input SNR is 94 dB. In CW doppler mode, each LNA output drives an I/Q demodulator that has independently programmable phase rotation with 16 phase settings.

Power-down of individual channels is supported to increase battery life for portable applications. Standby mode allows quick power-up for power cycling. In CW doppler operation, the VGA, AAF, and ADC are powered down. The ADC contains several features designed to maximize flexibility and minimize system cost, such as a programmable clock, data alignment, and programmable digital test pattern generation. The digital test patterns include built-in fixed patterns, built-in pseudorandom patterns, and custom user-defined test patterns entered via the serial port interface. This product is protected by a U.S. patent.

FUNCTIONAL BLOCK DIAGRAM

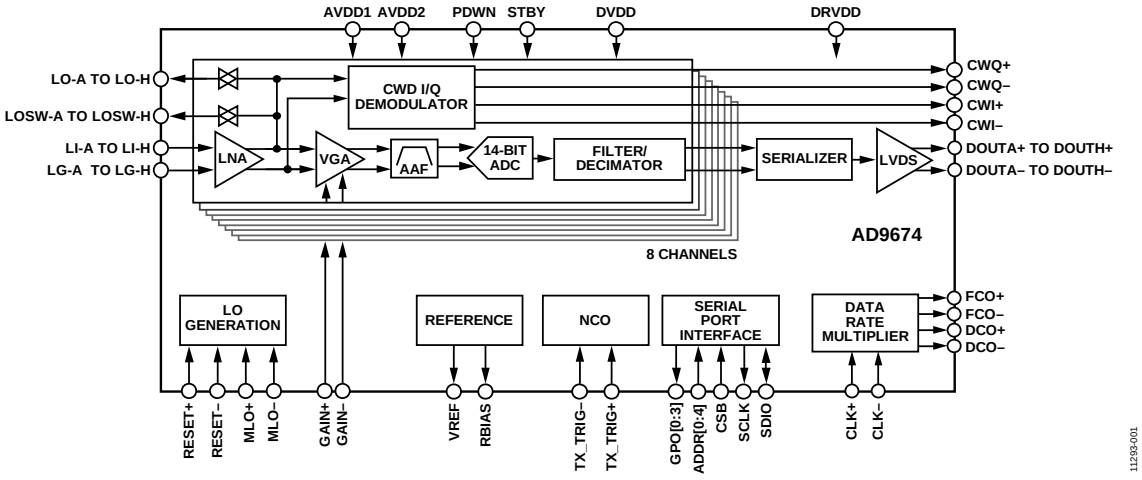

Figure 1.

For more information about the AD9674, contact Analog Devices, Inc., at Highspeed.converters@analog.com.

Rev. Sp0 **Document Feedback**

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NOTES

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