

SN54ALS666, SN54ALS667, SN74ALS666, SN74ALS667 8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES WITH 3-STATE OUTPUTS

D2855, JUNE 1984 - REVISED MAY 1986

- 3-State I/O-Type Read-Back Inputs
- Bus-Structured Pinout
- Choice of True or Inverting Logic
'ALS666 . . . True Outputs
'ALS667 . . . Inverting Outputs
- Preset and Clear Inputs
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

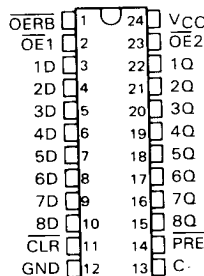
These 8-bit latches are designed specifically for storing the contents of the input data bus plus providing the capability of reading-back the stored data onto the input data bus. In addition, they provide a 3-state buffer type output and are easily utilized in bus-structured applications.

The eight latches of the 'ALS666 and 'ALS667 are transparent D-type. While the enable (C) is high, the Q outputs of the 'ALS666 will follow the data (D) inputs. On the 'ALS667, the $\bar{Q}$ outputs will provide the inverse of what is applied to its data (D) inputs. On both devices, the Q or $\bar{Q}$ output will be in the high-impedance state if either output control, OE1 or OE2, is at a high logic level.

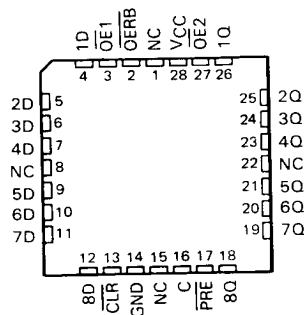
Read-back is provided thru the read-back control input (OERB). When OERB is taken low, the data present at the output of the data latches will be allowed to pass back onto the input data bus. When it is taken high, the output of the data latches will be isolated from the data (D) inputs. The read-back control does not affect the internal operation of the latches; however, caution should be exercised not to create a bus-conflict situation.

The SN54ALS666 and SN54ALS667 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS666 and SN75ALS667 are characterized for operation from 0°C to 70°C .

SN54ALS666 . . . JT PACKAGE
SN74ALS666 . . . DW OR NT PACKAGE
(TOP VIEW)



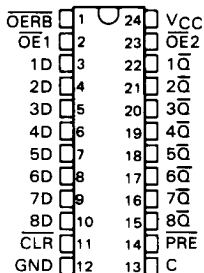
SN54ALS666 . . . FK PACKAGE
SN74ALS666 . . . FN PACKAGE
(TOP VIEW)



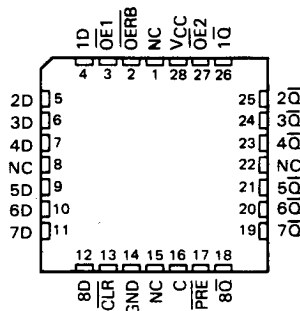
NC - No internal connection.

SN54ALS666, SN54ALS667, SN74ALS666, SN74ALS667 **8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES** **WITH 3-STATE OUTPUTS**

SN54ALS667 . . . JT PACKAGE
 SN74ALS667 . . . DW OR NT PACKAGE
 (TOP VIEW)

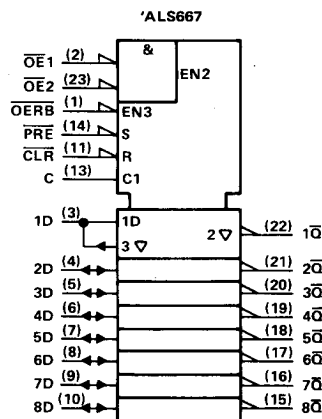
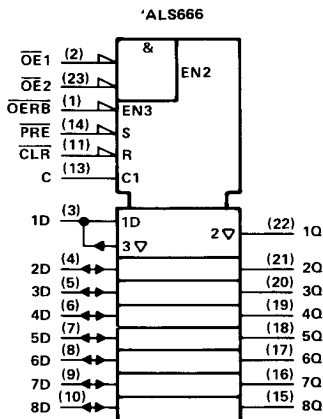


SN54ALS667 . . . FK PACKAGE
 SN74ALS667 . . . FN PACKAGE
 (TOP VIEW)



NC—No internal connection.

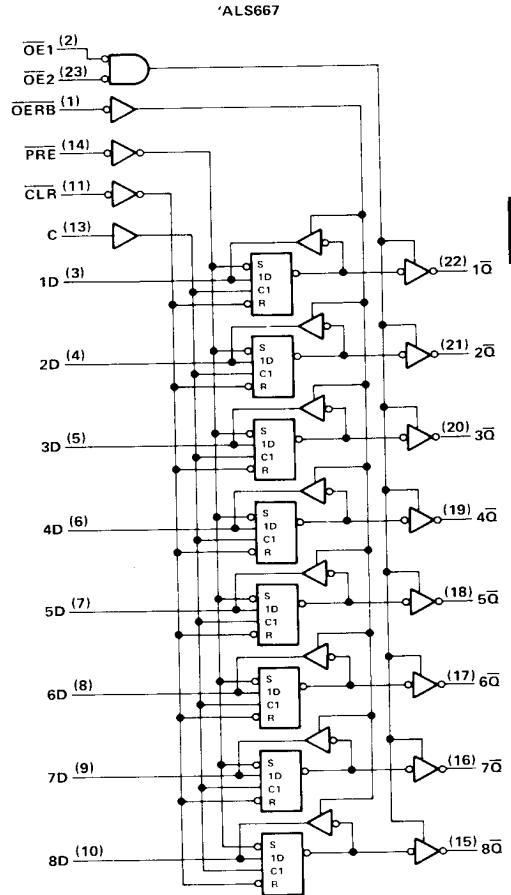
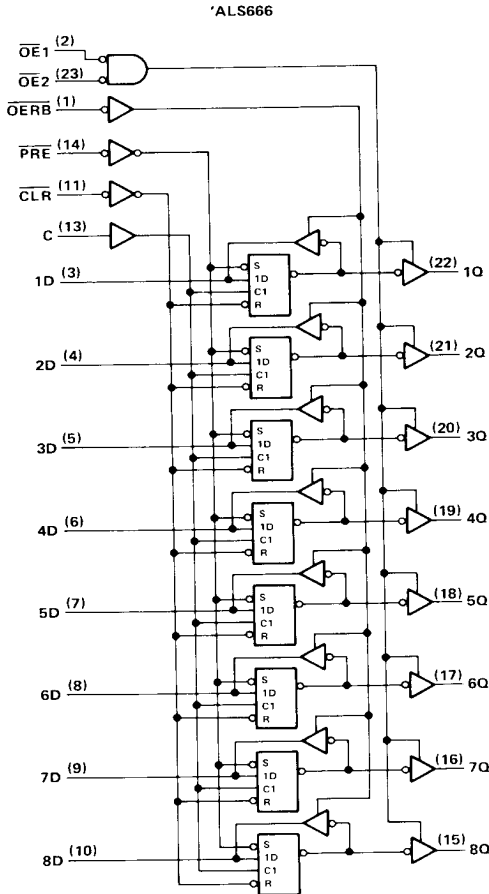
logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.

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8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES
WITH 3-STATE OUTPUTS

logic diagrams (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

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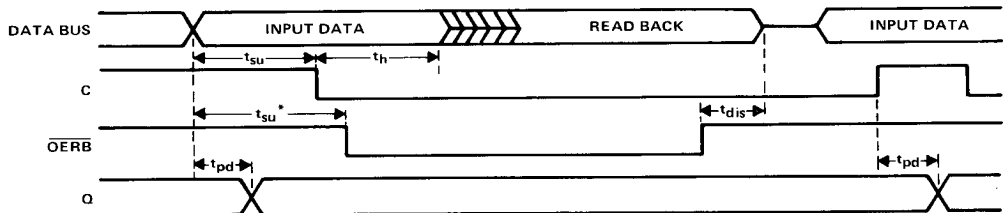
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SN54ALS666, SN54ALS667, SN74ALS666, SN74ALS667 **8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES** **WITH 3-STATE OUTPUTS**

timing diagram



CLR = H, PRE = H, OE1 = L, OE2 = L

*This setup time ensures the readback circuit will not create a conflict on the input data bus.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC}	7 V
Input voltage (all inputs except D input)	7 V
Voltage applied to D inputs and to disabled 3-state outputs	5.5 V
Operating free-air temperature range: SN54ALS666, SN54ALS667	–55°C to 125°C
SN74ALS666, SN74ALS667	0°C to 70°C
Storage temperature range	–65°C to 150°C

recommended operating conditions

			SN54ALS666			SN74ALS666			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.7			0.8	V
I _{OH}	High-level output current	Q			–1			–2.6	mA
		D			0.4			0.4	
I _{OL}	Load-level output current	Q			12			24	mA
		D			4			8	
t _w	Pulse duration	Enable C high	15			10			ns
		CLR low	10			10			
		PRE low	10			10			
t _{su}	Setup time	Data before C.	15			10			ns
		Data before OERB.	15			10			
t _h	Hold time	Data after C.	10			5			ns
T _A	Operating free-air temperature		55		125	0		70	°C

SN54ALS666, SN54ALS667, SN74ALS666, SN74ALS667

8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES

WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ALS666 SN54ALS667			SN74ALS666 SN74ALS667			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = -18 mA	-1.2			-1.2			V
V _{OH}	All outputs	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA	V _{CC} - 2			V _{CC} - 2			V
	Q or Q̄	V _{CC} = 4.5 V, I _{OH} = -1 mA	2.4	3.3		2.4	3.2		
V _{OL}	D	V _{CC} = 4.5 V, I _{OH} = -2.6 mA							V
		V _{CC} = 4.5 V, I _{OL} = 4 mA	0.25	0.4		0.25	0.4		
	V _{CC} = 4.5 V, I _{OL} = 8 mA				0.35 0.5				
	Q or Q̄	V _{CC} = 4.5 V, I _{OL} = 12 mA	0.25	0.4		0.25	0.4		
		V _{CC} = 4.5 V, I _{OL} = 24 mA				0.35 0.5			
I _{OZH}	Q or Q̄	V _{CC} = 5.5 V, V _O = 2.7 V	20			20			μA
I _{OZL}		V _{CC} = 5.5 V, V _O = 0.4 V	-20			-20			
I _I	D inputs	V _{CC} = 5.5 V, V _I = 5.5 V	0.1			0.1			mA
	All others	V _{CC} = 5.5 V, V = 7 V	0.1			0.1			
I _{IH}	D inputs†	V _{CC} = 5.5 V, V = 2.7 V	20			20			μA
	All others		20			20			
I _{IL}	D inputs†	V _{CC} = 5.5 V, V _I = 0.4 V	-0.1			-0.1			mA
	All others		-0.1			-0.1			
I _O ‡		V _{CC} = 5.5 V, V _O = 2.25 V	-30		-112	-30		-112	mA
I _{CC}	'ALS666	V _{CC} = 5.5 V, O _{ERB} high	Q outputs high		25 50	25 50		mA	
			Q outputs low		40 73	40 73			
			Q outputs disabled		30 55	30 55			
	'ALS667		Q̄ outputs high		25 50	25 50			
			Q̄ outputs low		45 79†	45 79			
			Q̄ outputs disabled		30 60	30 60			

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

† For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit output currents, I_{OS} .

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8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES
WITH 3-STATE OUTPUTS

***ALS666 switching characteristics (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, T _A = MIN to MAX			UNIT	
			ALS666			SN54ALS666		SN74ALS666		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
t _{PLH}	D	Q		7	10	3	18✓	3	14	ns
t _{PHL}				11	15	4	22✓	4	18	
t _{PLH}	C	Q		12	16	6	25	6	21	ns
t _{PHL}				16	21	8	32✓	8	27	
t _{PLH}	CLR	Q		17	22	9	32	9	29	ns
t _{PHL}		D		17	24	11	36	11	32	
t _{PLH}	PRE	Q		13	18	7	28✓	7	22	ns
t _{PHL}		D		17	22	9	35	9	28	
t _{en}	OR _B	D		11	17	4	25✓	4	21	ns
t _{dis}				6	11	1	18✓	1	14	
t _{en}	OE1, OE2	Q		11	17	4	25✓	4	21	ns
t _{dis}				6	11	1	18✓	1	14	

***ALS667 switching characteristics (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, T _A = MIN to MAX				UNIT
			'ALS667			SN54ALS667		SN74ALS667		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	D	$\overline{Q}$		13	17	6	24	6	20	ns
t _{PHL}				9	13	4	18	4	15	
t _{PLH}	C	$\overline{Q}$		18	23	9	35	9	28	ns
t _{PHL}				14	19	7	27	7	22	
t _{PLH}	$\overline{CLR}$	$\overline{Q}$		14	19	7	28	7	24	ns
t _{PHL}		D		17	23	8	30	8	26	
t _{PHL}	$\overline{PRE}$	$\overline{Q}$		17	23	8	30	8	25	ns
t _{PLH}		D		18	25	9	35	9	28	
t _{en}	$\overline{OERB}$	D		11	17	4	25	4	21	ns
t _{dis}				6	11	1	20	1	14	
t _{en}	$\overline{OE1}, \overline{OE2}$	$\overline{Q}$		11	17	4	25	4	21	ns
t _{dis}				6	11	1	20	1	14	

t_{en} = t_{PZH} or t_{PZL}
t_{dis} = t_{PHZ} or t_{PLZ}

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8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES
WITH 3-STATE OUTPUTS

PARAMETER MEASUREMENT INFORMATION

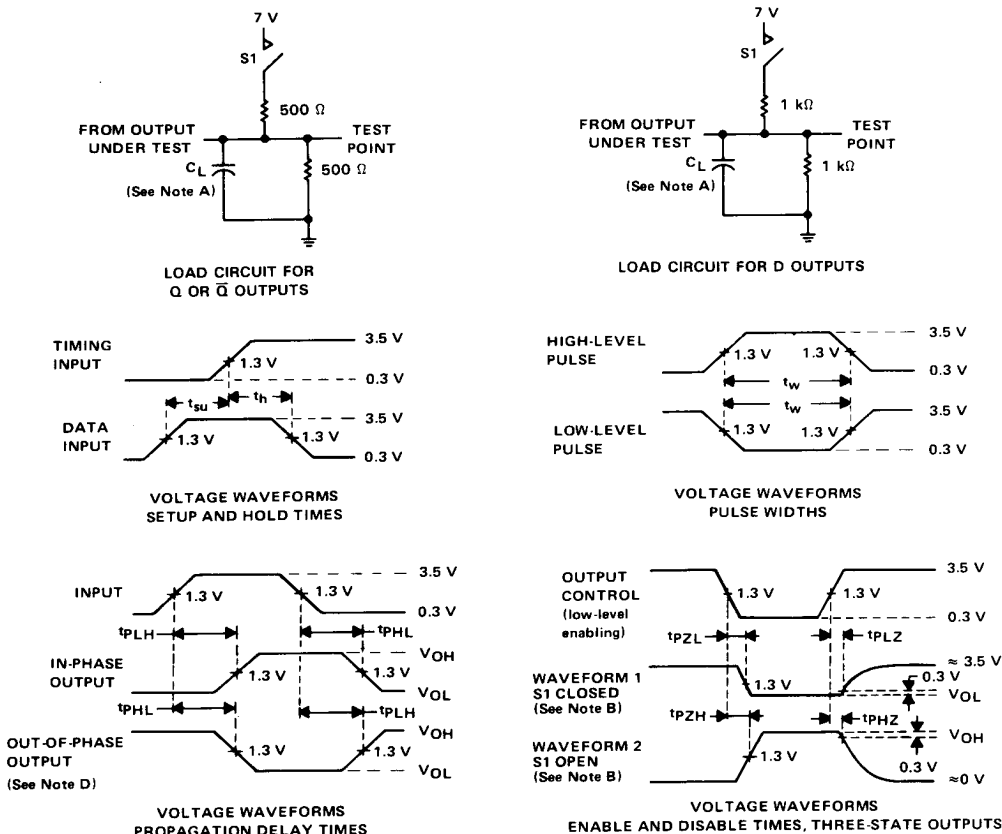


FIGURE 1