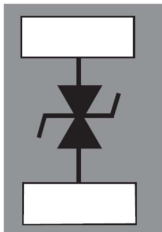


## 3.3 V ultra-low clamping single line bidirectional ESD protection



ST0201 package



### Features

- Ultra-low clamping voltage: 6.3 V TLP at 16 A  $I_{pp}$
- Bidirectional protection diode
- Very low dynamic resistance: 85 m $\Omega$
- Low leakage current: 100 nA max at 3.3 V  $V_{RM}$
- ST0201 package
- [ECOPACK2](#) compliant component
- Exceeds IEC 61000-4-2 level 4:
  - $\pm 25$  kV (contact discharge)
  - $\pm 30$  kV (air discharge)

### Application

Where transient over voltage protection in ESD sensitive equipment is required, such as:

- Smartphones, mobile phones and accessories
- Tablets and notebooks
- Portable multimedia devices and accessories
- Wearable, home automation, healthcare
- Highly integrated systems

Product status link

[ESDL031-1BF4](#)

### Description

The [ESDL031-1BF4](#) is a bidirectional single line TVS diode designed to protect the power line against EOS and ESD transients.

The device is ideal for applications where board space saving is required.

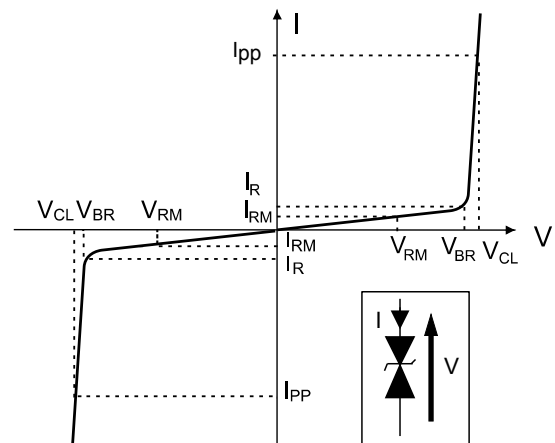
# 1 Characteristics

**Table 1. Absolute maximum ratings ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ )**

Symbol	Parameter		Value	Unit
$V_{pp}$	Peak pulse voltage	IEC 61000-4-2 contact discharge	$\pm 25$	kV
		IEC 61000-4-2 air discharge	$\pm 30$	
$P_{pp}$	Peak pulse power (8/20 $\mu\text{s}$ )		45	W
$I_{pp}$	Peak pulse current (8/20 $\mu\text{s}$ )		7	A
$T_j$	Operating junction temperature range		-55 to 150	$^{\circ}\text{C}$
$T_{stg}$	Storage junction temperature range		-65 to 150	
$T_L$	Maximum lead temperature for soldering during 10 s		260	

**Figure 1. Electrical characteristics (definitions)**

Symbol	Parameter
$V_{BR}$	= Breakdown voltage
$I_R$	= Breakdown current
$V_{CL}$	= Clamping voltage
$I_{RM}$	= Leakage current at $V_{RM}$
$V_{RM}$	= Stand-off voltage
$I_{PP}$	= Peak pulse current
$R_D$	= Dynamic resistance

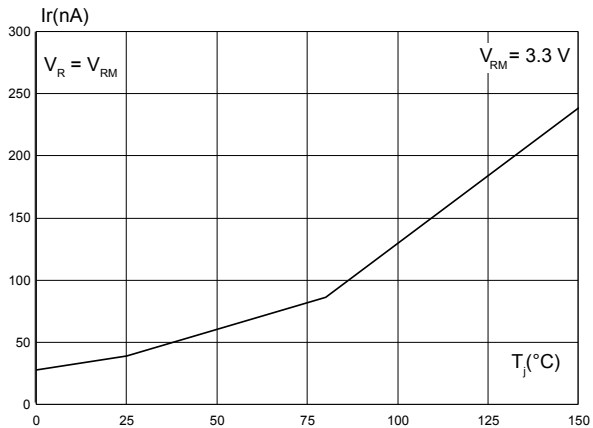


**Table 2. Electrical characteristics (values) ( $T_{amb} = 25^{\circ}C$ )**

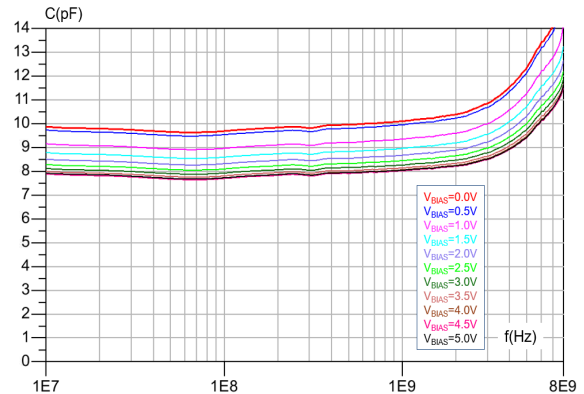
Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{RM}$	Reverse working voltage				3.3	V
$V_{BR}$	Breakdown voltage	$I_R = 1\text{ mA}$	5.0	5.5	6.6	V
$I_{RM}$	Leakage current	$V_{RM} = 3.3\text{ V}$		30	100	nA
$V_{CL}$	Reverse clamping voltage	$I_{pp} = 7\text{ A} - 8/20\mu\text{s}$			7	V
$V_{CL}$	Reverse clamping voltage	8 kV contact discharge after 30 ns, IEC 61000-4-2		6.6		V
$V_{CL}$	Reverse clamping voltage	TLP measurement (pulse duration 100 ns)	$I_{pp} = 4\text{ A}$	5.2		V
			$I_{pp} = 16\text{ A}$	6.3		
$R_D$	Dynamic resistance, TLP pulse duration 100 ns (from 4 A to 16 A $I_{pp}$ )			85		m $\Omega$
$C_{LINE}$	Line capacitance	$V_{LINE} = 0\text{ V}$ , $F = 1\text{ MHz}$ , $V_{OSC} = 30\text{ mV}$		10	12	pF

## 1.1 Characteristics (curves)

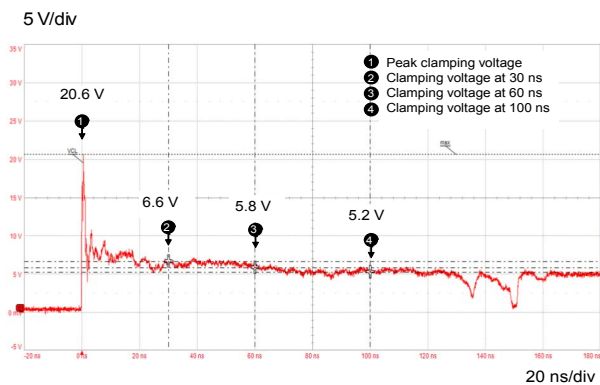
**Figure 2. Leakage current versus junction temperature (typical values)**



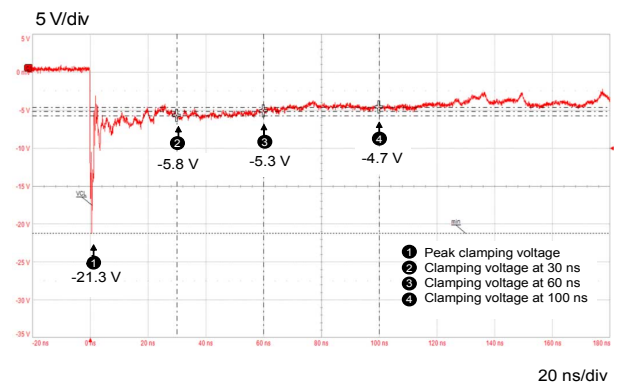
**Figure 3. Junction capacitance versus applied voltage (typical values)**



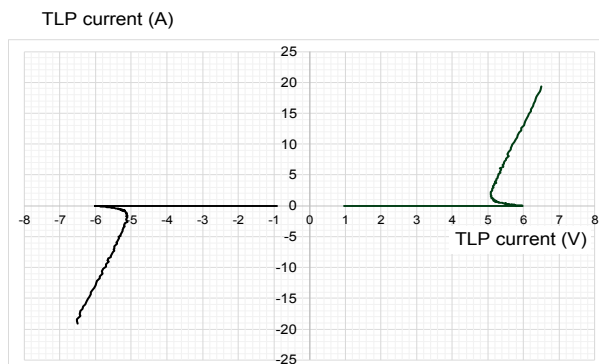
**Figure 4. ESD response to IEC 61000-4-2 (+8 kV contact discharge)**



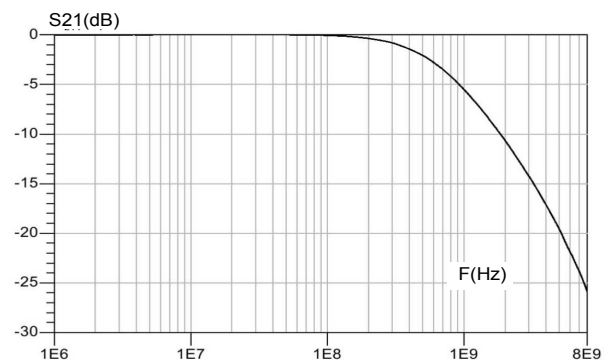
**Figure 5. ESD response to IEC 61000-4-2 (-8 kV contact discharge)**



**Figure 6. TLP characteristic**



**Figure 7. S21 attenuation measurement result**

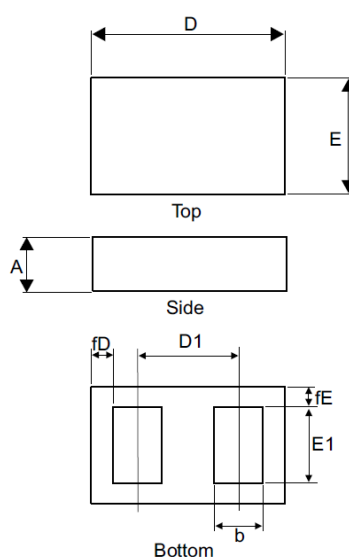


## 2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 2.1 ST0201 package information

**Figure 8. ST0201 package outline**

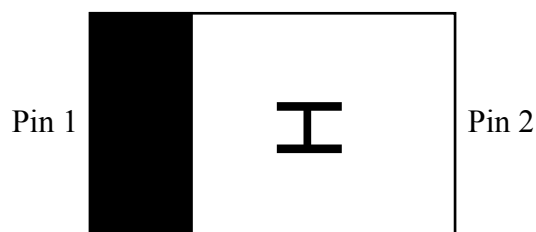


**Note:** The marking codes can be rotated by 90° or 180° to differentiate assembly location. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

**Table 3. 0201 package mechanical data**

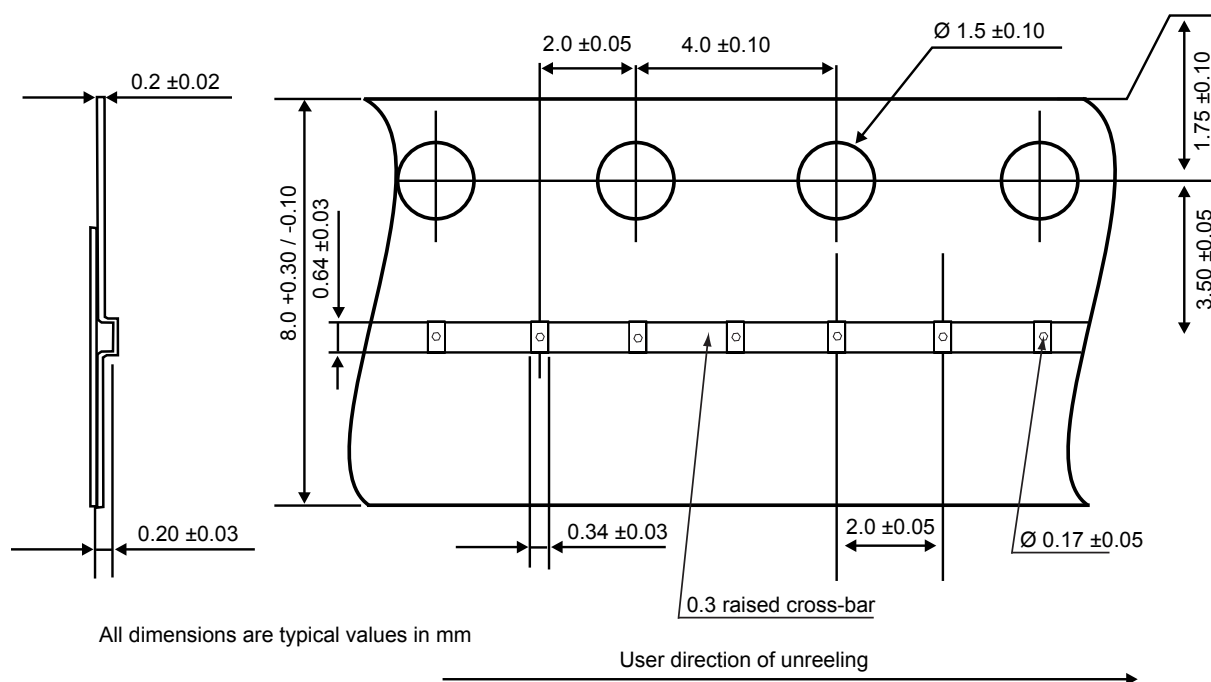
Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	0.130	0.150	0.170
b	0.1675	0.1875	0.2075
D	0.560	0.580	0.600
D1		0.3375	
E	0.260	0.280	0.300
E1	0.205	0.225	0.245
fD	0.0175	0.0275	0.0375
fE	0.0175	0.0275	0.0375

Figure 9. Marking



**Note:** The marking codes can be rotated by 90° or 180° to differentiate assembly location. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Figure 10. Tape and reel specification (in mm)

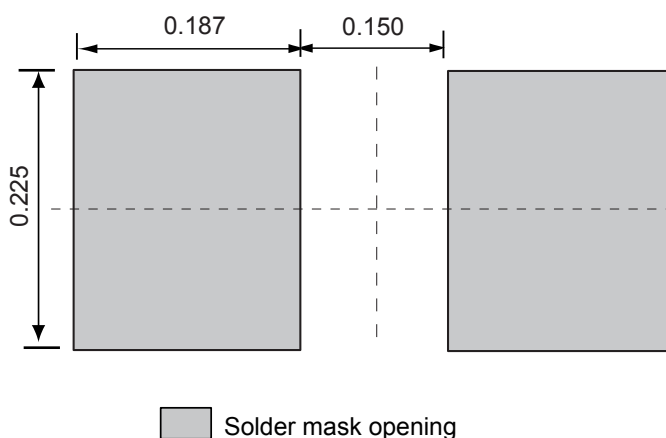


### 3 Recommendation on PCB assembly

#### 3.1 Footprint

1. SMD footprint design is recommended

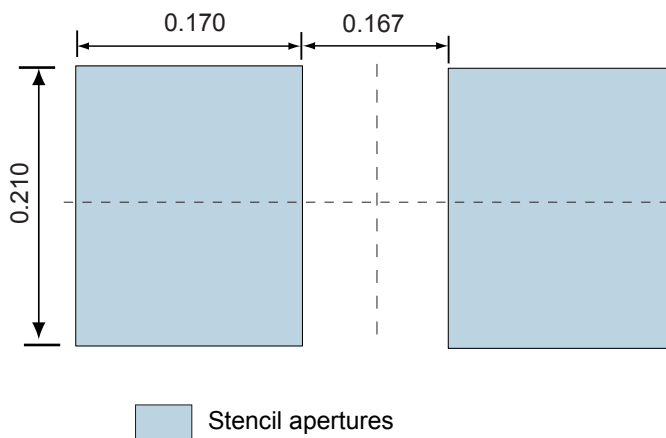
**Figure 11. Footprint in mm**



#### 3.2 Stencil opening design

1. Recommended design reference
  - a. Stencil opening dimensions: 75  $\mu\text{m}$  / 3 mils
  - b. Stencil aperture ratio : 100%

**Figure 12. Stencil opening recommendations**



### 3.3 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. "No clean" solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Use solder paste with fine particles: powder particle size 20-38  $\mu\text{m}$ .

### 3.4 Placement

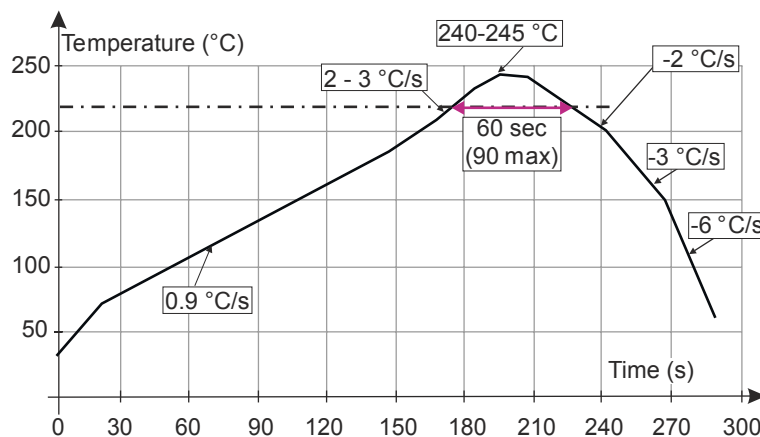
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of  $\pm 0.05$  mm is recommended.
4. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

### 3.5 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

### 3.6 Reflow profile

**Figure 13. ST ECOPACK® recommended soldering reflow profile for PCB mounting**



**Note:** Minimize air convection currents in the reflow oven to avoid component movement. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.



## 4 Ordering information

Figure 14. Ordering information scheme

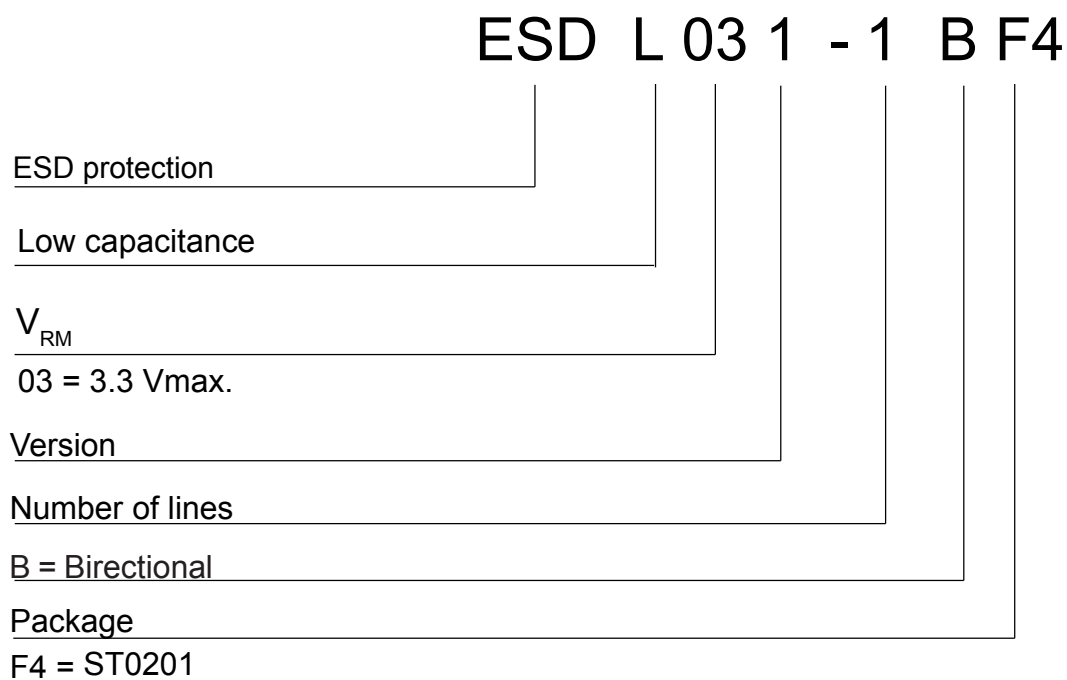


Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
ESDL031-1BF4	H	ST0201	0.116 mg	15000	Tape and reel

## Revision history

**Table 5. Document revision history**

Date	Revision	Changes
24-Sep-2019	1	First issue.

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