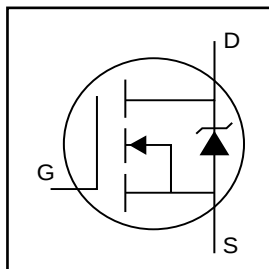


- Surface Mount (IRF640S)
- Low-profile through-hole (IRF640L)
- Available in Tape & Reel (IRF640S)
- Dynamic dv/dt Rating
- 150°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated



$$V_{DS} = 200V$$

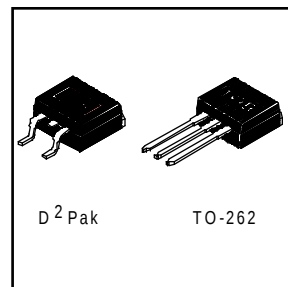
$$R_{DS(on)} = 0.18\Omega$$

$$I_D = 18A$$

Description

Third generation HEXFETs from international Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application. The through-hole version (IRF640L) is available for low-profile applications.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ⑤	18	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ⑤	11	
I_{DM}	Pulsed Drain Current ①⑤	72	
$P_D @ T_A = 25^\circ C$	Power Dissipation	3.1	W
$P_D @ T_C = 25^\circ C$	Power Dissipation	130	W
	Linear Derating Factor	1.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②⑤	580	mJ
I_{AR}	Avalanche Current①	18	A
E_{AR}	Repetitive Avalanche Energy①	13	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	5.0	V/ns
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.0	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted, steady-state)**	—	40	

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.29	—	V/°C	Reference to 25°C , $I_D = 1mA$ ⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.18	Ω	$V_{GS} = 10V, I_D = 11A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	6.7	—	—	S	$V_{DS} = 50V, I_D = 11A$ ⑤
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 200V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 160V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
Q_g	Total Gate Charge	—	—	70	nC	$I_D = 18A$
Q_{gs}	Gate-to-Source Charge	—	—	13		$V_{DS} = 160V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	39		$V_{GS} = 10V$, See Fig. 6 and 13 ④⑤
$t_{d(on)}$	Turn-On Delay Time	—	14	—	ns	$V_{DD} = 100V$
t_r	Rise Time	—	51	—		$I_D = 18A$
$t_{d(off)}$	Turn-Off Delay Time	—	45	—		$R_G = 9.1\Omega$
t_f	Fall Time	—	36	—		$R_D = 5.4\Omega$, See Fig. 10 ④⑤
L_S	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C_{iss}	Input Capacitance	—	1300	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	430	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	130	—		$f = 1.0MHz$, See Fig. 5⑤

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	18	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	72		
V_{SD}	Diode Forward Voltage	—	—	2.0	V	$T_J = 25^\circ\text{C}, I_S = 18A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	300	610	ns	$T_J = 25^\circ\text{C}, I_F = 18A$
Q_{rr}	Reverse Recovery Charge	—	3.4	7.1	μC	$di/dt = 100A/\mu s$ ④⑤
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② $V_{DD} = 50V$, starting $T_J = 25^\circ\text{C}$, $L = 2.7mH$
 $R_G = 25\Omega$, $I_{AS} = 18A$. (See Figure 11)
- ③ $I_{SD} \leq 18A$, $di/dt \leq 150A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 150^\circ\text{C}$
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ⑤ Uses IRF640 data and test conditions

** When mounted on 1" square PCB (FR-4 or G-10 Material).

For recommended footprint and soldering techniques refer to application note #AN-994.

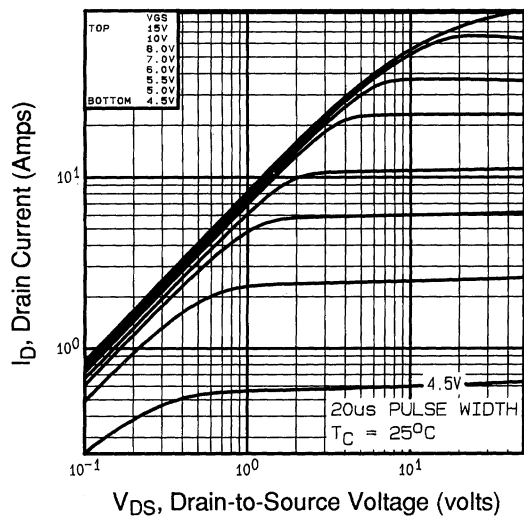


Fig 1. Typical Output Characteristics,

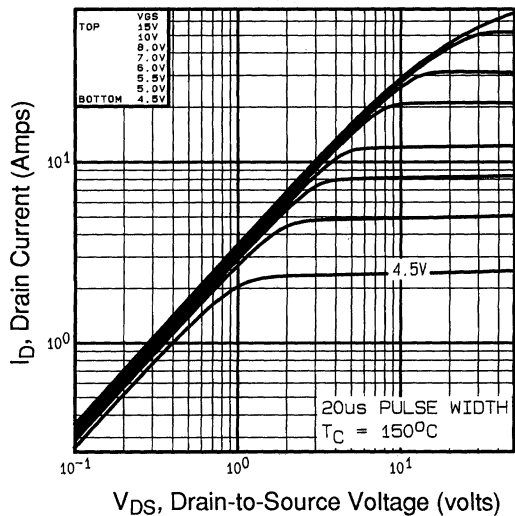


Fig 2. Typical Output Characteristics,

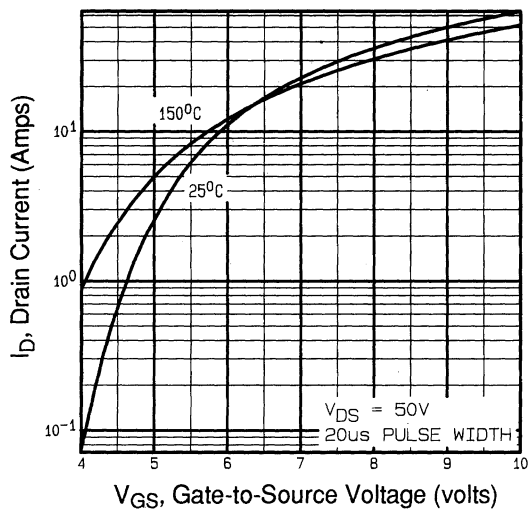


Fig 3. Typical Transfer Characteristics

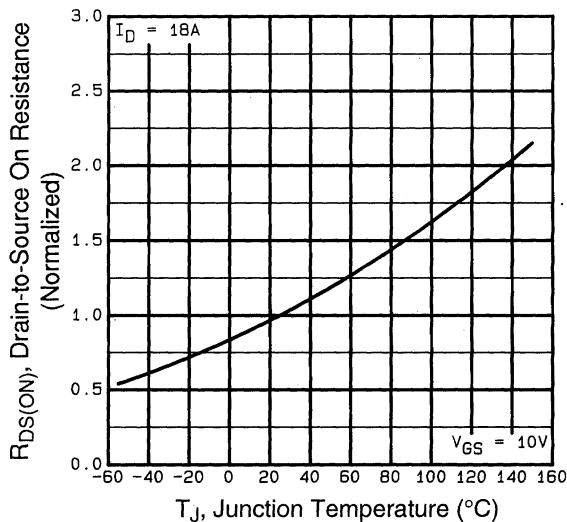


Fig 4. Normalized On-Resistance
Vs. Temperature

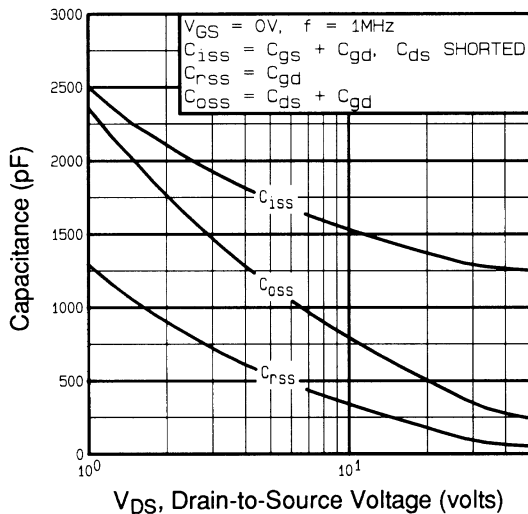


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

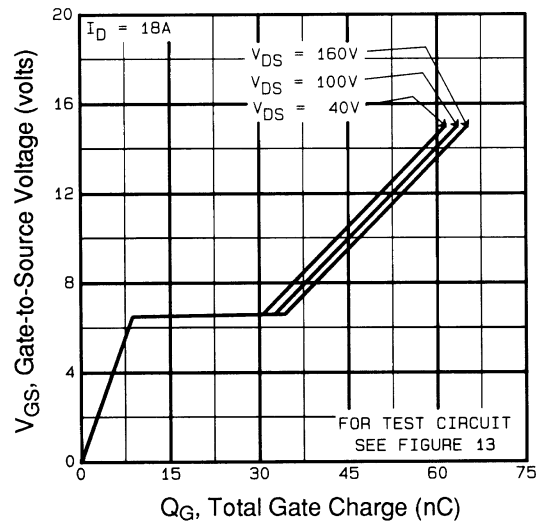


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

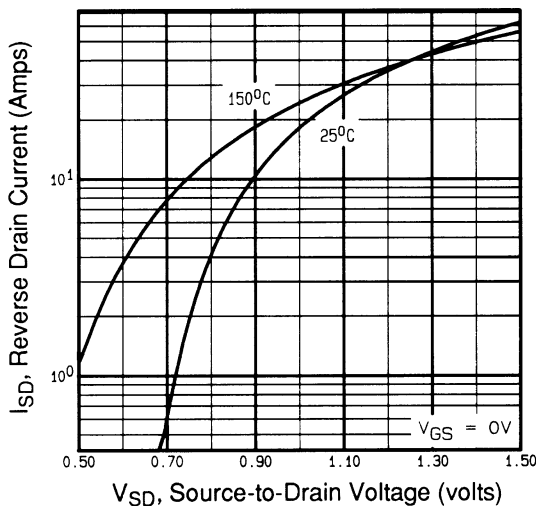


Fig 7. Typical Source-Drain Diode Forward Voltage

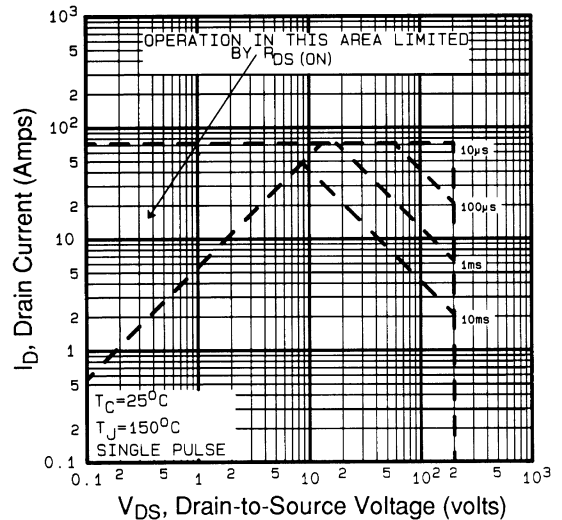


Fig 8. Maximum Safe Operating Area

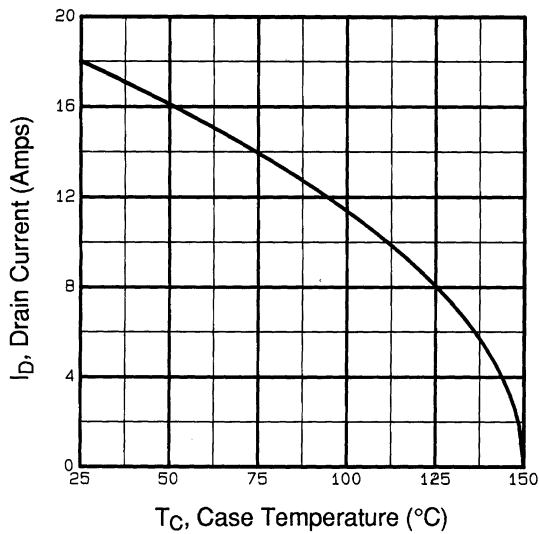


Fig 9. Maximum Drain Current Vs. Case Temperature

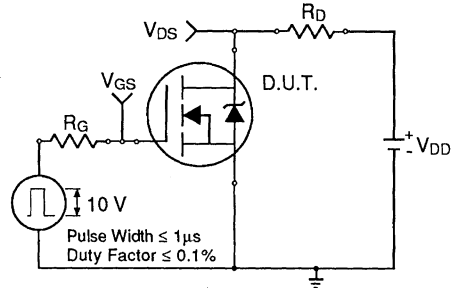


Fig 10a. Switching Time Test Circuit

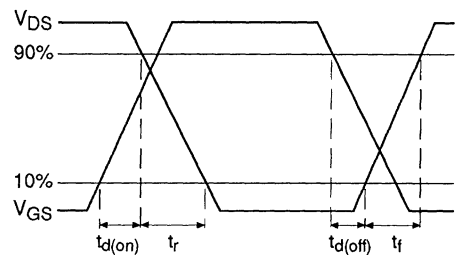


Fig 10b. Switching Time Waveforms

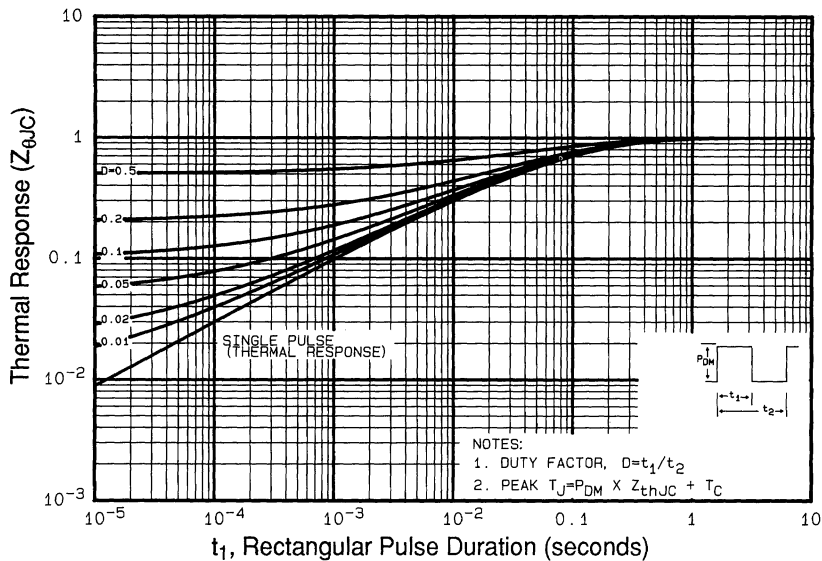


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

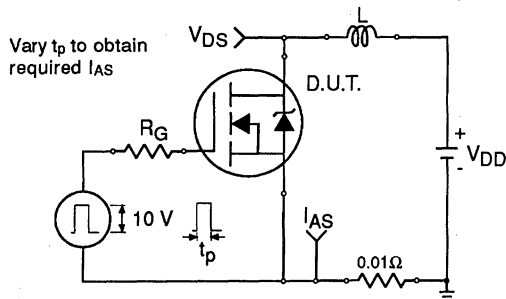


Fig 12a. Unclamped Inductive Test Circuit

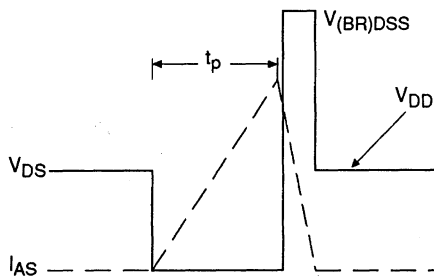


Fig 12b. Unclamped Inductive Waveforms

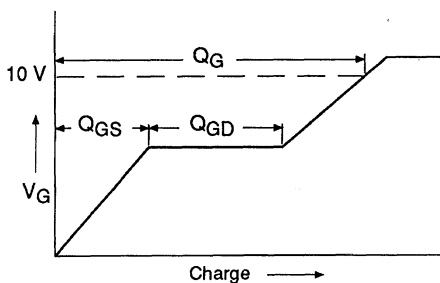


Fig 13a. Basic Gate Charge Waveform

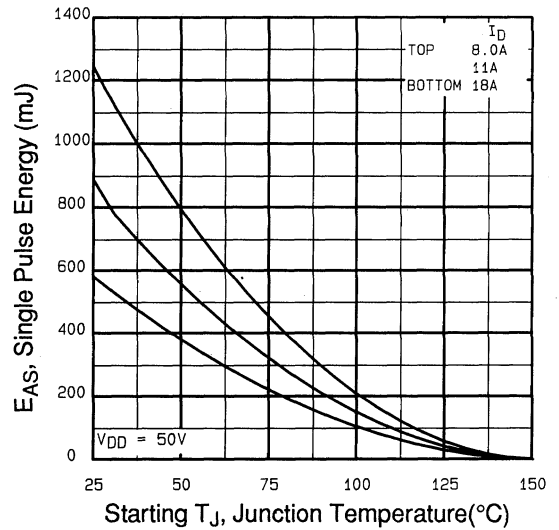


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

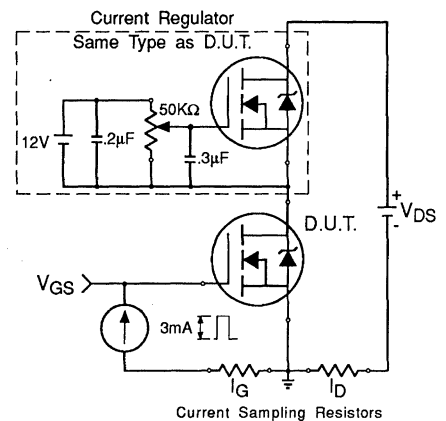
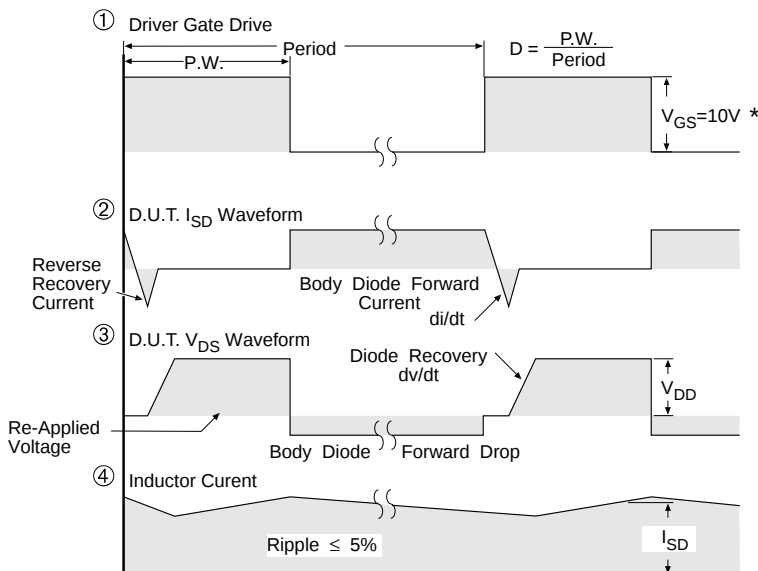
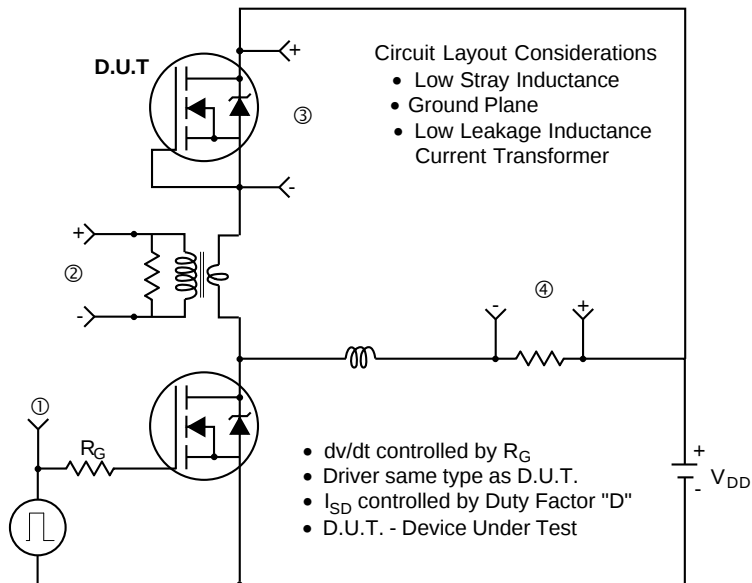


Fig 13b. Gate Charge Test Circuit

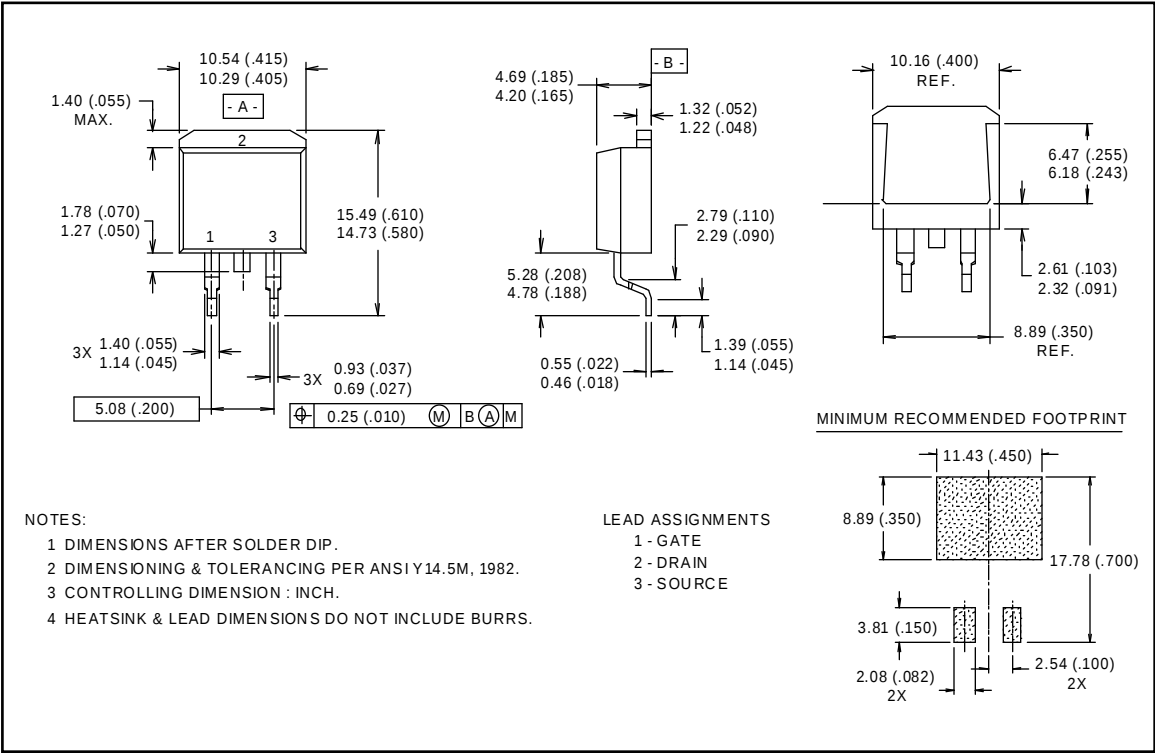
Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

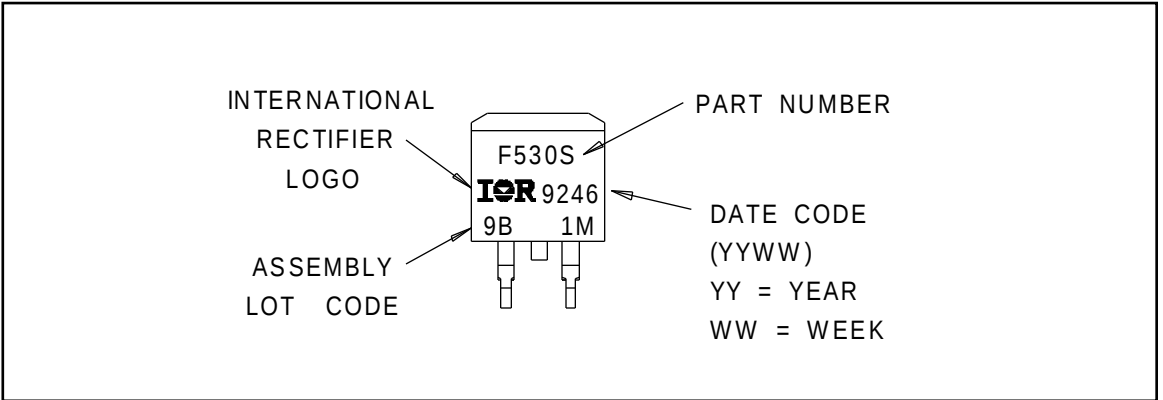
Fig 14.For N-Channel HEXFETS

D²Pak Package Outline



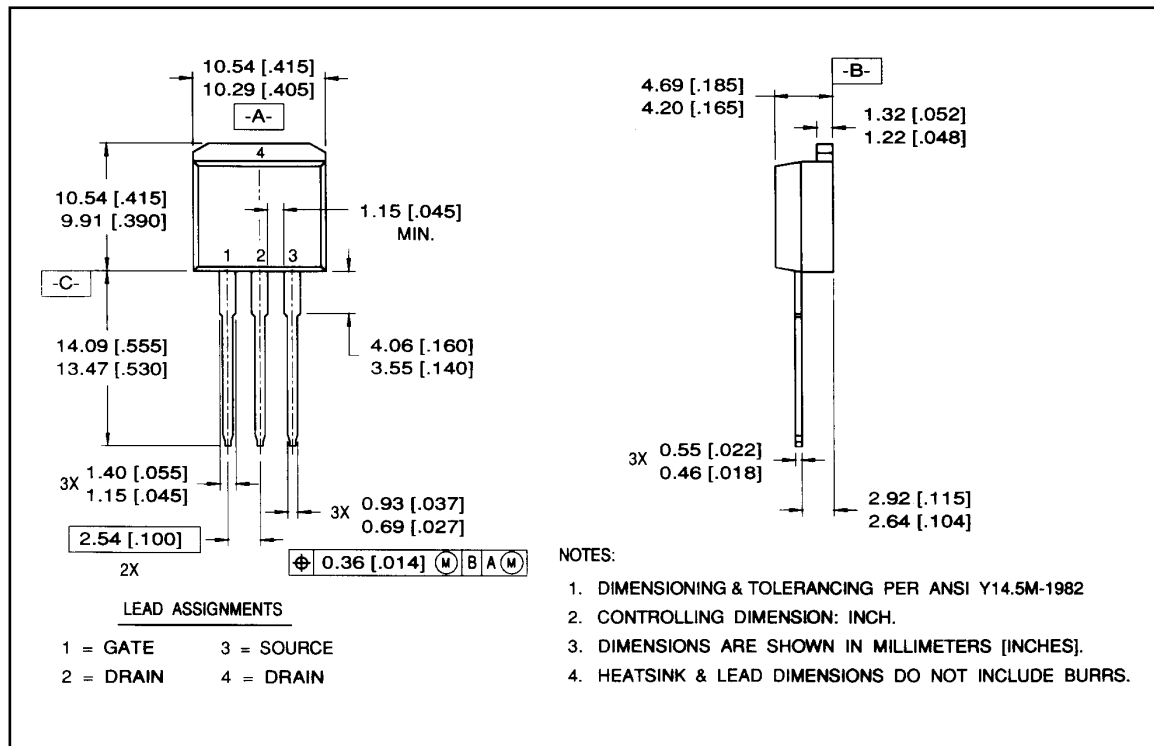
Part Marking Information

D²Pak



Package Outline

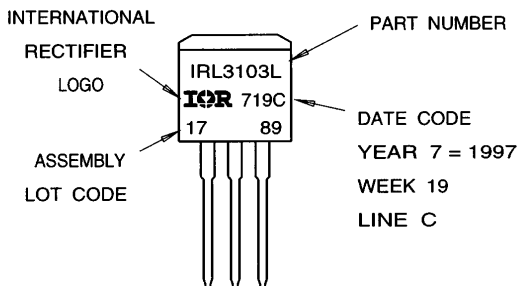
TO-262 Outline



Part Marking Information

TO-262

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



Tape & Reel Information

D²Pak

