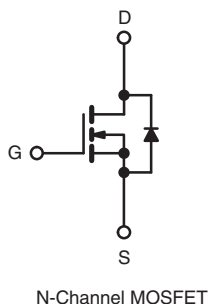
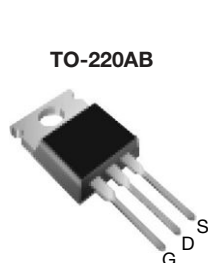


Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	250	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	1.1
Q_g (Max.) (nC)	14	
Q_{gs} (nC)	2.7	
Q_{gd} (nC)	7.8	
Configuration	Single	



FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC



Available
RoHS*
COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free	IRF624PbF SiHF624-E3
SnPb	IRF624 SiHF624

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	250	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	I_D	$T_C = 25\text{ }^{\circ}\text{C}$	A
		$T_C = 100\text{ }^{\circ}\text{C}$	
Pulsed Drain Current ^a	I_{DM}	14	
Linear Derating Factor		0.40	W/ $^{\circ}\text{C}$
Single Pulse Avalanche Energy ^b	E_{AS}	100	mJ
Repetitive Avalanche Current ^a	I_{AR}	4.4	A
Repetitive Avalanche Energy ^a	E_{AR}	5.0	mJ
Maximum Power Dissipation	P_D	50	W
Peak Diode Recovery dV/dt ^c	dV/dt	4.8	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^{\circ}\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	
Mounting Torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

Notes

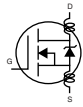
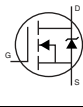
- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$, starting $T_J = 25\text{ }^{\circ}\text{C}$, $L = 8.3\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 4.4\text{ A}$ (see fig. 12).
- $I_{SD} \leq 4.4\text{ A}$, $dI/dt \leq 90\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^{\circ}\text{C}$.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	2.5	

SPECIFICATIONS ($T_J = 25\text{ °C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		250	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.36	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 250 V, V _{GS} = 0 V		-	-	25	μA
		V _{DS} = 200 V, V _{GS} = 0 V, T _J = 125 °C		-	-	250	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 2.6 A ^b	-	-	1.1	Ω
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 2.6 A ^b		1.5	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	260	-	pF
Output Capacitance	C _{oss}			-	77	-	
Reverse Transfer Capacitance	C _{rss}			-	15	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 4.4 A, V _{DS} = 200 V, see fig. 6 and 13 ^b	-	-	14	nC
Gate-Source Charge	Q _{gs}			-	-	2.7	
Gate-Drain Charge	Q _{gd}			-	-	7.8	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 125 V, I _D = 4.4 A, R _g = 18 Ω, R _D = 28 Ω, see fig. 10 ^b		-	7.0	-	ns
Rise Time	t _r			-	13	-	
Turn-Off Delay Time	t _{d(off)}			-	20	-	
Fall Time	t _f			-	12	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal Source Inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	4.4	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	14	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 4.4 A, V _{GS} = 0 V ^b		-	-	1.8	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 4.4 A, dI/dt = 100 A/μs ^b		-	200	400	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	0.93	1.9	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

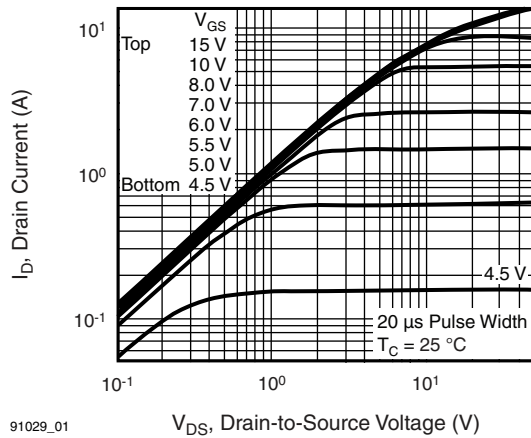


Fig. 1 - Typical Output Characteristics, $T_C = 25^\circ\text{C}$

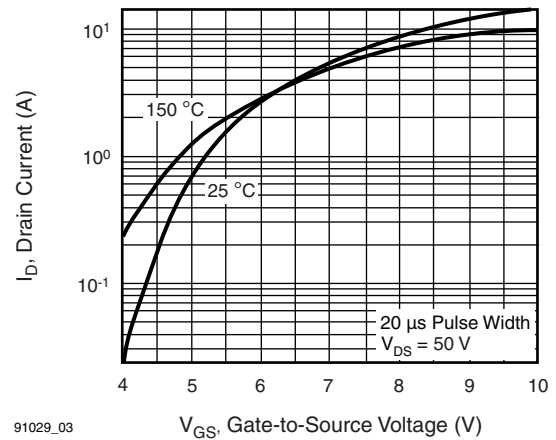


Fig. 3 - Typical Transfer Characteristics

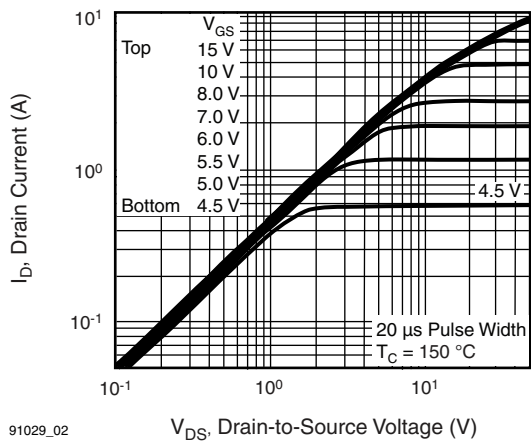


Fig. 2 - Typical Output Characteristics, $T_C = 150^\circ\text{C}$

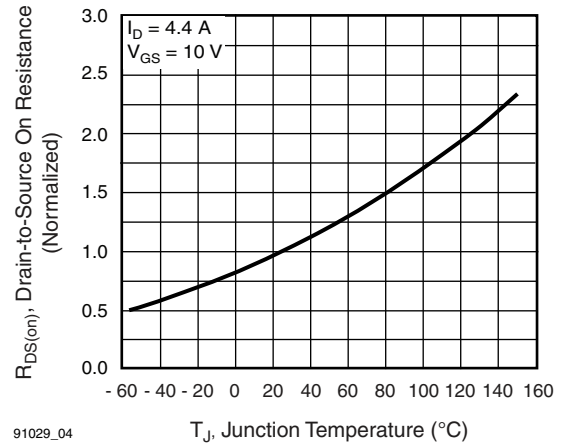
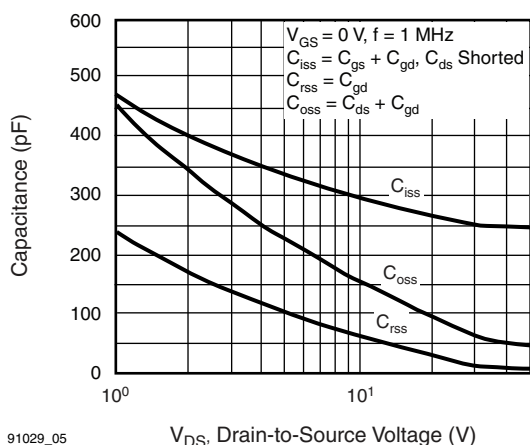
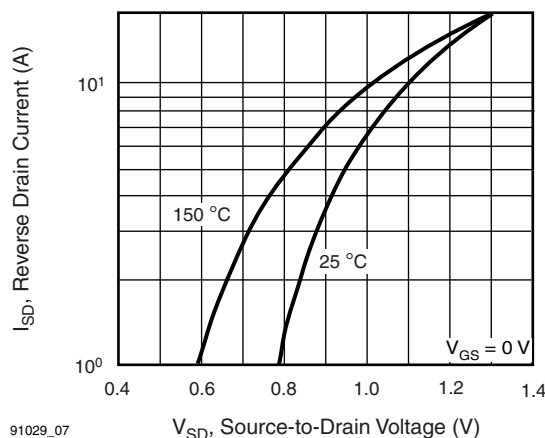


Fig. 4 - Normalized On-Resistance vs. Temperature



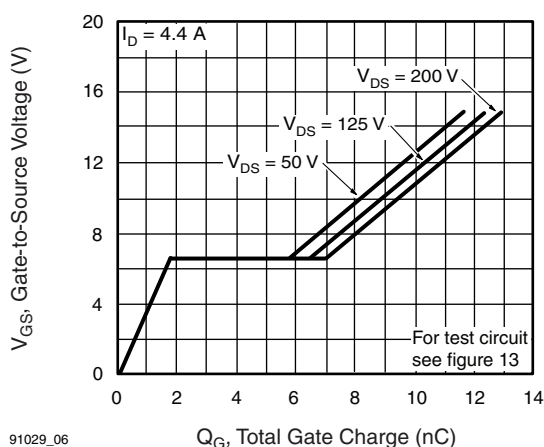
91029_05

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



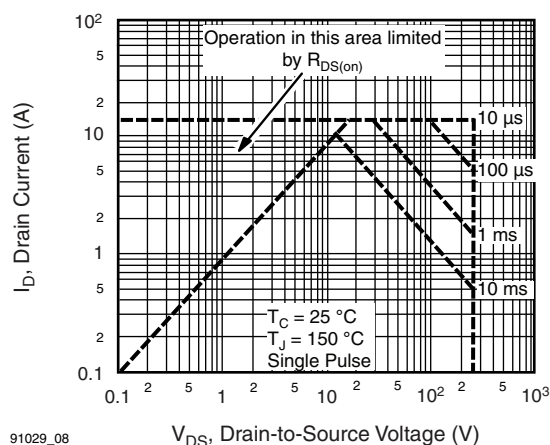
91029_07

Fig. 7 - Typical Source-Drain Diode Forward Voltage



91029_06

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



91029_08

Fig. 8 - Maximum Safe Operating Area

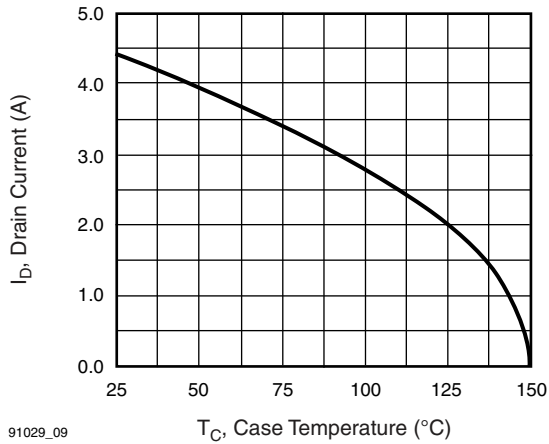


Fig. 9 - Maximum Drain Current vs. Case Temperature

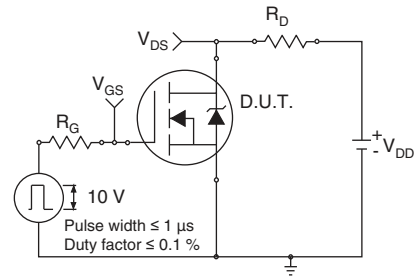


Fig. 10a - Switching Time Test Circuit

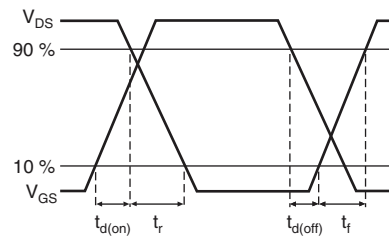


Fig. 10b - Switching Time Waveforms

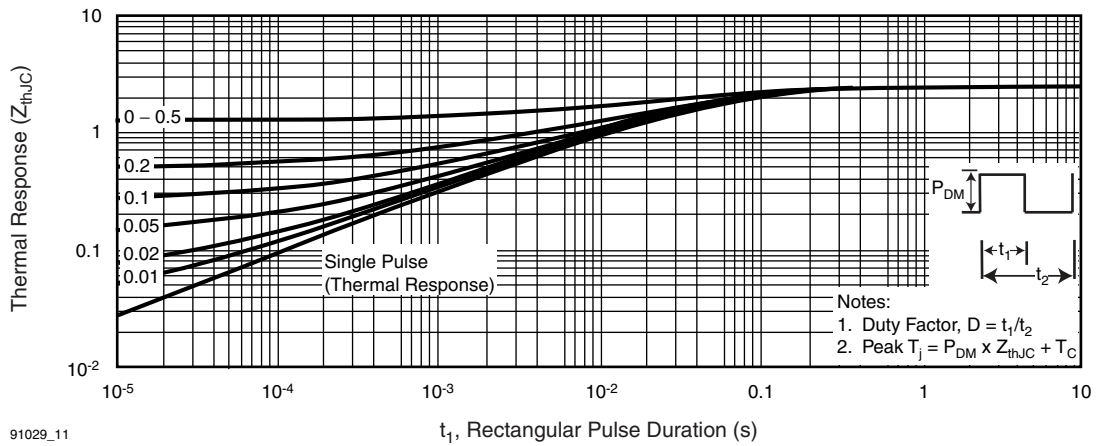


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

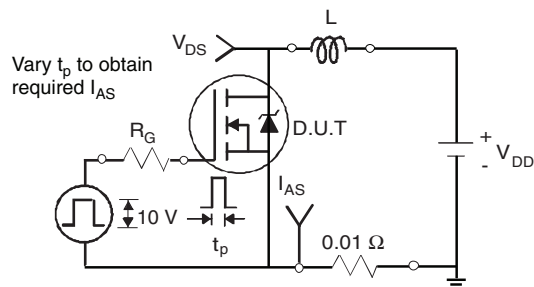


Fig. 12a - Unclamped Inductive Test Circuit

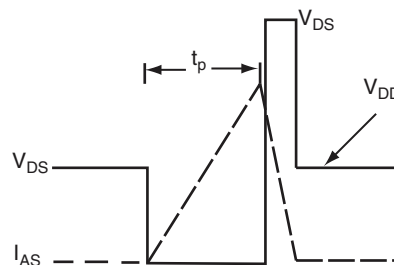


Fig. 12b - Unclamped Inductive Waveforms

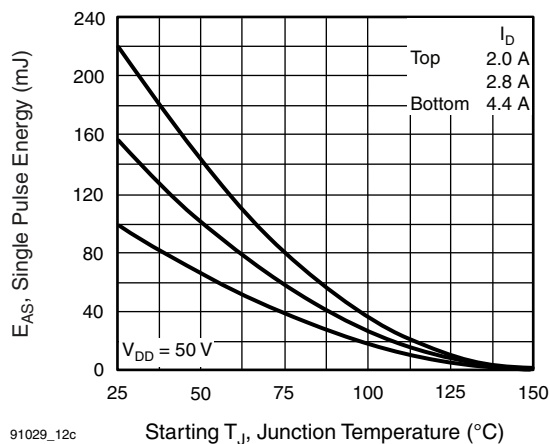


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

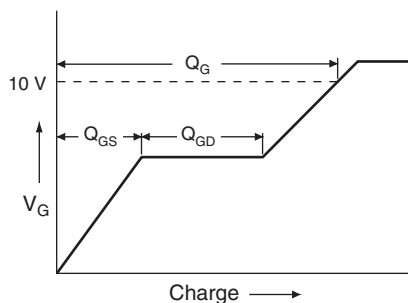


Fig. 13a - Basic Gate Charge Waveform

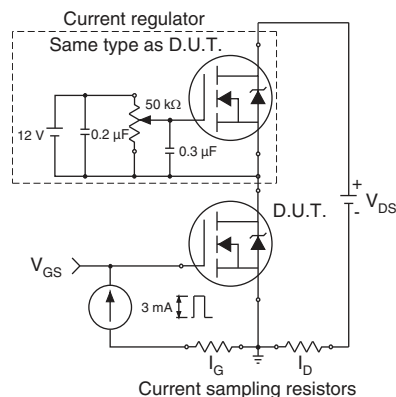
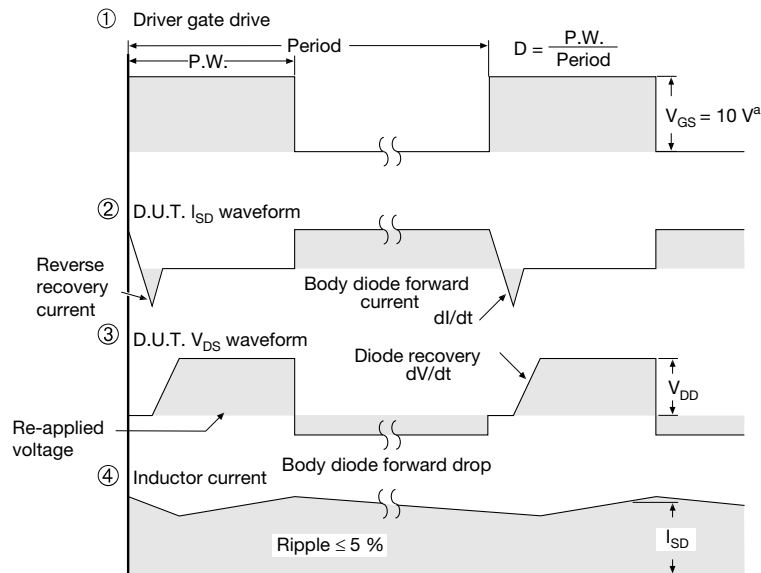
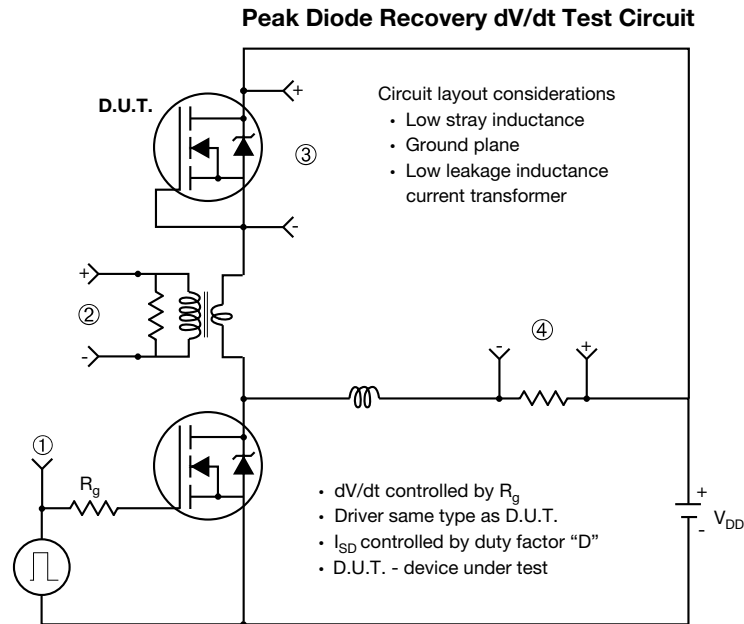


Fig. 13b - Gate Charge Test Circuit



Note

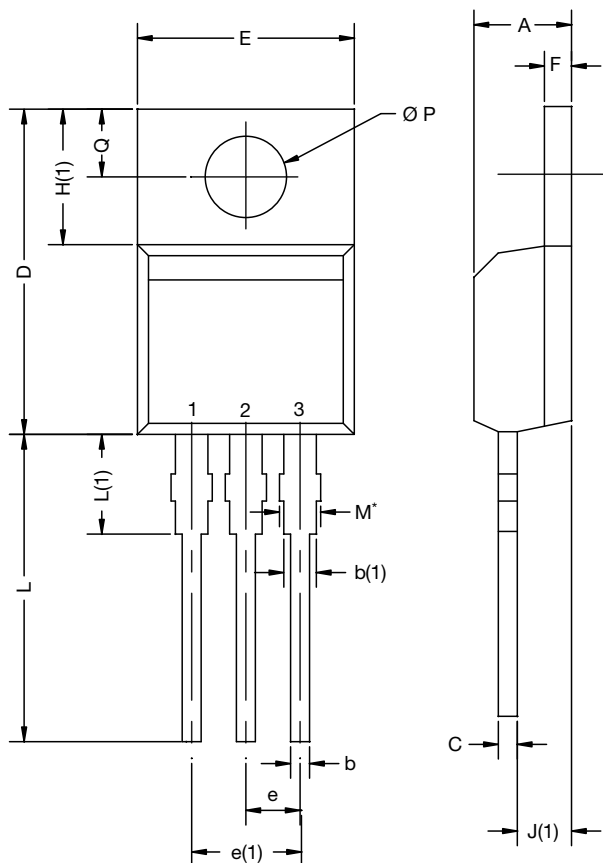
a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91029.



TO-220-1

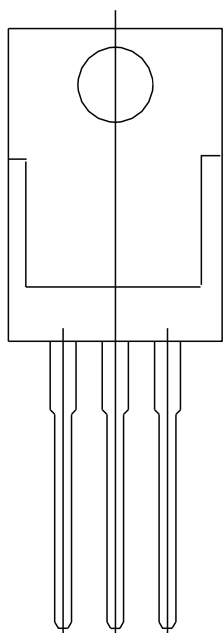


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.14	4.70	0.163	0.185
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.73	0.045	0.068
c	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
E	9.96	10.52	0.392	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	0.43	1.40	0.017	0.055
H(1)	6.10	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
Ø P	3.53	3.94	0.139	0.155
Q	2.59	3.00	0.102	0.118

ECN: X15-0003-Rev. A, 19-Jan-15
DWG: 6031

Notes

- M* = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM
- Outline conforms to JEDEC® outline TO-220AB with exception of dimension F





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