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MC68306

Product Brief

Integrated EC000 Processor

The MC68306 is an integrated processor containing a 68EC000 processor and elements common to many 68000- and 68EC000-based systems. Designers of virtually any application requiring 68000-class performance will find that the MC68306 reduces design time by providing valuable system elements pre-packaged in one chip. The combination of peripherals offered in the MC68306 can be found in a diverse range of microprocessor-based systems, including embedded control and general computing. Systems requiring serial communication and dynamic random access memory (DRAM) can especially benefit from using the MC68306.

The MC68306's high level of functional integration results in significant reductions in component count, power consumption, board space, and cost while yielding much higher system reliability and shorter design time. Complete code compatibility with the MC68000 affords the designer access to a broad base of established real-time kernels, operating systems, languages, applications, and development tools, many of which are oriented towards embedded control. Figure 1 shows a simplified block diagram of the MC68306.

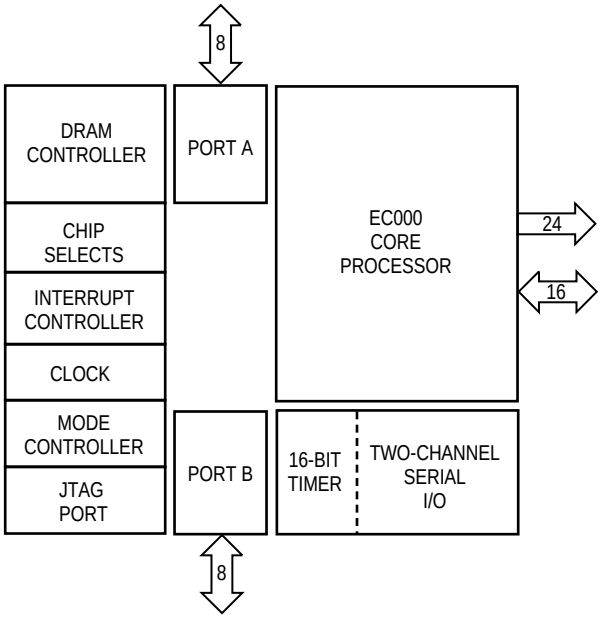

Figure 1. MC68306 Simplified Block Diagram

The primary features of the MC68306 are as follows:

- Functional Integration on a Single Piece of Silicon
- EC000 Core—Identical to MC68EC000 Microprocessor
  - — Complete Code Compatibility with MC68000 and MC68EC000
  - — High Performance—2.4 MIPS
- Two-Channel Universal Synchronous/Asynchronous Receiver/Transmitter (a DUART)
  - — Baud Rate Generators
  - — Modem Control
  - — Identical to MC68681/MC2681
  - — Integrated 16-Bit Timer/Counter (useful for periodic interrupt generation, event counting, etc.)
- Dynamic Random Access Memory (DRAM) Controller
  - — Supports 16 Mbytes using 4M x 1 DRAMs, 64 Mbytes using 16M x 1 DRAMs (compatible with larger future-generation DRAMs)
  - — Provides 0 Wait State Interface to 80-ns DRAMs
  - — Programmable Refresh Timer Provides CAS-before-RAS Refresh
- Chip Selects
  - — Eight Programmable Chip Select Signals
  - — Provide Eight Separate 1-Mbyte Spaces or Four Separate 16-Mbyte Spaces Locatable anywhere within the 4-Gbyte Address Range of the EC000 Core
  - — Programmable Wait States
- Programmable Interrupt Controller
- Bus Watchdog Timer
- 24 Address Lines, 16 Data Lines
- 16.67-MHz, 5-V Operation
- 128-Pin Plastic Quad Flat Pack (QFP) or 132-Pin Plastic Quad Flat Pack (PQFP)

M68300 FAMILY

The MC68306 is one of a series of components in Motorola's M68300 family. Other members of the family include the MC68302, MC68330, MC68331, MC68332, MC68F333, MC68334, and MC68340.

ORGANIZATION

The M68300 family of integrated processors and controllers is built on an M68000 core processor and a selection of intelligent peripherals appropriate for a set of applications. Common system glue logic such as address decoding, wait state insertion, interrupt prioritization, and watchdog timing is also included.

Each member of the M68300 family is distinguished by its selection of peripherals. Peripherals are chosen to address specific applications but are often useful in a wide variety of applications. The peripherals may be highly sophisticated timing or protocol engines that have their own processors, or they may be more traditional peripheral functions, such as UARTs and timers.

ADVANTAGES

By incorporating so many major features into a single M68300 family chip, a system designer can realize significant savings in design time, power consumption, cost, board space, pin count, and programming. The equivalent functionality can easily require 20 separate components. Each component might have 16–64 pins, totaling over 350 connections. Most of these connections require interconnects or are duplications. Each connection is a candidate for a bad solder joint or misrouted trace. Each component is another part to qualify, purchase, inventory, and maintain. Each component requires a share of the printed circuit board. Each component draws power, which is often used to drive large buffers to get the signal to another chip. The cumulative power consumption of all the components must be available from the power supply. The signals between the CPU and a peripheral might not be compatible nor run from the same clock, requiring time delays or other special design considerations.

In an M68300 family component, the major functions and glue logic are all properly connected internally, timed with the same clock, fully tested, and uniformly documented. Only essential signals are brought out to pins. The primary package is the surface-mount plastic quad flat pack for the smallest possible footprint.

MC68306 SIGNALS

Figure 2 is a detailed diagram showing the integrated peripherals and signals.

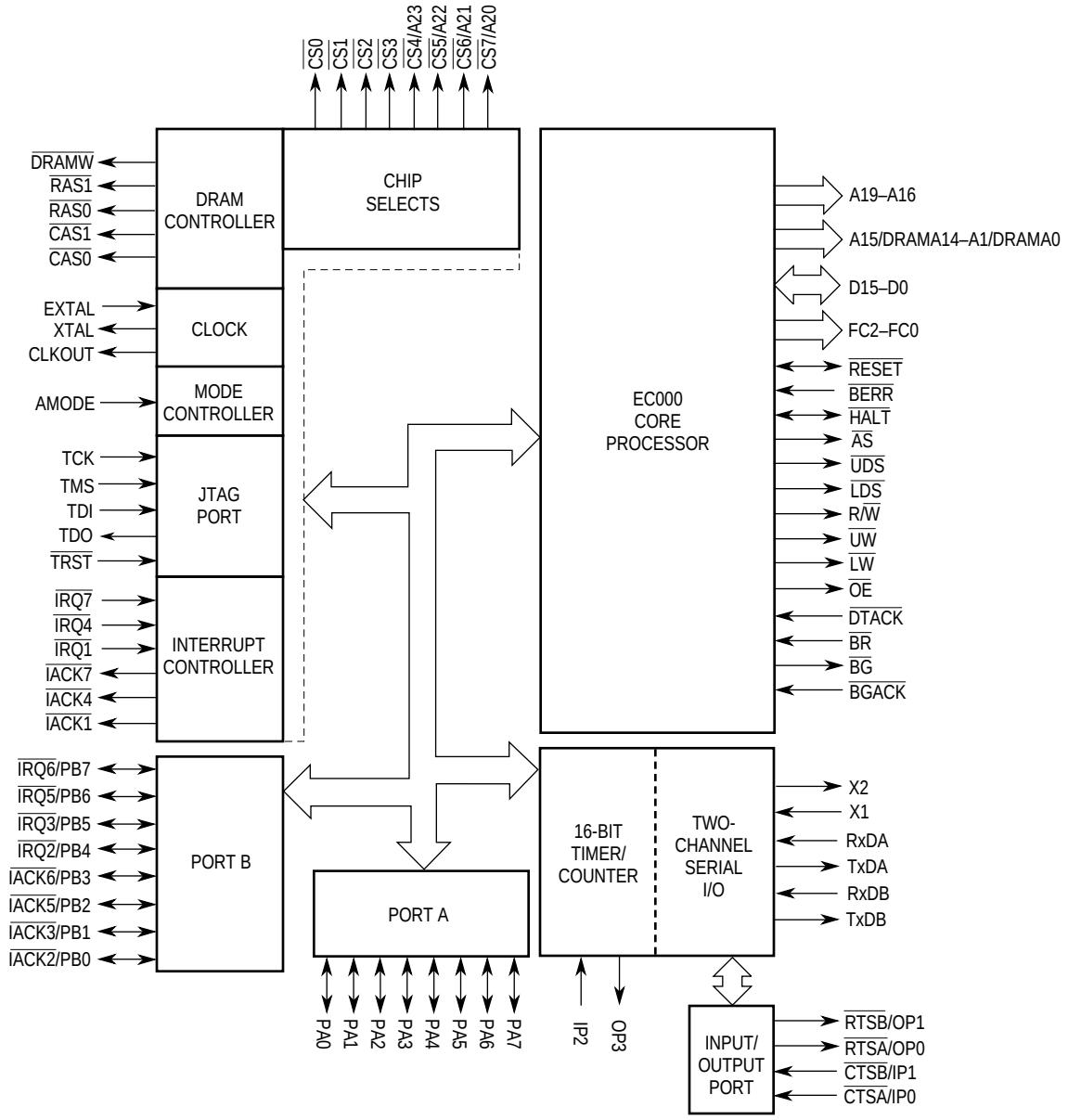

Figure 2. MC68306 Detailed Block Diagram

EC000 CORE PROCESSOR

The core processor is the heart of an integrated processor; it supervises system functions, makes decisions, manipulates data, and directs I/O. The EC000 core is a core implementation of the MC68000 32-bit microprocessor architecture. The programmer can use any of the eight 32-bit data registers for fast manipulation of data and any of the eight 32-bit address registers for indexing data in memory. Flexible instructions support data movement, arithmetic functions, logical operations, shifts and rotates, bit set and clear, conditional and unconditional program branches, and overall system control.

The EC000 core can operate on data types of single bits, binary-coded decimal (BCD) digits, and 8, 16, and 32 bits. The integrated chip selects allow peripherals and data in memory to reside anywhere in the 4-Gbyte linear address space. A supervisor operating mode protects system-level resources from the more restricted user mode, allowing a true virtual environment to be developed. Many addressing modes complement these instructions, including predecrement and postincrement, which allow simple stack and queue maintenance and scaled indexing for efficient table accesses. Data types and addressing modes are supported orthogonally by all data operations and with all appropriate addressing modes. Position-independent code is easily written.

Like all M68000 family processors, the EC000 core recognizes interrupts of seven different priority levels and allows the peripheral to vector the processor to the desired service routine. Internal trap exceptions ensure proper instruction execution with good addresses and data, allow operating system intervention in special situations, and permit instruction tracing. Hardware signals can either terminate or rerun bad memory accesses before instructions process data incorrectly. The EC000 core provides 2.4 MIPS at 16.67 MHz.

ON-CHIP PERIPHERALS

To improve total system throughput and reduce part count, board size, and cost of system implementation, the M68300 family integrates on-chip, intelligent peripheral modules and typical glue logic. The functions on the MC68306 include two serial channels, a DRAM controller, a parallel port, and system glue logic.

68681 MODULE

Most digital systems use serial I/O to communicate with host computers, operator terminals, or remote devices. The MC68306 contains a two-channel, full-duplex UART with an integrated timer. An on-chip baud rate generator provides standard baud rates up the 38.4K baud to each channel's receiver and transmitter. The 68681 module is identical to the MC68681/MC2681 DUART.

Each communication channel is completely independent. Data formats can be 5, 6, 7, or 8 bits with even, odd, or no parity and stop bits up to 2 in 1/16 increments. Four-byte receive buffers and two-byte transmit buffers minimize CPU service calls. Each channel provides a wide variety of error detection and maskable interrupt capability. Full-duplex, autoecho loopback, local loopback, and remote loopback modes can be selected. Multidrop applications are also supported.

A 3.6864-MHz crystal drives the baud rate generators. Each transmit and receive channel can be programmed for a different baud rate. Full modem support is provided with separate request-to-send (RTS) and clear-to-send (CTS) signals for each channel.

The integrated 16-bit timer/counter can operate in a counter mode or a timer mode. The timer/counter can function as a system stopwatch, a real-time single interrupt generator, or a device watchdog when in counter mode. In timer mode, the timer/counter can be used as a programmable clock source for channels A and B, a periodic interrupt generator, or a variable duty cycle square-wave generator.

DRAM CONTROLLER

DRAM is used in many systems, since it is the least expensive form of high-speed storage available. However, considerable design effort is often spent designing the interface between the processor and DRAM. The MC68306 contains a full DRAM controller, greatly reducing design time and complexity.

The DRAM controller provides RAS and CAS signals for two separate banks of DRAMs. Each bank can include up to 16 devices; 15 multiplexed address lines are also available. Thus, using 4M x 1 DRAMs, up to 16 Mbytes of DRAM are supported; and with 16M x 1 DRAMs, up to 64 Mbytes of DRAM are supported. A programmable refresh timer provides CAS-before-RAS refreshes at designated intervals.

The DRAM controller has its own address registers that control the address range selected by each RAS and CAS signal, leaving the eight integrated chip selects free for other system peripherals. DRAM accesses are 0 wait states using 80-ns DRAMs.

CHIP SELECTS

The MC68306 provides up to eight programmable chip select outputs, in most cases eliminating the need for external address decoding. All handshaking and timing signals are provided, with up to 950-ns access times. Each chip select can access a 16 Mbyte address space located anywhere in the 4-Gbyte address range. Internal registers allow the base address, range, and cycle duration of each chip select to be independently programmed. After reset, CS0 responds to all accesses until the chip selects have been properly programmed. Four of the chip selects are multiplexed with the most significant address bits (A23–A20). The AMODE input determines the functions of these outputs.

PARALLEL PORTS

Two 8-bit parallel ports are provided. The port pins can be individually programmed to be inputs or outputs. If the pins are programmed to be inputs, the value on those pins can be read by accessing an on-board register. If the pins are programmed to be outputs, the pins will reflect the value programmed into another on-board register. The port B pins are multiplexed with four interrupt request and four interrupt acknowledge lines. The function of these pins is controlled by the internal registers.

INTERRUPT CONTROLLER

Seven input signals are provided to trigger an external interrupt, one for each of the seven priority levels supported. Each input can be programmed to be active high or active low. Seven separate outputs indicate the priority level of the interrupt being serviced. Interrupts at each priority level can be pre-programmed to go to the default service routine. For maximum flexibility, interrupts can be vectored to the correct service routine by the interrupting device.

CLOCK

To save on system costs, the MC68306 has an on-board oscillator that can be driven with a 16.67 MHz crystal. A bus clock output is provided by a CLKOUT pin. Alternatively, an external 16.67 MHz oscillator can be used, with a tight skew between the input clock signal and the bus clock on the CLKOUT pin.

BUS WATCHDOG TIMER

A bus watchdog timer is provided to automatically terminate and report as erroneous any bus cycle that is not normally terminated after a pre-programmed length of time. The user can program this timeout period to be up to 4096 clocks.

MODE CONTROLLER

One input signal is used to determine the function of the multiplexed address/chip select pins. The mode input is sampled on the rising edge of $\overline{\text{RESET}}$.

IEEE 1149.1 TEST

To aid in system diagnostics, the MC68306 includes dedicated user-accessible test logic that is fully compliant with the IEEE 1149.1 standard for boundary scan testability, often referred to as JTAG (Joint Test Action Group).

PHYSICAL

The MC68306 is available as 16.67 MHz, 0°C to +70°C, and 5.0 V ± 5% supply voltage. Twenty power and ground leads minimize ground bounce and ensure proper isolation of different sections of the chip. A total of 128 pins are used for signals and power. The MC68306 is available in a 128-pin gull-wing plastic quad flat pack (QFP) with 0.8-mm lead spacing. For customers desiring emulation capability, the MC68306 is available in a 132-pin gull-wing plastic quad flat pack (PQFP) with 0.25 in. lead spacing.

MORE INFORMATION

The documents listed in the following table contain detailed information on the MC68306. These documents may be obtained from the Literature Distribution Centers at the addresses listed on the back page.

Documentation

Document Title	Order Number	Contents
M68300 Integrated Processor Family	BR1114/D	M68300 Family Overview
MC68306 User's Manual	MC68306UM/AD	Detailed Information for Design
M68000 Family Programmer's Reference Manual	M68000PM/AD	M68000 Family Instruction Set
The 68K Source	BR729/D	Independent Vendor Listing Supporting Software and Development Tools

Literature Distribution Centers:

USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.

EUROPE: Motorola Ltd.; European Literature Centre; 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.

JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141 Japan.

ASIA-PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No.2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.

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