



93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

16K Microwire Compatible Serial EEPROM

Device Selection Table

Part Number	Vcc Range	ORG Pin	PE Pin	Word Size	Temp Ranges	Packages
93AA86A	1.8-5.5	No	No	8-bit	I	P, SN, ST, MS, OT
93AA86B	1.8-5.5	No	No	16-bit	I	P, SN, ST, MS, OT
93LC86A	2.5-5.5	No	No	8-bit	I, E	P, SN, ST, MS, OT
93LC86B	2.5-5.5	No	No	16-bit	I, E	P, SN, ST, MS, OT
93C86A	4.5-5.5	No	No	8-bit	I, E	P, SN, ST, MS, OT
93C86B	4.5-5.5	No	No	16-bit	I, E	P, SN, ST, MS, OT
93AA86C	1.8-5.5	Yes	Yes	8- or 16-bit	I	P, SN, ST, MS, MC, MN
93LC86C	2.5-5.5	Yes	Yes	8- or 16-bit	I, E	P, SN, ST, MS, MC, MN
93C86C	4.5-5.5	Yes	Yes	8- or 16-bit	I, E	P, SN, ST, MS, MC, MN

Features:

- Low-Power CMOS Technology
- ORG Pin to Select Word Size for '86C' Version
- 2048 x 8-bit Organization 'A' Devices (no ORG)
- 1024 x 16-bit Organization 'B' Devices (no ORG)
- Program Enable Pin to Write-Protect the Entire Array ('86C' version only)
- Self-timed Erase/Write Cycles (including Auto-Erase)
- Automatic Erase All (ERALL) before Write All (WRALL)
- Power-On/Off Data Protection Circuitry
- Industry Standard 3-Wire Serial I/O
- Device Status Signal (Ready/Busy)
- Sequential Read Function
- 1,000,000 E/W Cycles
- Data Retention > 200 Years
- Pb-free and RoHS Compliant
- Temperature Ranges Supported:
 - Industrial (I) -40°C to +85°C
 - Automotive (E) -40°C to +125°C

Description:

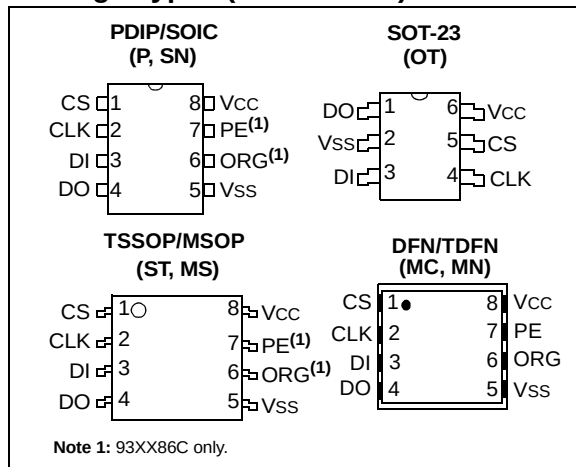
The Microchip Technology Inc. 93XX86A/B/C devices are 16K bit low-voltage serial Electrically Erasable PROMs (EEPROM). Word-selectable devices such as the 93XX86C are dependent upon external logic levels driving the ORG pin to set word size. The 93XX86A devices provide dedicated 8-bit memory organization, while the 93XX86B devices provide dedicated 16-bit memory organization. A Program Enable (PE) pin allows the user to write-protect the entire memory array. Advanced CMOS technology makes these devices ideal for low-power, nonvolatile memory applications. The entire 93XX Series is available in standard packages including 8-lead PDIP and SOIC, and advanced packaging including 8-lead MSOP, 6-lead SOT-23, 8-lead 2x3 DFN/TDFN and 8-lead TSSOP. All packages are Pb-free (Matte Tin) finish.

Pin Function Table

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
Vss	Ground
PE	Program Enable – 93XX86C only
ORG	Memory Configuration – 93XX86C only
Vcc	Power Supply

93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

Package Types (not to scale)



93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings ^(†)

V _{CC}	7.0V
All inputs and outputs w.r.t. V _{SS}	-0.6V to V _{CC} +1.0V
Storage temperature	-65°C to +150°C
Ambient temperature with power applied.....	-40°C to +125°C
ESD protection on all pins	≥ 4 kV

Note: † NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

All parameters apply over the specified ranges unless otherwise noted.			Industrial (I): TA = -40°C to +85°C, V _{CC} = +1.8V to 5.5V Automotive (E): TA = -40°C to +125°C, V _{CC} = +2.5V to 5.5V				
Param. No.	Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
D1	V _{IH1}	High-level input voltage	2.0	—	V _{CC} +1	V	V _{CC} ≥ 2.7V
	V _{IH2}		0.7 V _{CC}	—	V _{CC} +1	V	V _{CC} < 2.7V
D2	V _{IL1}	Low-level input voltage	-0.3	—	0.8	V	V _{CC} ≥ 2.7V
	V _{IL2}		-0.3	—	0.2 V _{CC}	V	V _{CC} < 2.7V
D3	V _{OL1}	Low-level output voltage	—	—	0.4	V	I _{OL} = 2.1 mA, V _{CC} = 4.5V
	V _{OL2}		—	—	0.2	V	I _{OL} = 100 µA, V _{CC} = 2.5V
D4	V _{OH1}	High-level output voltage	2.4	—	—	V	I _{OH} = -400 µA, V _{CC} = 4.5V
	V _{OH2}		V _{CC} - 0.2	—	—	V	I _{OH} = -100 µA, V _{CC} = 2.5V
D5	I _{LI}	Input leakage current	—	—	±1	µA	V _{IN} = V _{SS} or V _{CC}
D6	I _{LO}	Output leakage current	—	—	±1	µA	V _{OUT} = V _{SS} or V _{CC}
D7	C _{IN} , C _{OUT}	Pin capacitance (all inputs/ outputs)	—	—	7	pF	V _{IN} /V _{OUT} = 0V (Note 1) TA = 25°C, F _{CLK} = 1 MHz
D8	I _{CC} write	Write current	—	—	3	mA	F _{CLK} = 3 MHz, V _{CC} = 5.5V
			—	500	—	µA	F _{CLK} = 2 MHz, V _{CC} = 2.5V
D9	I _{CC} read	Read current	—	—	1	mA	F _{CLK} = 3 MHz, V _{CC} = 5.5V
			—	—	500	µA	F _{CLK} = 2 MHz, V _{CC} = 3.0V
			—	100	—	µA	F _{CLK} = 2 MHz, V _{CC} = 2.5V
D10	I _{CCS}	Standby current	—	—	1	µA	I – Temp
			—	—	5	µA	E – Temp CLK = CS = 0V ORG = DI PE = V _{SS} or V _{CC} (Note 2) (Note 3)
D11	V _{POR}	V _{CC} voltage detect	—	1.5	—	V	(Note 1)
			—	3.8	—	V	93AA86A/B/C, 93LC86A/B/C 93C86A/B/C

- Note 1:** This parameter is periodically sampled and not 100% tested.
2: ORG and PE pin not available on 'A' or 'B' versions.
3: Ready/Busy status must be cleared from DO; see [Section 3.4 “Data Out \(DO\)”](#).

93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

TABLE 1-2: AC CHARACTERISTICS

All parameters apply over the specified ranges unless otherwise noted.			Industrial (I): TA = -40°C to +85°C, VCC = +1.8V to 5.5V Automotive (E): TA = -40°C to +125°C, VCC = +2.5V to 5.5V			
Param. No.	Symbol	Parameter	Min.	Max.	Units	Conditions
A1	FCLK	Clock frequency	—	3 2 1	MHz MHz MHz	4.5V ≤ VCC < 5.5V 2.5V ≤ VCC < 4.5V 1.8V ≤ VCC < 2.5V
A2	TCKH	Clock high time	200 250 450	—	ns ns ns	4.5V ≤ VCC < 5.5V 2.5V ≤ VCC < 4.5V 1.8V ≤ VCC < 2.5V
A3	TCKL	Clock low time	100 200 450	—	ns ns ns	4.5V ≤ VCC < 5.5V 2.5V ≤ VCC < 4.5V 1.8V ≤ VCC < 2.5V
A4	TCSS	Chip Select setup time	50 100 250	—	ns ns ns	4.5V ≤ VCC < 5.5V 2.5V ≤ VCC < 4.5V 1.8V ≤ VCC < 2.5V
A5	TCSH	Chip Select hold time	0	—	ns	1.8V ≤ VCC < 5.5V
A6	TCSL	Chip Select low time	250	—	ns	1.8V ≤ VCC < 5.5V
A7	TDIS	Data input setup time	50 100 250	—	ns ns ns	4.5V ≤ VCC < 5.5V 2.5V ≤ VCC < 4.5V 1.8V ≤ VCC < 2.5V
A8	TDIH	Data input hold time	50 100 250	—	ns ns ns	4.5V ≤ VCC < 5.5V 2.5V ≤ VCC < 4.5V 1.8V ≤ VCC < 2.5V
A9	TPD	Data output delay time	—	100 250 400	ns ns ns	4.5V ≤ VCC < 5.5V, CL = 100 pF 2.5V ≤ VCC < 4.5V, CL = 100 pF 1.8V ≤ VCC < 2.5V, CL = 100 pF
A10	TCZ	Data output disable time	—	100 200	ns ns	4.5V ≤ VCC < 5.5V, (Note 1) 1.8V ≤ VCC < 4.5V, (Note 1)
A11	Tsv	Status valid time	—	200 300 500	ns ns ns	4.5V ≤ VCC < 5.5V, CL = 100 pF 2.5V ≤ VCC < 4.5V, CL = 100 pF 1.8V ≤ VCC < 2.5V, CL = 100 pF
A12	TWC	Program cycle time	—	5	ms	Erase/Write mode (AA and LC versions)
A13	TWC		—	2	ms	Erase/Write mode (93C versions)
A14	TEC		—	6	ms	ERAL mode, 4.5V ≤ VCC ≤ 5.5V
A15	TWL		—	15	ms	WRAL mode, 4.5V ≤ VCC ≤ 5.5V
A16	—	Endurance	1M	—	cycles	25°C, VCC = 5.0V, (Note 2)

Note 1: This parameter is periodically sampled and not 100% tested.

- 2:** This application is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model, which may be obtained from Microchip's web site at www.microchip.com.

93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

FIGURE 1-1: SYNCHRONOUS DATA TIMING

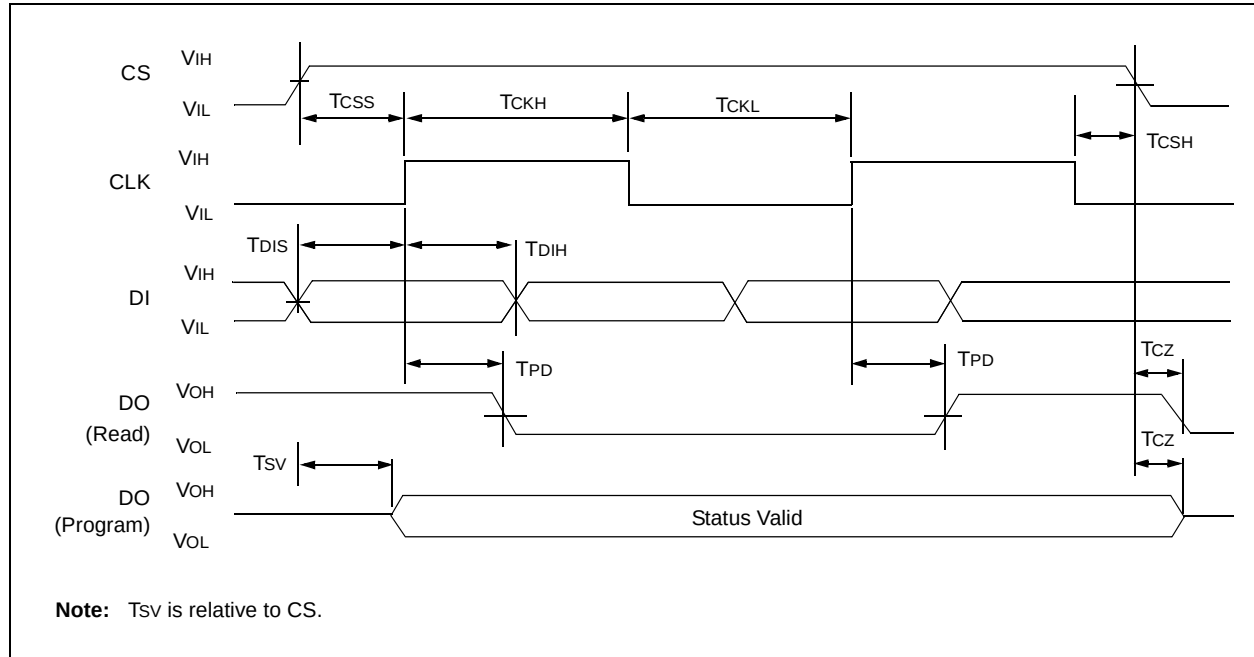


TABLE 1-3: INSTRUCTION SET FOR X16 ORGANIZATION (93XX86B OR 93XX86C WITH ORG = 1)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	—	D15-D0	29
EWEN	1	00	1 1 X X X X X X X X X X	—	HighZ	13
ERASE	1	11	A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/ $\overline{BSY}$)	13
ERAL	1	00	1 0 X X X X X X X X X X	—	(RDY/ $\overline{BSY}$)	13
WRITE	1	01	A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	D15-D0	(RDY/ $\overline{BSY}$)	29
WRAL	1	00	0 1 X X X X X X X X X X	D15-D0	(RDY/ $\overline{BSY}$)	29
EWDS	1	00	0 0 X X X X X X X X X X	—	High-Z	13

TABLE 1-4: INSTRUCTION SET FOR X8 ORGANIZATION (93XX86A OR 93XX86C WITH ORG = 0)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	—	D7-D0	22
EWEN	1	00	1 1 X X X X X X X X X X X X	—	High-Z	14
ERASE	1	11	A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/ $\overline{BSY}$)	14
ERAL	1	00	1 0 X X X X X X X X X X X X	—	(RDY/ $\overline{BSY}$)	14
WRITE	1	01	A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	D7-D0	(RDY/ $\overline{BSY}$)	22
WRAL	1	00	0 1 X X X X X X X X X X X X	D7-D0	(RDY/ $\overline{BSY}$)	22
EWDS	1	00	0 0 X X X X X X X X X X X X	—	High-Z	14

93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

2.0 FUNCTIONAL DESCRIPTION

When the ORG pin (93XX86C) is connected to VCC, the (x16) organization is selected. When it is connected to ground, the (x8) organization is selected. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a High-Z state except when reading data from the device, or when checking the Ready/Busy status during a programming operation. The Ready/Busy status can be verified during an Erase/Write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. DO will enter the High-Z state on the falling edge of CS.

2.1 Start Condition

The Start bit is detected by the device if CS and DI are both high with respect to the positive edge of CLK for the first time.

Before a Start condition is detected, CS, CLK and DI may change in any combination (except to that of a Start condition), without resulting in any device operation (Read, Write, Erase, EWEN, EWDS, ERAL or WRAL). As soon as CS is high, the device is no longer in Standby mode.

An instruction following a Start condition will only be executed if the required opcode, address and data bits for any particular instruction are clocked in.

Note: When preparing to transmit an instruction, either the CLK or DI signal levels must be at a logic low as CS is toggled active high.

2.2 Data In/Data Out (DI/DO)

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation, if A0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of the driver, the higher the voltage at the Data Out pin. In order to limit this current, a resistor should be connected between DI and DO.

2.3 Data Protection

All modes of operation are inhibited when VCC is below a typical voltage of 1.5V for '93AA' and '93LC' devices or 3.8V for '93C' devices.

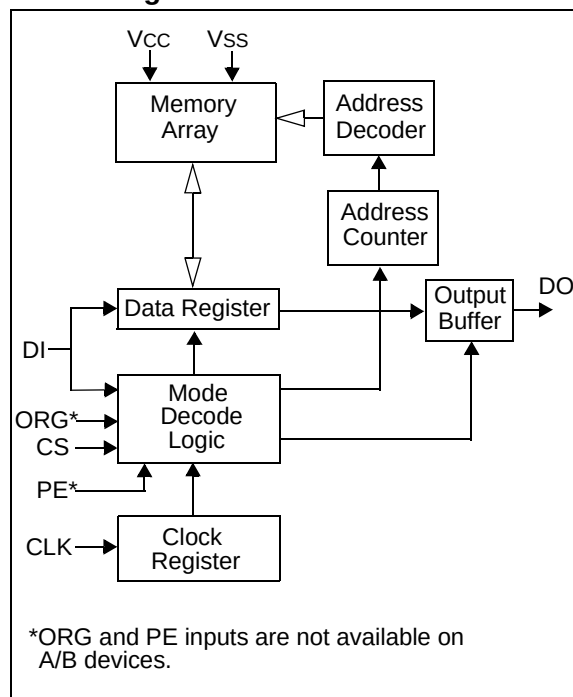
The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

Note: For added protection, an EWDS command should be performed after every write operation and an external 10 kΩ pull-down protection resistor should be added to the CS pin.

After power-up the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before the initial ERASE or WRITE instruction can be executed.

Note: To prevent accidental writes to the array in the 93XX86C devices, set the PE pin to a logic low.

Block Diagram



93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

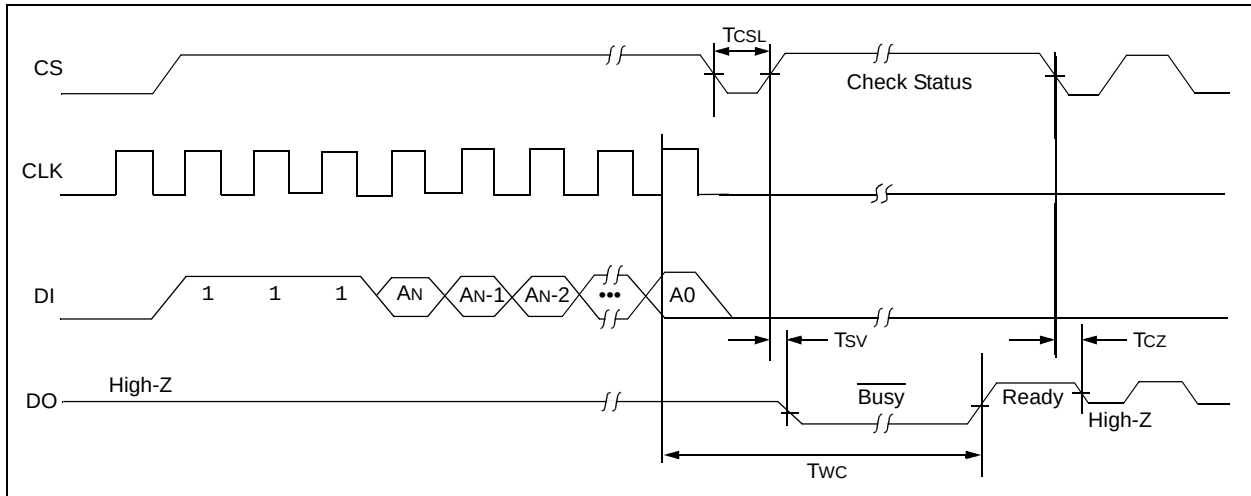
2.4 Erase

The **ERASE** instruction forces all data bits of the specified address to the logical '1' state. The rising edge of CLK before the last address bit initiates the write cycle.

The DO pin indicates the Ready/ $\overline{\text{Busy}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL). DO at logical '0' indicates that programming is still in progress. DO at logical '1' indicates that the register at the specified address has been erased and the device is ready for another instruction.

Note: After the Erase cycle is complete, issuing a Start bit and then taking CS low will clear the Ready/ $\overline{\text{Busy}}$ status from DO.

FIGURE 2-1: ERASE TIMING



2.5 Erase All (ERAL)

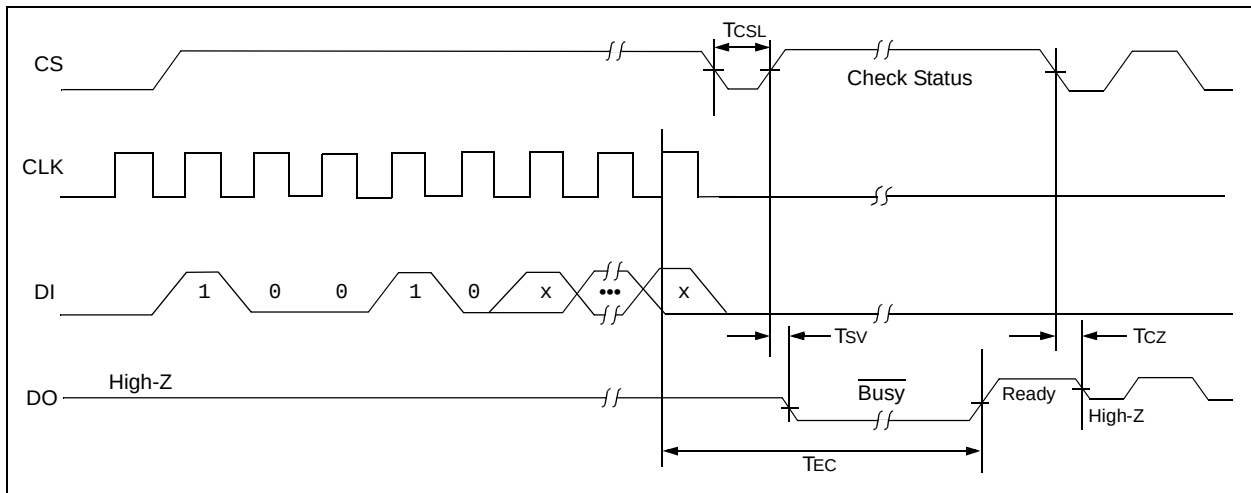
The Erase All (ERAL) instruction will erase the entire memory array to the logical '1' state. The ERAL cycle is identical to the erase cycle, except for the different opcode. The ERAL cycle is completely self-timed. The rising edge of CLK before the last data bit initiates the write cycle. Clocking of the CLK pin is not necessary after the device has entered the ERAL cycle.

The DO pin indicates the Ready/ $\overline{\text{Busy}}$ status of the device, if CS is brought high after a minimum of 250 ns low (TCSL).

Note: After the ERAL command is complete, issuing a Start bit and then taking CS low will clear the Ready/ $\overline{\text{Busy}}$ status from DO.

VCC must be $\geq 4.5\text{V}$ for proper operation of ERAL.

FIGURE 2-2: ERAL TIMING



93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

2.6 Erase/Write Disable and Enable (EWDS/EWEN)

The 93XX86A/B/C powers up in the Erase/Write Disable (EWDS) state. All programming modes must be preceded by an Erase/Write Enable (EWEN) instruction.

Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or VCC is removed from the device.

To protect against accidental data disturbance, the EWDS instruction can be used to disable all Erase/Write functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

FIGURE 2-3: EWDS TIMING

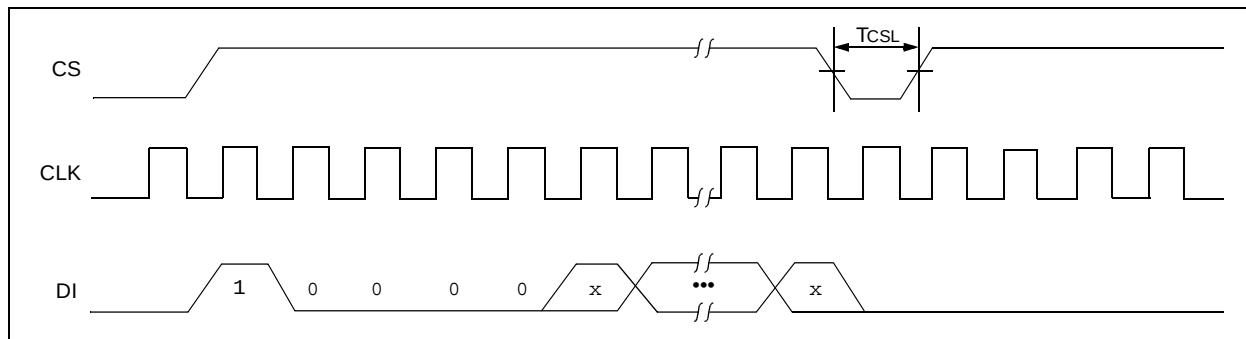
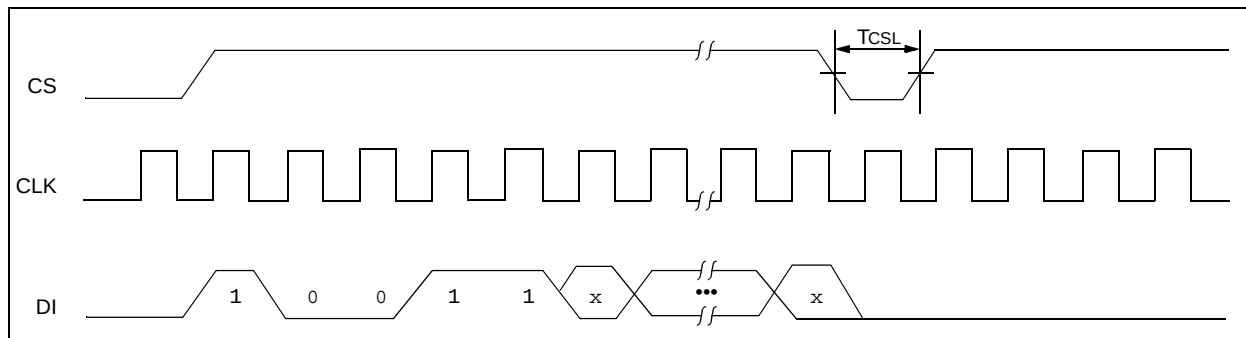


FIGURE 2-4: EWEN TIMING

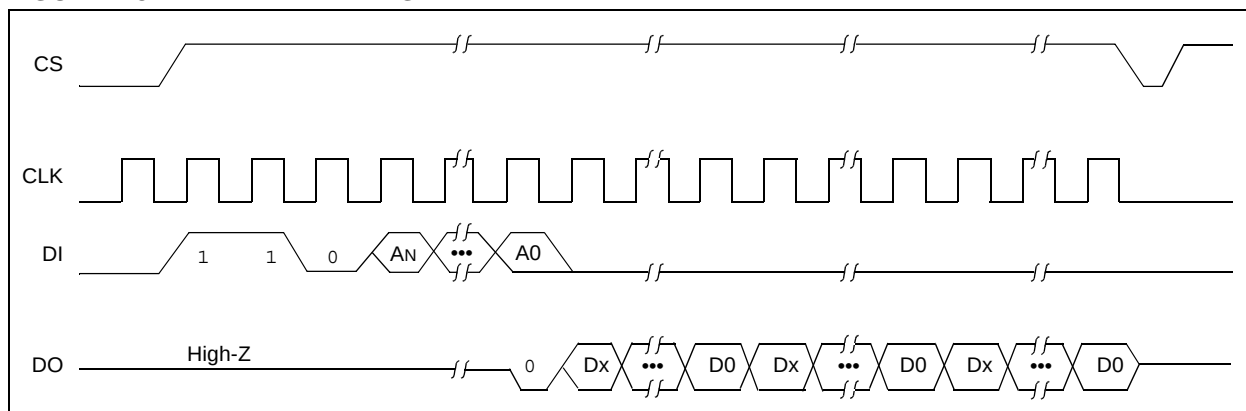


2.7 Read

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 8-bit (If ORG pin is low or A-Version devices) or 16-bit (If ORG pin is high or B-version devices) output string.

The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

FIGURE 2-5: READ TIMING



93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

2.8 Write

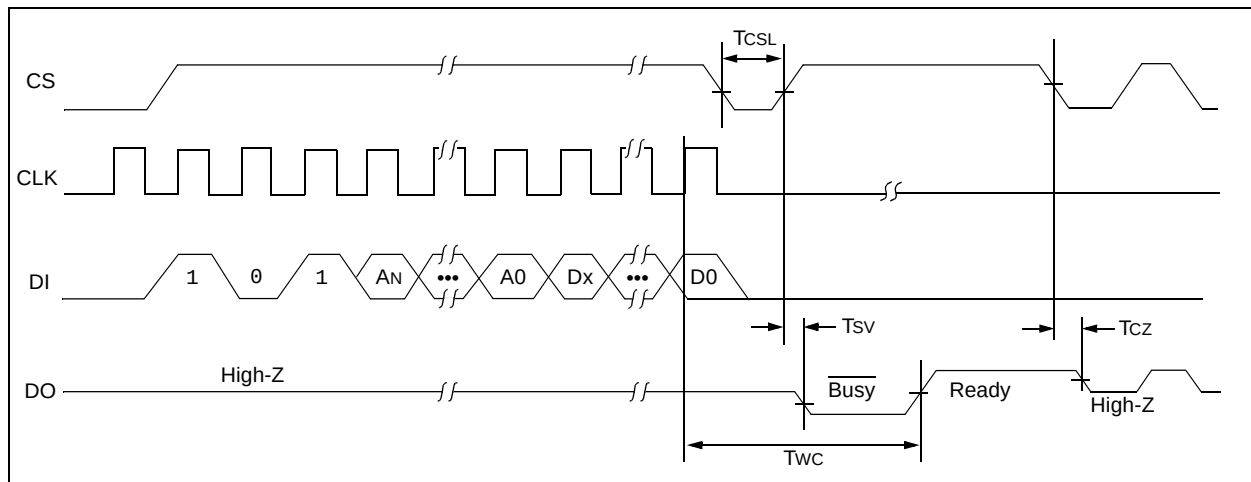
The **WRITE** instruction is followed by 8 bits (If **ORG** is low or A-version devices) or 16 bits (If **ORG** pin is high or B-version devices) of data which are written into the specified address. The self-timed auto-erase and programming cycle is initiated by the rising edge of **CLK** on the last data bit.

The **DO** pin indicates the Ready/ $\overline{\text{Busy}}$ status of the device, if **CS** is brought high after a minimum of 250 ns low (T_{CSL}). **DO** at logical '0' indicates that programming is still in progress. **DO** at logical '1' indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

Note: The write sequence requires a logic high signal on the **PE** pin prior to the rising edge of the last data bit.

Note: After the Write cycle is complete, issuing a Start bit and then taking **CS** low will clear the Ready/ $\overline{\text{Busy}}$ status from **DO**

FIGURE 2-6: WRITE TIMING



93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

2.9 Write All (WRAL)

The Write All (WRAL) instruction will write the entire memory array with the data specified in the command. The self-timed auto-erase and programming cycle is initiated by the rising edge of CLK on the last data bit. Clocking of the CLK pin is not necessary after the device has entered the WRAL cycle. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction, but the chip must be in the EWEN status.

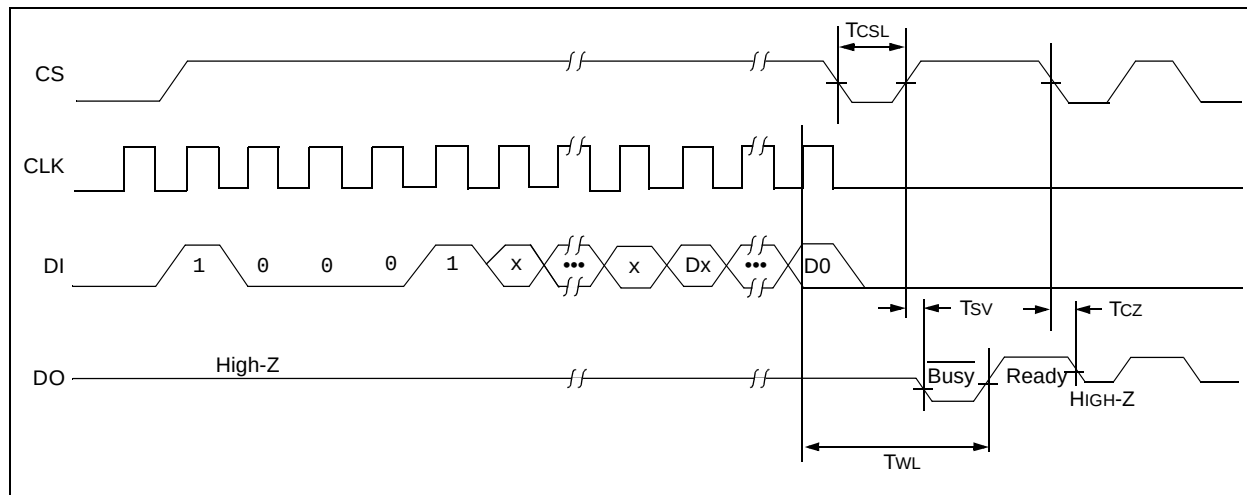
The DO pin indicates the Ready/Busy status of the device if CS is brought high after a minimum of 250 ns low (TCSL).

Note: The write sequence requires a logic high signal on the PE pin prior to the rising edge of the last data bit.

Note: After the Write All cycle is complete, issuing a Start bit and then taking CS low will clear the Ready/Busy status from DO.

Vcc must be $\geq 4.5V$ for proper operation of WRAL.

FIGURE 2-7: WRAL TIMING



93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

3.0 PIN DESCRIPTIONS

TABLE 3-1: PIN DESCRIPTIONS

Name	PDIP	SOIC	TSSOP	MSOP	DFN ⁽¹⁾	TDFN ⁽¹⁾	SOT-23	Function
CS	1	1	1	1	1	1	5	Chip Select
CLK	2	2	2	2	2	2	4	Serial Clock
DI	3	3	3	3	3	3	3	Data In
DO	4	4	4	4	4	4	1	Data Out
Vss	5	5	5	5	5	5	2	Ground
ORG	6	6	6	6	6	6	—	Organization/93XX86C only
PE	7	7	7	7	7	7	—	Program Enable/93XX86C only
Vcc	8	8	8	8	8	8	6	Power Supply

Note 1: The exposed pad on the DFN/TDFN package may be connected to Vss or left floating.

3.1 Chip Select (CS)

A high level selects the device; a low level deselects the device and forces it into Standby mode. However, a programming cycle which is already in progress will be completed, regardless of the Chip Select (CS) input signal. If CS is brought low during a program cycle, the device will go into Standby mode as soon as the programming cycle is completed.

CS must be low for 250 ns minimum (T_{CSL}) between consecutive instructions. If CS is low, the internal control logic is held in a Reset status.

3.2 Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93XX series device. Opcodes, address and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at high or low level) and can be continued anytime with respect to clock high time (T_{CKH}) and clock low time (T_{CKL}). This gives the controlling master freedom in preparing opcode, address and data.

CLK is a “don't care” if CS is low (device deselected). If CS is high, but the Start condition has not been detected (DI = 0), any number of clock cycles can be received by the device without changing its status (i.e., waiting for a Start condition).

CLK cycles are not required during the self-timed write (i.e., auto erase/write) cycle.

After detection of a Start condition the specified number of clock cycles (respectively low-to-high transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address and data bits before an instruction is executed. CLK and DI then become “don't care” inputs waiting for a new Start condition to be detected.

3.3 Data In (DI)

Data In (DI) is used to clock in a Start bit, opcode, address and data, synchronously with the CLK input.

3.4 Data Out (DO)

Data Out (DO) is used in the Read mode to output data synchronously with the CLK input (T_{PD} after the positive edge of CLK).

This pin also provides Ready/Busy status information during erase and write cycles. Ready/Busy status information is available on the DO pin if CS is brought high after being low for minimum Chip Select low time (T_{CSL}), and an erase or write operation has been initiated.

The Status signal is not available on DO if CS is held low during the entire erase or write cycle. In this case, DO is in the High-Z mode. If status is checked after the erase/write cycle, the data line will be high to indicate the device is ready.

Note: After a programming cycle is complete, issuing a Start bit and then taking CS low will clear the Ready/Busy status from DO.

3.5 Organization (ORG)

When the ORG pin is connected to Vcc or logic high, the (x16) memory organization is selected. When the ORG pin is tied to Vss or logic low, the (x8) memory organization is selected. For proper operation, ORG must be tied to a valid logic level.

93XX86A devices are always (x8) organization and 93XX86B devices are always (x16) organization.

3.6 Program Enable (PE)

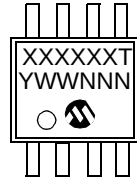
This pin allows the user to enable or disable the ability to write data to the memory array. If the PE pin is tied to V_{CC}, the device can be programmed. If the PE pin is tied to V_{SS}, programming will be inhibited. This pin cannot be floated, it must be tied to V_{CC} or V_{SS}. PE is not available on 93XX86A or 93XX86B. On those devices, programming is always enabled.

93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

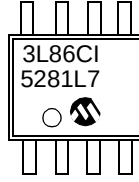
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

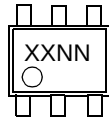
8-Lead MSOP (150 mil)



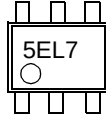
Example:



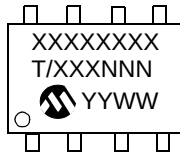
6-Lead SOT-23



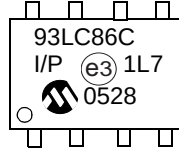
Example:



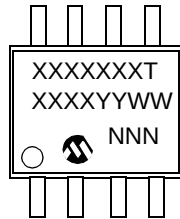
8-Lead PDIP



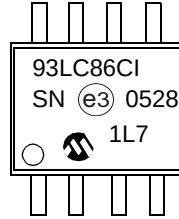
Example:



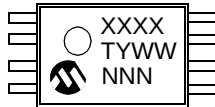
8-Lead SOIC



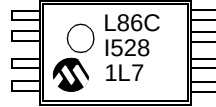
Example:



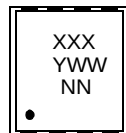
8-Lead TSSOP



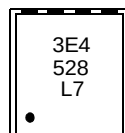
Example:



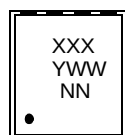
8-Lead 2x3 DFN



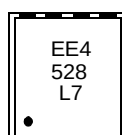
Example:



8-Lead 2x3 TDFN



Example:



93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

Part Number	1st Line Marking Codes							
	TSSOP	MSOP	SOT-23		DFN		TDFN	
			I Temp.	E Temp.	I Temp.	E Temp.	I Temp.	E Temp.
93AA86A	A86A	3A86AT	5BNN	—	—	—	—	—
93AA86B	A86B	3A86BT	5LNN	—	—	—	—	—
93AA86C	A86C	3A86CT	—	—	3E1	—	EE1	—
93LC86A	L86A	3L86AT	5ENN	5FNN	—	—	—	—
93LC86B	L86B	3L86BT	5PNN	5RNN	—	—	—	—
93LC86C	L86C	3L86CT	—	—	3E4	—	EE4	EE5
93C86A	C86A	3C86AT	5HNN	5JNN	—	—	—	—
93C86B	C86B	3C86BT	5TNN	5UNN	—	—	—	—
93C86C	C86C	3C86CT	—	—	3E7	—	EE7	EE8

Note: T = Temperature grade (I, E)
 NN = Alphanumeric traceability code

Legend: XX...X Part number or part number code
 T Temperature (I, E)
 Y Year code (last digit of calendar year)
 YY Year code (last 2 digits of calendar year)
 WW Week code (week of January 1 is week '01')
 NNN Alphanumeric traceability code (2 characters for small packages)
 Ⓔ3 Pb-free JEDEC designator for Matte Tin (Sn)

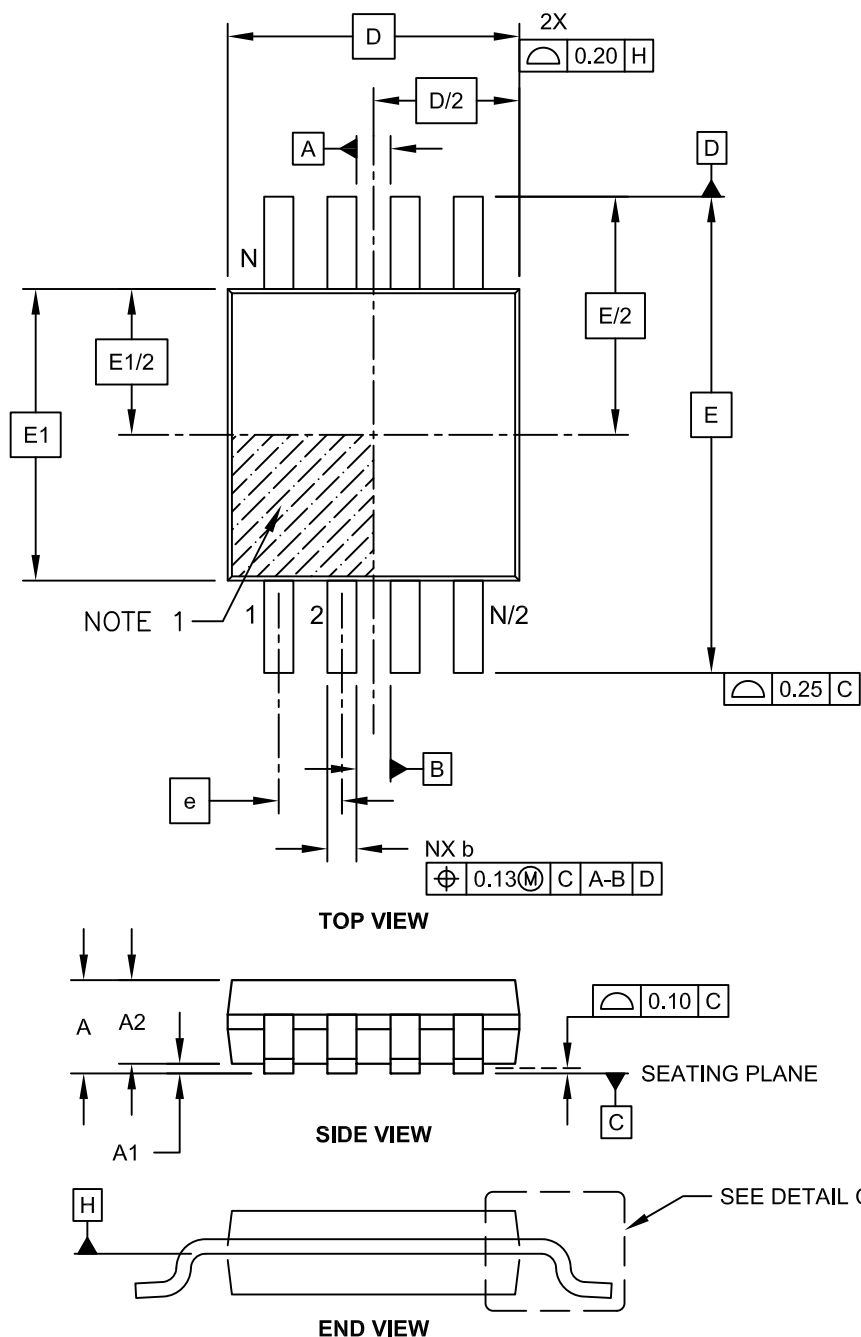
Note: For very small packages with no room for the Pb-free JEDEC designator Ⓔ3, the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

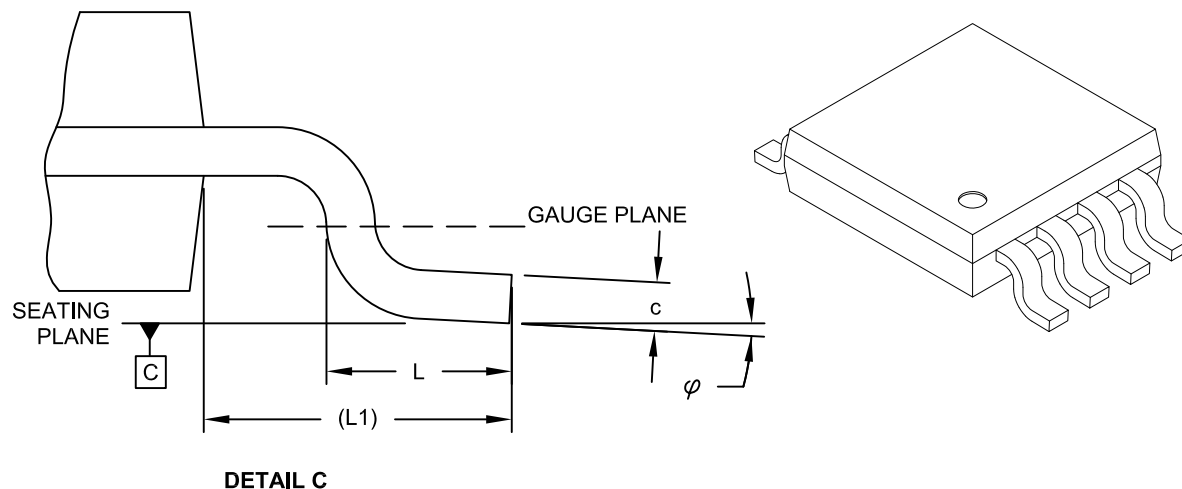


Microchip Technology Drawing C04-111C Sheet 1 of 2

93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e	0.65 BSC		
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E	4.90 BSC		
Molded Package Width	E1	3.00 BSC		
Overall Length	D	3.00 BSC		
Foot Length	L	0.40	0.60	0.80
Footprint	L1	0.95 REF		
Foot Angle	ϕ	0°	-	8°
Lead Thickness	c	0.08	-	0.23
Lead Width	b	0.22	-	0.40

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

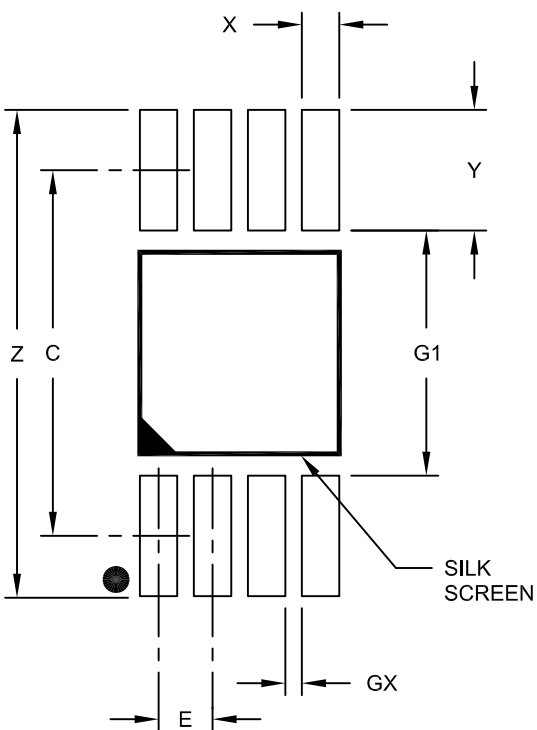
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111C Sheet 2 of 2

93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.85
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G1	2.95		
Distance Between Pads	GX	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

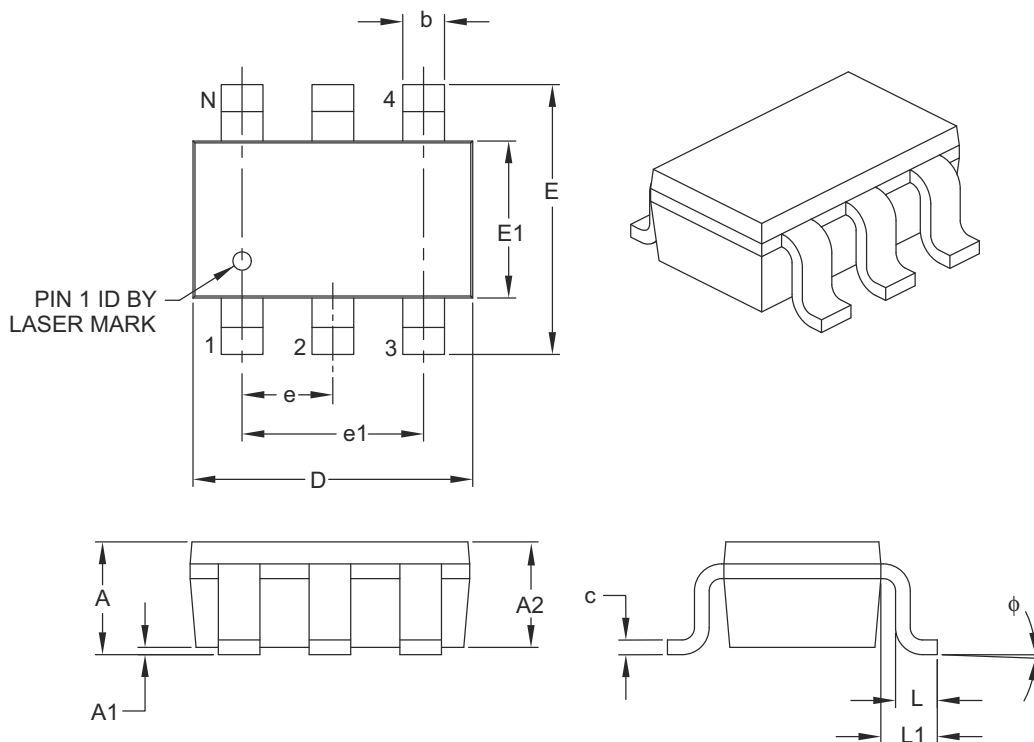
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2111A

93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

6-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	6		
Pitch	e	0.95 BSC		
Outside Lead Pitch	e1	1.90 BSC		
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	φ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

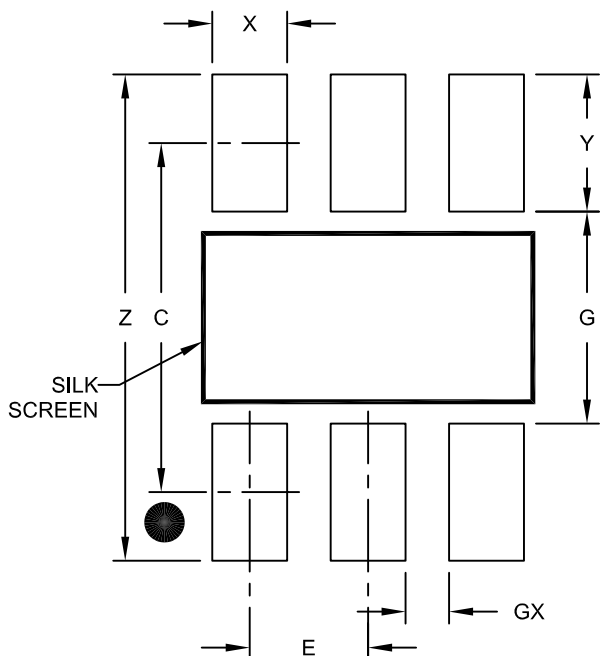
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-028B

93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

6-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.95 BSC		
Contact Pad Spacing	C		2.80	
Contact Pad Width (X6)	X			0.60
Contact Pad Length (X6)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

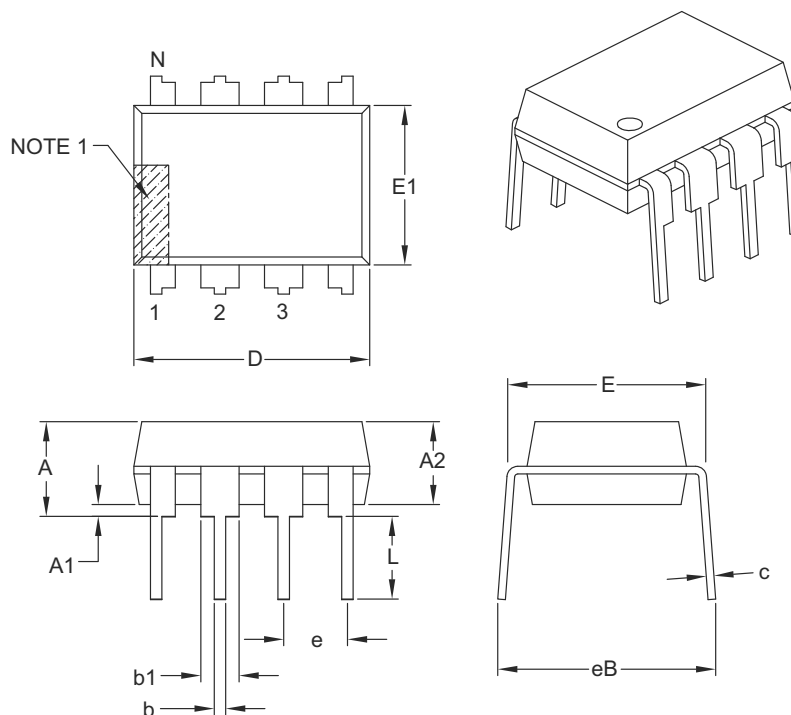
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2028A

93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	INCHES		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	.100 BSC		
Top to Seating Plane	A	—	—	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	—	—
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	—	—	.430

Notes:

- Pin 1 visual index feature may vary, but must be located with the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.

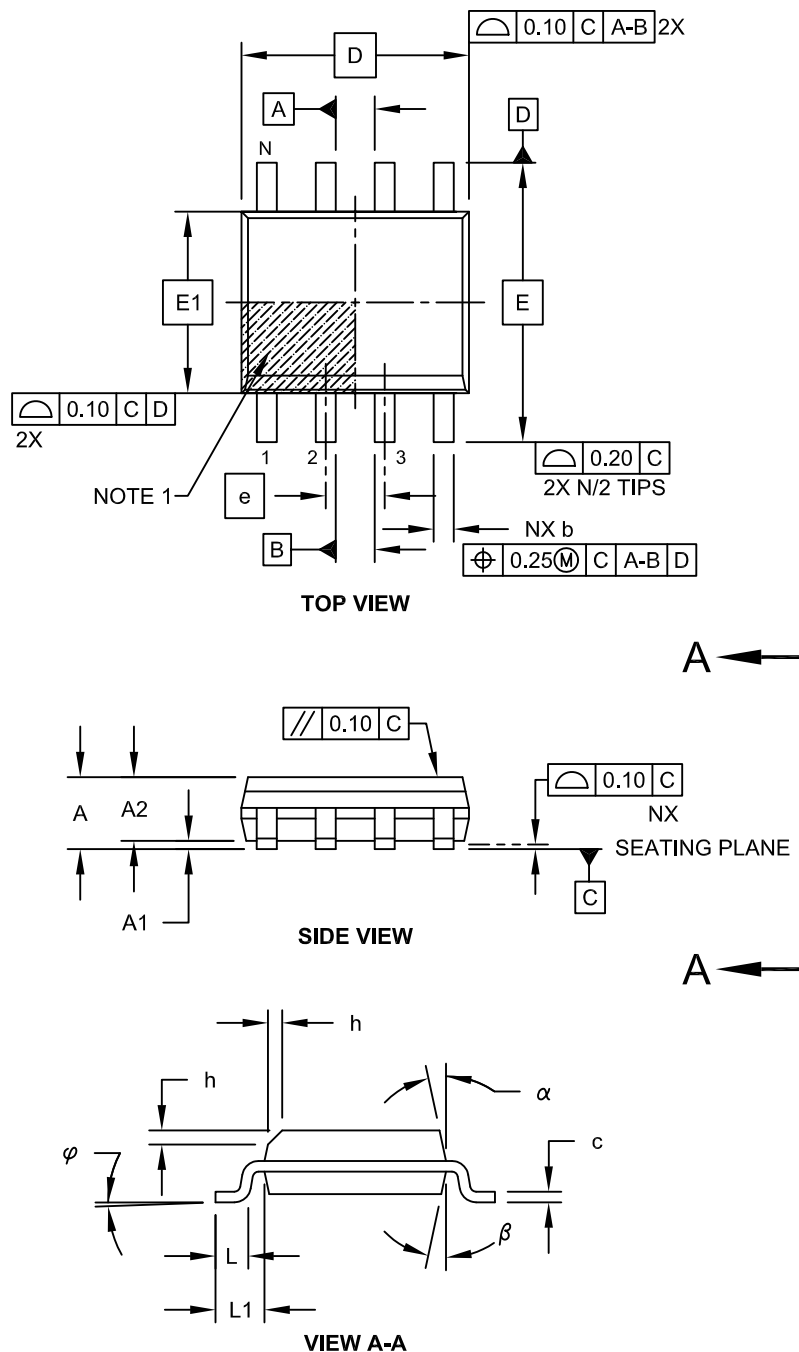
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

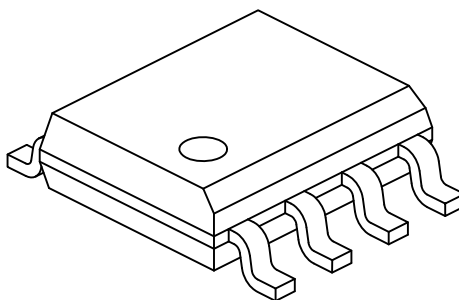


Microchip Technology Drawing No. C04-057C Sheet 1 of 2

93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

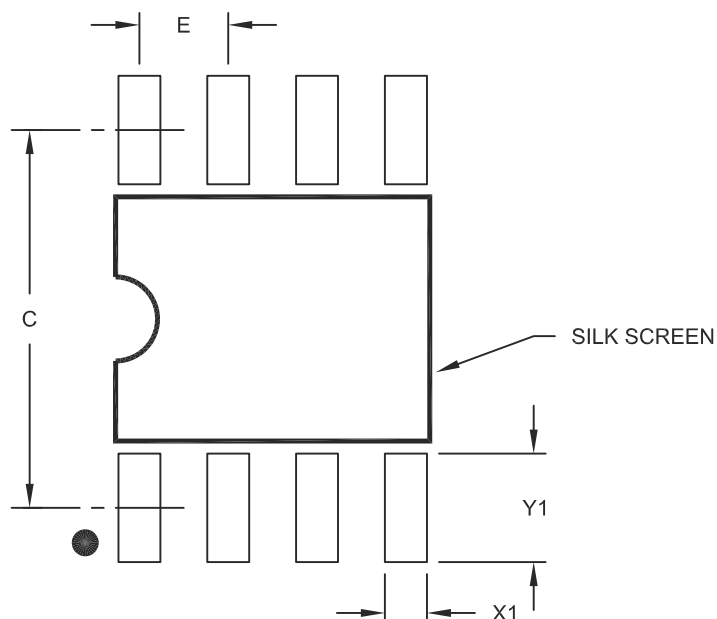
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

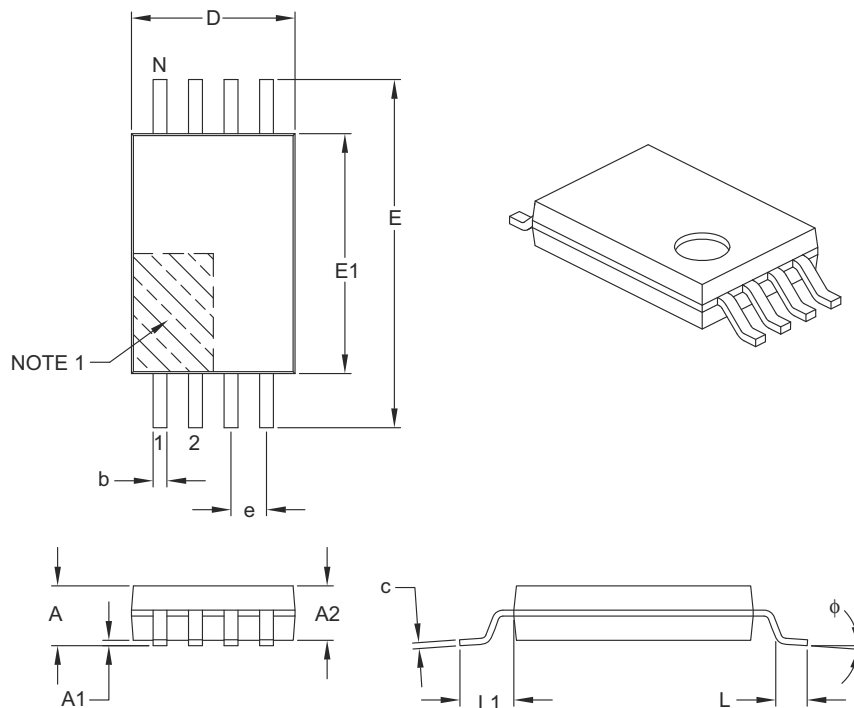
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E	6.40 BSC		
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	2.90	3.00	3.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

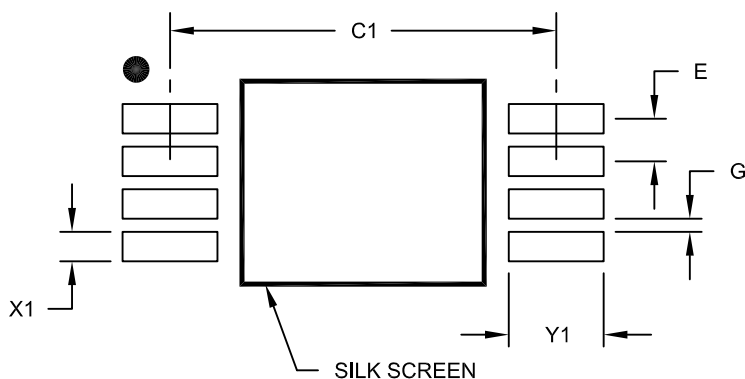
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086B

93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

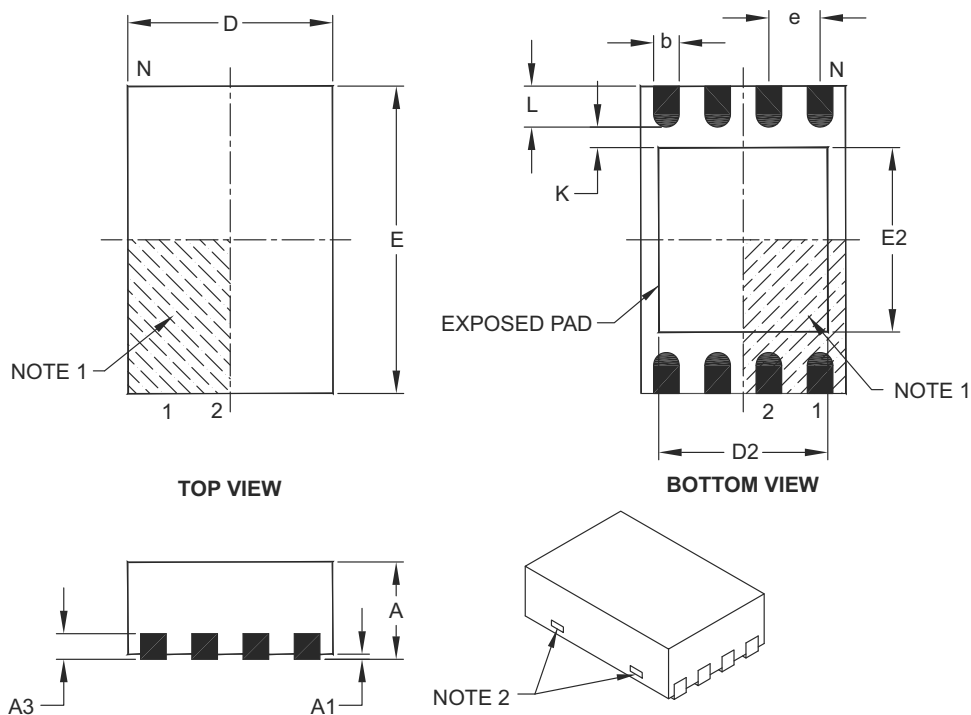
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2086A

93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Length	D	2.00 BSC		
Overall Width	E	3.00 BSC		
Exposed Pad Length	D2	1.30	–	1.55
Exposed Pad Width	E2	1.50	–	1.75
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package may have one or more exposed tie bars at ends.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

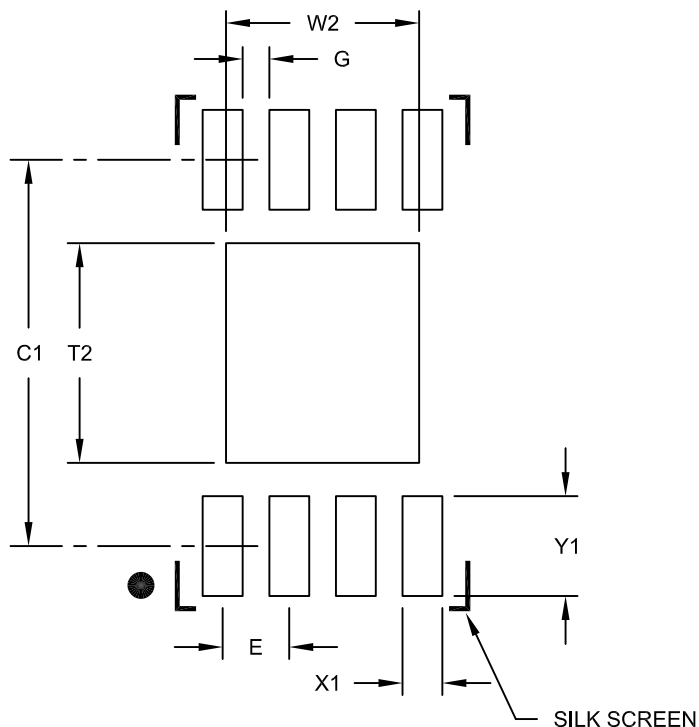
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-123C

93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

8-Lead Plastic Dual Flat, No Lead Package (MC) - 2x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	W2			1.45
Optional Center Pad Length	T2			1.75
Contact Pad Spacing	C1		2.90	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

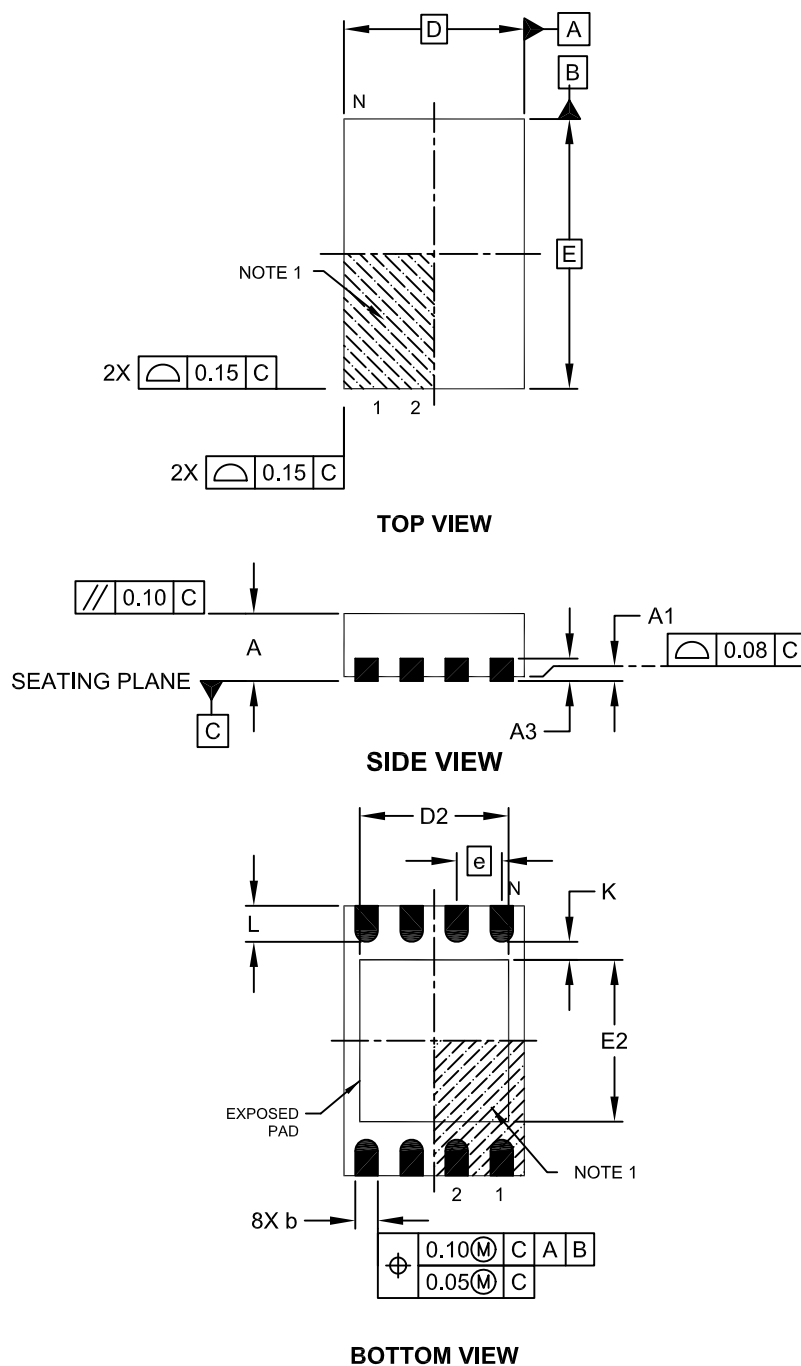
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2123B

93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

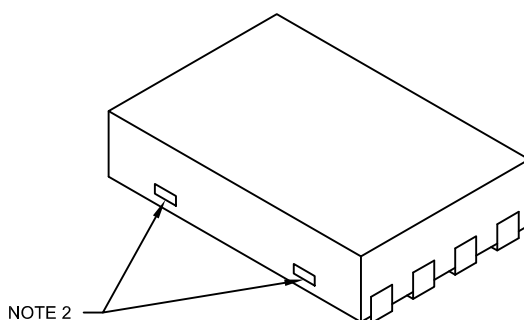


Microchip Technology Drawing No. C04-129C Sheet 1 of 2

93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Pins	N		8		
Pitch	e		0.50 BSC		
Overall Height	A		0.70	0.75	0.80
Standoff	A1		0.00	0.02	0.05
Contact Thickness	A3		0.20 REF		
Overall Length	D		2.00 BSC		
Overall Width	E		3.00 BSC		
Exposed Pad Length	D2		1.20	-	1.60
Exposed Pad Width	E2		1.20	-	1.60
Contact Width	b		0.20	0.25	0.30
Contact Length	L		0.25	0.30	0.45
Contact-to-Exposed Pad	K		0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

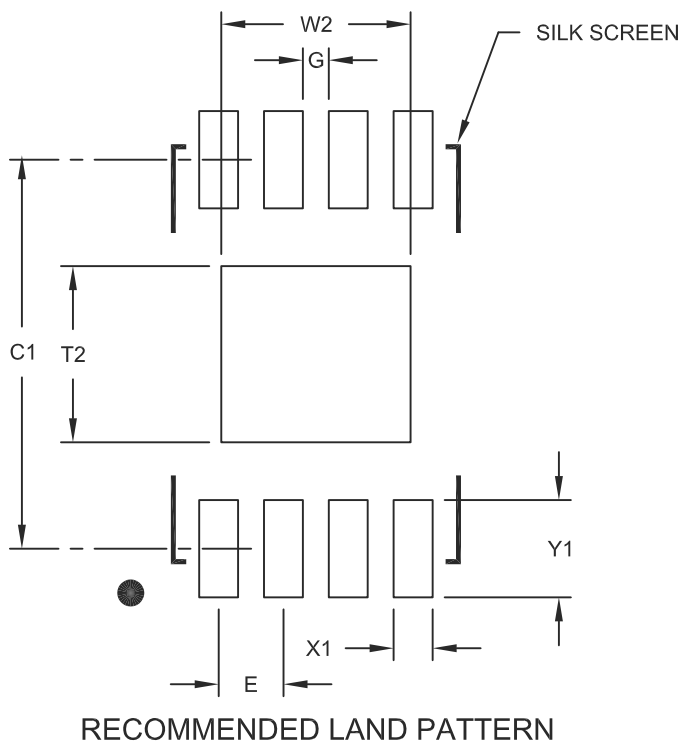
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-129C Sheet 2 of 2

93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75 mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	W2			1.46
Optional Center Pad Length	T2			1.36
Contact Pad Spacing	C1		3.00	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2129A

APPENDIX A: REVISION HISTORY

Revision A (5/2003)

Initial Release.

Revision B (7/2003)

Revised DC Char. Param. D8; Revised Figures 2.1, 2.2, 2.6, 2.7; Revised Section 3.6; Revised Product ID System.

Revision C (12/2003)

Corrections to Section 1.0, Electrical Characteristics. Section 4.1, 6-Lead SOT-23 package to OT.

Revision D (2/2004)

Corrections to Device Selection Table, Table 1-1, Table 1-2, Section 2.4, Section 2.5, Section 2.8 and Section 2.9. Added note to Figure 2-7.

Revision E (3/2005)

Added DFN package.

Revision F (4/2005)

Added notes throughout.

Revision G (1/2006)

Revised note in Sections 2.8 and 2.9.
Replaced DFN package drawing.

Revision H (10/2007)

Added SN package to Device Selection Table; Revised Pin Function Table; Revised Package Types; Revised Table 3-1; Replaced Package Drawings; Revised Product ID System.

Revision J (5/2008)

Revised Figures 2-1, 2-2, 2-6 and 2-7; Revised Package Marking Information; Replaced Package Drawings.

Revision K (1/2012)

Added TDFN package; Revised Product ID System.

Revision L (04/2012)

Revised Device Selection Table; Added Note 1 to Package Types Diagram; Revised Marking Code table; Revised Product ID System.

93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

NOTES:

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at www.microchip.com. Under "Support", click on "Customer Change Notification" and follow the registration instructions.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support
- Development Systems Information Line

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: <http://microchip.com/support>

93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this document.

TO: Technical Publications Manager Total Pages Sent _____

RE: Reader Response

From: Name _____

Company _____

Address _____

City / State / ZIP / Country _____

Telephone: (____) _____ - _____ FAX: (____) _____ - _____

Application (optional):

Would you like a reply? __Y__ __N__

Device: 93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

Literature Number: DS21797L

Questions:

1. What are the best features of this document?

2. How does this document meet your hardware and software development needs?

3. Do you find the organization of this document easy to follow? If not, why?

4. What additions to the document do you think would enhance the structure and subject?

5. What deletions from the document could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?

93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>X</u>	<u>/XX</u>
Device	Tape & Reel	Temperature Range	Package
Device:			
93AA86A:	16K	1.8V	Microwire Serial EEPROM (x8)
93AA86B:	16K	1.8V	Microwire Serial EEPROM (x16)
93AA86C:	16K	1.8V	Microwire Serial EEPROM w/ORG
93LC86A:	16K	2.5V	Microwire Serial EEPROM (x8)
93LC86B:	16K	2.5V	Microwire Serial EEPROM (x16)
93LC86C:	16K	2.5V	Microwire Serial EEPROM w/ORG
93C86A:	16K	5.0V	Microwire Serial EEPROM (x8)
93C86B:	16K	5.0V	Microwire Serial EEPROM (x16)
93C86C:	16K	5.0V	Microwire Serial EEPROM w/ORG
Tape & Reel:			
Blank	=	Standard packaging	
T	=	Tape & Reel	
Temperature Range:			
I	=	-40°C to +85°C	
E	=	-40°C to +125°C	
Package:			
MS	=	Plastic MSOP (Micro Small outline, 8-lead)	
OT	=	Plastic SOT-23, 6-lead (Tape & Reel only)	
P	=	Plastic DIP (300 mil body), 8-lead	
SN	=	Plastic SOIC (3.90 mm body), 8-lead	
ST	=	Plastic TSSOP (4.4 mm body), 8-lead	
MC	=	Plastic DFN (2x3x0.90 mm body), 8-lead	
MNY ⁽¹⁾	=	Plastic TDFN (2x3x0.75 mm body), 8-lead (Tape & Reel only)	
Note 1: "Y" indicates a Nickel Palladium Gold (NiPdAu) finish.			
Examples:			
a) 93AA86C-I/P: 16K, 2048x8 or 1024x16 Serial EEPROM, PDIP package, 1.8V			
b) 93AA86AT-I/OT: 16K, 2048x8 Serial EEPROM, SOT-23 package, tape and reel, 1.8V			
c) 93AA86CT-I/MS: 16K, 2048x8 or 1024x16 Serial EEPROM, MSOP package, tape and reel, 1.8V			
a) 93LC86C-I/ST: 16K, 2048x8, 1024x16 Serial EEPROM, TSSOP package, 2.5V			
b) 93LC86BT-I/OT: 16K, 1024x16 Serial EEPROM, SOT-23 package, tape and reel, 2.5V			
c) 93LC86CT-E/MNY: 16K, 2048x8 or 1024x16 Serial EEPROM, Automotive temp, TDFN package, tape and reel, 2.5V			
a) 93C86C-I/MS: 16K, 2048x8 or 1024x16 Serial EEPROM, MSOP package, 5.0V			
b) 93C86AT-I/OT: 16K, 2048x8 Serial EEPROM, SOT-23 package, tape and reel, 5.0V			

93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, dsPIC, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, PIC³² logo, rfPIC and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MXDEV, MXLAB, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, Mindi, MiWi, MPASM, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Omniscent Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICKit, PICtail, REAL ICE, rfLAB, Select Mode, Total Endurance, TSHARC, UniWinDriver, WiperLock and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2012, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.

ISBN: 9781620762165

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
= ISO/TS 16949 =

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://www.microchip.com/support>
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Hangzhou
Tel: 86-571-2819-3187
Fax: 86-571-2819-3189

China - Hong Kong SAR
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Osaka
Tel: 81-66-152-7160
Fax: 81-66-152-9310

Japan - Yokohama
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-536-4818
Fax: 886-7-330-9305

Taiwan - Taipei
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820