

# Single Supply 3.0 V to 44 V, Low Power Operational Amplifiers

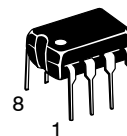
## MC33171, 2, 4, NCV33172, 4

Quality bipolar fabrication with innovative design concepts are employed for the MC33171/72/74, NCV33172/74 series of monolithic operational amplifiers. These devices operate at 180  $\mu$ A per amplifier and offer 1.8 MHz of gain bandwidth product and 2.1 V/ $\mu$ s slew rate without the use of JFET device technology. Although this series can be operated from split supplies, it is particularly suited for single supply operation, since the common mode input voltage includes ground potential ( $V_{EE}$ ). With a Darlington input stage, these devices exhibit high input resistance, low input offset voltage and high gain. The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, provides high capacitance drive capability, excellent phase and gain margins, low open loop high frequency output impedance and symmetrical source/sink AC frequency response.

The MC33171/72/74, NCV33172/74 are specified over the industrial/automotive temperature ranges. The complete series of single, dual and quad operational amplifiers are available in plastic as well as the surface mount packages.

### Features

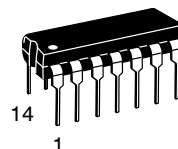
- Low Supply Current: 180  $\mu$ A (Per Amplifier)
- Wide Supply Operating Range: 3.0 V to 44 V or  $\pm 1.5$  V to  $\pm 22$  V
- Wide Input Common Mode Range, Including Ground ( $V_{EE}$ )
- Wide Bandwidth: 1.8 MHz
- High Slew Rate: 2.1 V/ $\mu$ s
- Low Input Offset Voltage: 2.0 mV
- Large Output Voltage Swing:  $-14.2$  V to  $+14.2$  V (with  $\pm 15$  V Supplies)
- Large Capacitance Drive Capability: 0 pF to 500 pF
- Low Total Harmonic Distortion: 0.03%
- Excellent Phase Margin: 60°
- Excellent Gain Margin: 15 dB
- Output Short Circuit Protection
- ESD Diodes Provide Input Protection for Dual and Quad
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



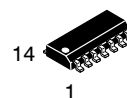
PDIP-8  
P SUFFIX  
CASE 626



SO-8  
D, VD SUFFIX  
CASE 751



PDIP-14  
P, VP SUFFIX  
CASE 646



SO-14  
D, VD SUFFIX  
CASE 751A



TSSOP-14  
DTB SUFFIX  
CASE 948G

### ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

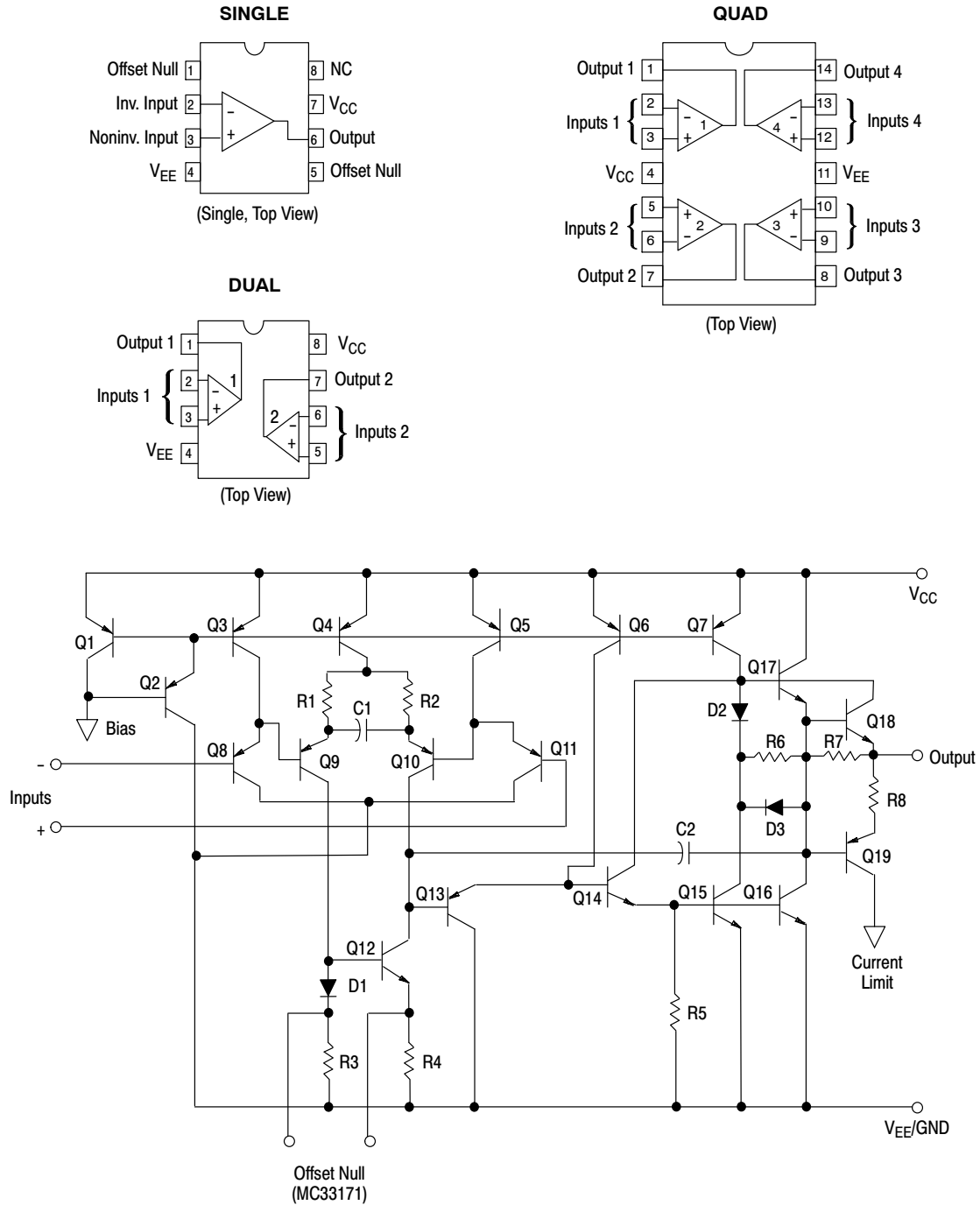
NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 9.

### DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 10 of this data sheet.

# MC33171, 2, 4, NCV33172, 4

## PIN CONNECTIONS



**Figure 1. Representative Schematic Diagram**  
(Each Amplifier)

# MC33171, 2, 4, NCV33172, 4

## MAXIMUM RATINGS

| Rating                                 | Symbol          | Value       | Unit |
|----------------------------------------|-----------------|-------------|------|
| Supply Voltage                         | $V_{CC}/V_{EE}$ | $\pm 22$    | V    |
| Input Differential Voltage Range       | $V_{IDR}$       | (Note 1)    | V    |
| Input Voltage Range                    | $V_{IR}$        | (Note 1)    | V    |
| Output Short Circuit Duration (Note 2) | $t_{SC}$        | Indefinite  | sec  |
| Operating Ambient Temperature Range    | $T_A$           | (Note 3)    | °C   |
| Operating Junction Temperature         | $T_J$           | +150        | °C   |
| Storage Temperature Range              | $T_{stg}$       | -65 to +150 | °C   |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## DC ELECTRICAL CHARACTERISTICS ( $V_{CC} = +15$ V, $V_{EE} = -15$ V, $R_L$ connected to ground, $T_A = +25$ °C, unless otherwise noted.)

| Characteristics                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Symbol                                                   | Min                                                          | Typ                                        | Max                                       | Unit             |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------|--------------------------------------------------------------|--------------------------------------------|-------------------------------------------|------------------|
| Input Offset Voltage ( $V_{CM} = 0$ V)<br>$V_{CC} = +15$ V, $V_{EE} = -15$ V, $T_A = +25$ °C<br>$V_{CC} = +5.0$ V, $V_{EE} = 0$ V, $T_A = +25$ °C<br>$V_{CC} = +15$ V, $V_{EE} = -15$ V, $T_A = T_{low}$ to $T_{high}$ (Note 3)                                                                                                                                                                                                                                                                | $V_{IO}$                                                 | –<br>–<br>–                                                  | 2.0<br>2.5<br>–                            | 4.5<br>5.0<br>6.5                         | mV               |
| Average Temperature Coefficient of Offset Voltage                                                                                                                                                                                                                                                                                                                                                                                                                                              | $\Delta V_{IO}/\Delta T$                                 | –                                                            | 10                                         | –                                         | $\mu V/^\circ C$ |
| Input Bias Current ( $V_{CM} = 0$ V)<br>$T_A = +25$ °C<br>$T_A = T_{low}$ to $T_{high}$ (Note 3)                                                                                                                                                                                                                                                                                                                                                                                               | $I_{IB}$                                                 | –<br>–                                                       | 20<br>–                                    | 100<br>200                                | nA               |
| Input Offset Current ( $V_{CM} = 0$ V)<br>$T_A = +25$ °C<br>$T_A = T_{low}$ to $T_{high}$ (Note 3)                                                                                                                                                                                                                                                                                                                                                                                             | $I_{IO}$                                                 | –<br>–                                                       | 5.0<br>–                                   | 20<br>40                                  | nA               |
| Large Signal Voltage Gain ( $V_O = \pm 10$ V, $R_L = 10$ k)<br>$T_A = +25$ °C<br>$T_A = T_{low}$ to $T_{high}$ (Note 3)                                                                                                                                                                                                                                                                                                                                                                        | $A_{VOL}$                                                | 50<br>25                                                     | 500<br>–                                   | –<br>–                                    | V/mV             |
| Output Voltage Swing<br>$V_{CC} = +5.0$ V, $V_{EE} = 0$ V, $R_L = 10$ k, $T_A = +25$ °C<br>$V_{CC} = +15$ V, $V_{EE} = -15$ V, $R_L = 10$ k, $T_A = +25$ °C<br>$V_{CC} = +15$ V, $V_{EE} = -15$ V, $R_L = 10$ k, $T_A = T_{low}$ to $T_{high}$ (Note 3)<br><br>$V_{CC} = +5.0$ V, $V_{EE} = 0$ V, $R_L = 10$ k, $T_A = +25$ °C<br>$V_{CC} = +15$ V, $V_{EE} = -15$ V, $R_L = 10$ k, $T_A = +25$ °C<br>$V_{CC} = +15$ V, $V_{EE} = -15$ V, $R_L = 10$ k, $T_A = T_{low}$ to $T_{high}$ (Note 3) | $V_{OH}$<br><br><br><br><br>$V_{OL}$<br><br><br><br><br> | 3.5<br>13.6<br>13.3<br><br>–<br>–<br>–                       | 4.3<br>14.2<br>–<br><br>0.05<br>–14.2<br>– | –<br>–<br>–<br><br>0.15<br>–13.6<br>–13.3 | V                |
| Output Short Circuit ( $T_A = +25$ °C)<br>Input Overdrive = 1.0 V, Output to Ground<br>Source<br>Sink                                                                                                                                                                                                                                                                                                                                                                                          | $I_{SC}$                                                 | 3.0<br>15                                                    | 5.0<br>27                                  | –<br>–                                    | mA               |
| Input Common Mode Voltage Range<br>$T_A = +25$ °C<br>$T_A = T_{low}$ to $T_{high}$ (Note 3)                                                                                                                                                                                                                                                                                                                                                                                                    | $V_{ICR}$                                                | $V_{EE}$ to $(V_{CC} - 1.8)$<br>$V_{EE}$ to $(V_{CC} - 2.2)$ |                                            |                                           | V                |
| Common Mode Rejection Ratio ( $R_S \leq 10$ k), $T_A = +25$ °C                                                                                                                                                                                                                                                                                                                                                                                                                                 | CMRR                                                     | 80                                                           | 90                                         | –                                         | dB               |
| Power Supply Rejection Ratio ( $R_S = 100 \Omega$ ), $T_A = +25$ °C                                                                                                                                                                                                                                                                                                                                                                                                                            | PSRR                                                     | 80                                                           | 100                                        | –                                         | dB               |
| Power Supply Current (Per Amplifier)<br>$V_{CC} = +5.0$ V, $V_{EE} = 0$ V, $T_A = +25$ °C<br>$V_{CC} = +15$ V, $V_{EE} = -15$ V, $T_A = +25$ °C<br>$V_{CC} = +15$ V, $V_{EE} = -15$ V, $T_A = T_{low}$ to $T_{high}$ (Note 3)                                                                                                                                                                                                                                                                  | $I_D$                                                    | –<br>–<br>–                                                  | 180<br>220<br>–                            | 250<br>250<br>300                         | $\mu A$          |

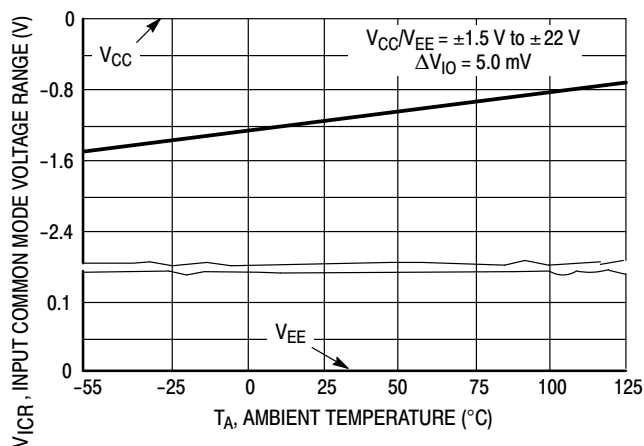
1. Either or both input voltages must not exceed the magnitude of  $V_{CC}$  or  $V_{EE}$ .
2. Power dissipation must be considered to ensure maximum junction temperature ( $T_J$ ) is not exceeded.
3. MC3317x  $T_{low} = -40$  °C  $T_{high} = +85$  °C  
MC3317xV, NCV3317x  $T_{low} = -40$  °C  $T_{high} = +125$  °C

# MC33171, 2, 4, NCV33172, 4

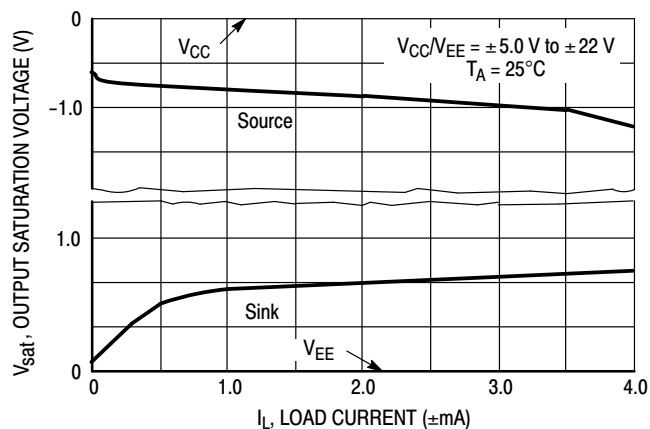
**AC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = +15\text{ V}$ ,  $V_{EE} = -15\text{ V}$ ,  $R_L$  connected to ground,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

| Characteristics                                                                                                                           | Symbol   | Min      | Typ        | Max    | Unit                   |
|-------------------------------------------------------------------------------------------------------------------------------------------|----------|----------|------------|--------|------------------------|
| Slew Rate ( $V_{in} = -10\text{ V to } +10\text{ V}$ , $R_L = 10\text{ k}$ , $C_L = 100\text{ pF}$ )<br>$A_V +1$<br>$A_V -1$              | SR       | 1.6<br>– | 2.1<br>2.1 | –<br>– | V/ $\mu\text{s}$       |
| Gain Bandwidth Product ( $f = 100\text{ kHz}$ )                                                                                           | GBW      | 1.4      | 1.8        | –      | MHz                    |
| Power Bandwidth<br>$A_V = +1.0$ , $R_L = 10\text{ k}$ , $V_O = 20\text{ V}_{pp}$ , THD = 5%                                               | BWp      | –        | 35         | –      | kHz                    |
| Phase Margin<br>$R_L = 10\text{ k}$<br>$R_L = 10\text{ k}$ , $C_L = 100\text{ pF}$                                                        | $\phi_m$ | –<br>–   | 60<br>45   | –<br>– | Deg                    |
| Gain Margin<br>$R_L = 10\text{ k}$<br>$R_L = 10\text{ k}$ , $C_L = 100\text{ pF}$                                                         | $A_m$    | –<br>–   | 15<br>5.0  | –<br>– | dB                     |
| Equivalent Input Noise Voltage<br>$R_S = 100\ \Omega$ , $f = 1.0\text{ kHz}$                                                              | $e_n$    | –        | 32         | –      | nV/ $\sqrt{\text{Hz}}$ |
| Equivalent Input Noise Current ( $f = 1.0\text{ kHz}$ )                                                                                   | $I_n$    | –        | 0.2        | –      | pA/ $\sqrt{\text{Hz}}$ |
| Differential Input Resistance<br>$V_{cm} = 0\text{ V}$                                                                                    | $R_{in}$ | –        | 300        | –      | M $\Omega$             |
| Input Capacitance                                                                                                                         | $C_{in}$ | –        | 0.8        | –      | pF                     |
| Total Harmonic Distortion<br>$A_V = +10$ , $R_L = 10\text{ k}$ , $2.0\text{ V}_{pp} \leq V_O \leq 20\text{ V}_{pp}$ , $f = 10\text{ kHz}$ | THD      | –        | 0.03       | –      | %                      |
| Channel Separation ( $f = 10\text{ kHz}$ )                                                                                                | CS       | –        | 120        | –      | dB                     |
| Open Loop Output Impedance ( $f = 1.0\text{ MHz}$ )                                                                                       | $z_o$    | –        | 100        | –      | $\Omega$               |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.



**Figure 2. Input Common Mode Voltage Range versus Temperature**



**Figure 3. Split Supply Output Saturation versus Load Current**

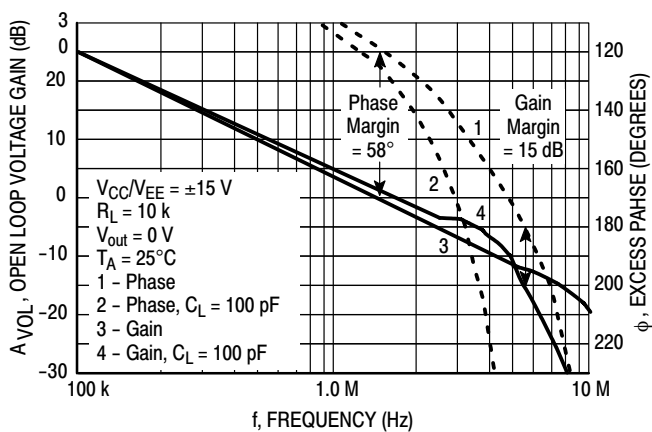


Figure 4. Open Loop Voltage Gain and Phase versus Frequency

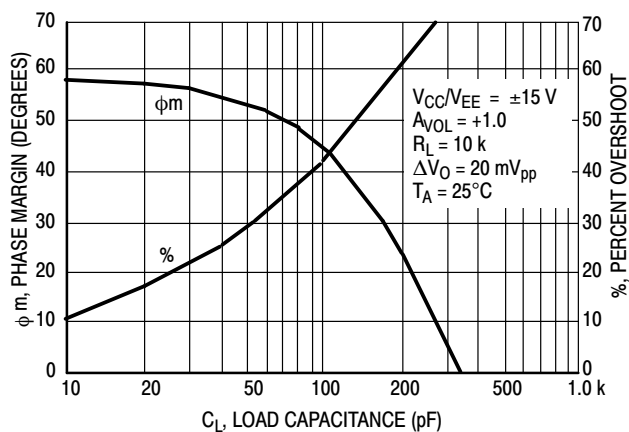


Figure 5. Phase Margin and Percent Overshoot versus Load Capacitance

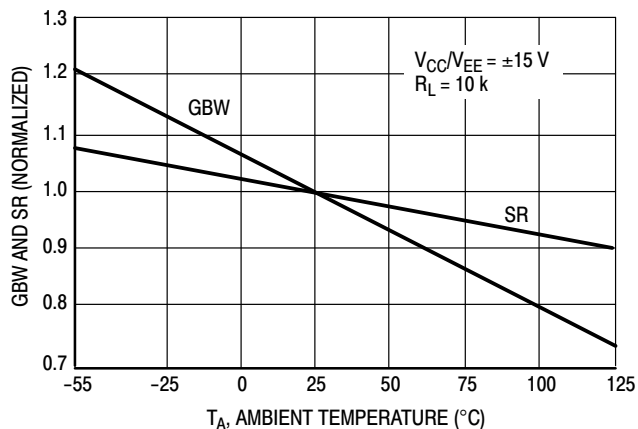


Figure 6. Normalized Gain Bandwidth Product and Slew Rate versus Temperature

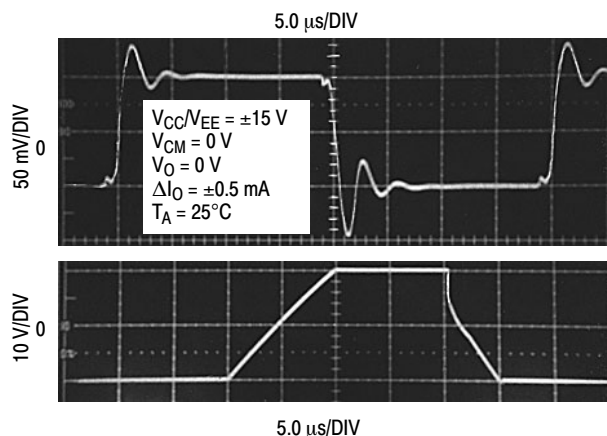


Figure 7. Small and Large Signal Transient Response

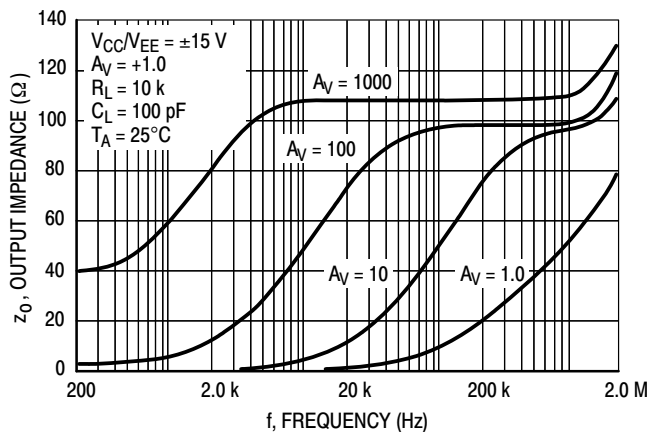


Figure 8. Output Impedance and Frequency

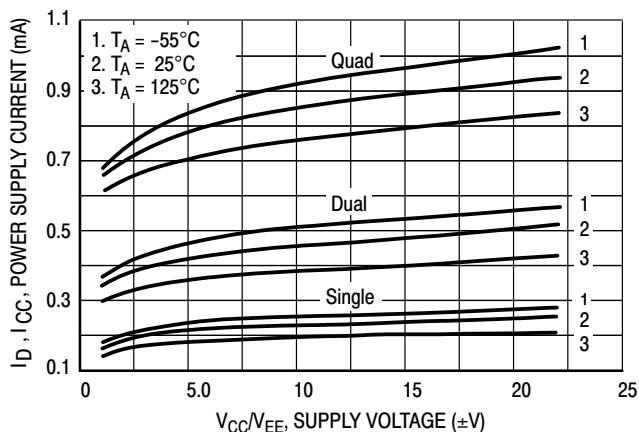


Figure 9. Supply Current versus Supply Voltage

## APPLICATIONS INFORMATION – CIRCUIT DESCRIPTION/PERFORMANCE FEATURES

Although the bandwidth, slew rate, and settling time of the MC33171/72/74 amplifier family is similar to low power op amp products utilizing JFET input devices, these amplifiers offer additional advantages as a result of the PNP transistor differential inputs and an all NPN transistor output stage.

Because the input common mode voltage range of this input stage includes the  $V_{EE}$  potential, single supply operation is feasible to as low as 3.0 V with the common mode input voltage at ground potential.

The input stage also allows differential input voltages up to  $\pm 44$  V, provided the maximum input voltage range is not exceeded. Specifically, the input voltages must range between  $V_{CC}$  and  $V_{EE}$  supply voltages as shown by the maximum rating table. In practice, although *not recommended*, the input voltages can exceed the  $V_{CC}$  voltage by approximately 3.0 V and decrease below the  $V_{EE}$  voltage by 0.3 V without causing product damage, although output phase reversal may occur. It is also possible to source up to 5.0 mA of current from  $V_{EE}$  through either inputs' clamping diode without damage or latching, but phase reversal may again occur. If at least one input is within the common mode input voltage range and the other input is within the maximum input voltage range, no phase reversal will occur. If both inputs exceed the upper common mode input voltage limit, the output will be forced to its lowest voltage state.

Since the input capacitance associated with the small geometry input device is substantially lower (0.8 pF) than that of a typical JFET (3.0 pF), the frequency response for a given input source resistance is greatly enhanced. This becomes evident in D-to-A current to voltage conversion applications where the feedback resistance can form a pole with the input capacitance of the op amp. This input pole creates a 2nd Order system with the single pole op amp and is therefore detrimental to its settling time. In this context, lower input capacitance is desirable especially for higher values of feedback resistances (lower current DACs). This input pole can be compensated for by creating a feedback zero with a capacitance across the feedback resistance, if necessary, to reduce overshoot. For 10 k $\Omega$  of feedback resistance, the MC33171/72/74 family can typically settle to within 1/2 LSB of 8 bits in 4.2  $\mu$ s, and within 1/2 LSB of 12 bits in 4.8  $\mu$ s for a 10 V step. In a standard inverting unity gain fast settling configuration, the symmetrical slew rate is typically  $\pm 2.1$  V/ $\mu$ s. In the classic noninverting unity gain configuration the typical output positive slew rate is also 2.1 V/ $\mu$ s, and the corresponding negative slew rate will usually exceed the positive slew rate as a function of the fall time of the input waveform.

The all NPN output stage, shown in its basic form on the equivalent circuit schematic, offers unique advantages over the more conventional NPN/PNP transistor Class AB output stage. A 10 k $\Omega$  load resistance can typically swing within

0.8 V of the positive rail ( $V_{CC}$ ) and negative rail ( $V_{EE}$ ), providing a 28.4 Vpp swing from  $\pm 15$  V supplies. This large output swing becomes most noticeable at lower supply voltages.

The positive swing is limited by the saturation voltage of the current source transistor Q7, the  $V_{BE}$  of the NPN pull-up transistor Q17, and the voltage drop associated with the short circuit resistance, R5. For sink currents less than 0.4 mA, the negative swing is limited by the saturation voltage of the pull-down transistor Q15, and the voltage drop across R4 and R5. For small valued sink currents, the above voltage drops are negligible, allowing the negative swing voltage to approach within millivolts of  $V_{EE}$ . For sink currents ( $> 0.4$  mA), diode D3 clamps the voltage across R4. Thus the negative swing is limited by the saturation voltage of Q15, plus the forward diode drop of D3 ( $\approx V_{EE} + 1.0$  V). Therefore an unprecedented peak-to-peak output voltage swing is possible for a given supply voltage as indicated by the output swing specifications.

If the load resistance is referenced to  $V_{CC}$  instead of ground for single supply applications, the maximum possible output swing can be achieved for a given supply voltage. For light load currents, the load resistance will pull the output to  $V_{CC}$  during the positive swing and the output will pull the load resistance near ground during the negative swing. The load resistance value should be much less than that of the feedback resistance to maximize pull-up capability.

Because the PNP output emitter-follower transistor has been eliminated, the MC33171/72/74 family offers a 15 mA minimum current sink capability, typically to an output voltage of ( $V_{EE} + 1.8$  V). In single supply applications the output can directly source or sink base current from a common emitter NPN transistor for current switching applications.

In addition, the all NPN transistor output stage is inherently faster than PNP types, contributing to the bipolar amplifier's improved gain bandwidth product. The associated high frequency low output impedance (200  $\Omega$  typ @ 1.0 MHz) allows capacitive drive capability from 0 pF to 400 pF without oscillation in the noninverting unity gain configuration. The 60° phase margin and 15 dB gain margin, as well as the general gain and phase characteristics, are virtually independent of the source/sink output swing conditions. This allows easier system phase compensation, since output swing will not be a phase consideration. The AC characteristics of the MC33171/72/74 family also allow excellent active filter capability, especially for low voltage single supply applications.

Although the single supply specification is defined at 5.0 V, these amplifiers are functional to at least 3.0 V @ 25 °C. However slight changes in parametrics such as bandwidth, slew rate, and DC gain may occur.

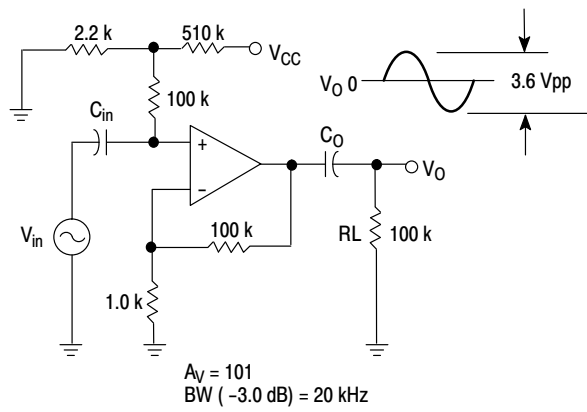
If power to this integrated circuit is applied in reverse polarity, or if the IC is installed backwards in a socket, large unlimited current surges will occur through the device that may result in device destruction.

As usual with most high frequency amplifiers, proper lead dress, component placement and PC board layout should be exercised for optimum frequency performance. For example, long unshielded input or output leads may result in unwanted input/output coupling. In order to preserve the relatively low input capacitance associated with these amplifiers, resistors connected to the inputs should be immediately adjacent to the input pin to minimize additional stray input capacitance. This not only minimizes the input

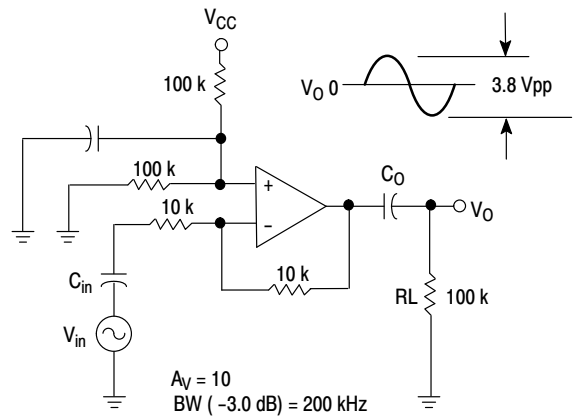
pole for optimum frequency response, but also minimizes extraneous “pick up” at this node. Supply decoupling with adequate capacitance immediately adjacent to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit great impedance changes over temperature.

The output of any one amplifier is current limited and thus protected from a direct short to ground. However, under such conditions, it is important not to allow the device to exceed the maximum junction temperature rating. Typically for  $\pm 15$  V supplies, any one output can be shorted continuously to ground without exceeding the maximum temperature rating.

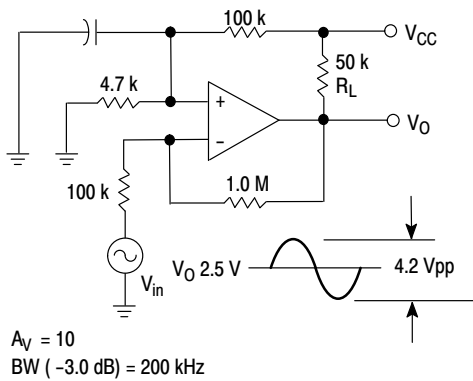
## MC33171, 2, 4, NCV33172, 4



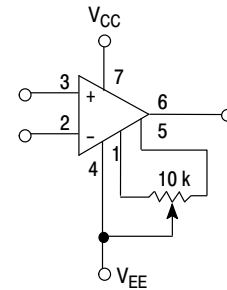
**Figure 10. AC Coupled Noninverting Amplifier with Single +5.0 V Supply**



**Figure 11. AC Coupled Inverting Amplifier with Single +5.0 V Supply**

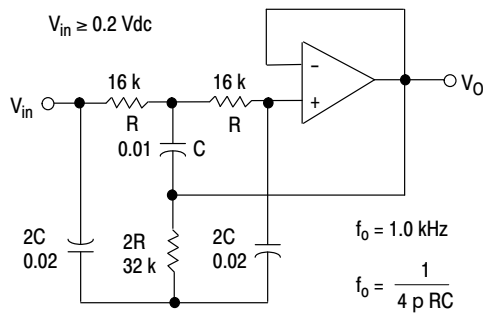


**Figure 12. DC Coupled Inverting Amplifier Maximum Output Swing with Single +5.0 V Supply**

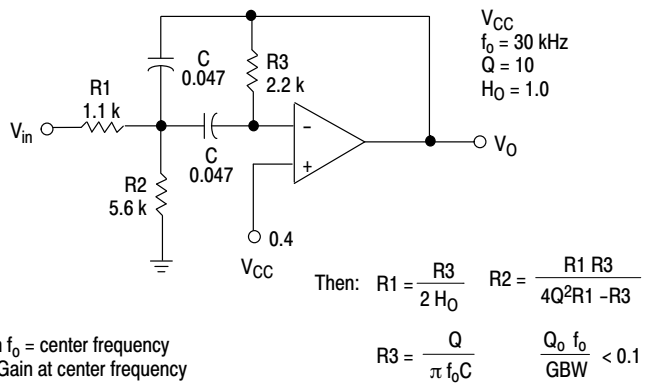


Offset Nulling range is approximately  $\pm 80 \text{ mV}$  with a 10 k potentiometer, MC33171 only.

**Figure 13. Offset Nulling Circuit**



**Figure 14. Active High-Q Notch Filter**



**Figure 15. Active Bandpass Filter**

## MC33171, 2, 4, NCV33172, 4

### ORDERING INFORMATION

| Op Amp Function | Device          | Operating Temperature Range        | Package            | Shipping <sup>†</sup> |
|-----------------|-----------------|------------------------------------|--------------------|-----------------------|
| Single          | MC33171DR2G     | T <sub>A</sub> = -40 °C to +85 °C  | SO-8 (Pb-Free)     | 2500 / Tape & Reel    |
| Dual            | MC33172DR2G     | T <sub>A</sub> = -40 °C to +85 °C  | SO-8 (Pb-Free)     | 2500 / Tape & Reel    |
|                 | MC33172VDR2G    | T <sub>A</sub> = -40 °C to +125 °C | SO-8 (Pb-Free)     | 2500 / Tape & Reel    |
|                 | NCV33172DR2G*   |                                    | SO-8 (Pb-Free)     | 2500 / Tape & Reel    |
| Quad            | MC33174DR2G     | T <sub>A</sub> = -40 °C to +85 °C  | SO-14 (Pb-Free)    | 2500 / Tape & Reel    |
|                 | MC33174DTBR2G   |                                    | TSSOP-14 (Pb-Free) | 2500 / Tape & Reel    |
|                 | MC33174VDR2G    | T <sub>A</sub> = -40 °C to +125 °C | SO-14 (Pb-Free)    | 2500 / Tape & Reel    |
|                 | NCV33174DTBR2G* |                                    | TSSOP-14 (Pb-Free) | 2500 / Tape & Reel    |

### DISCONTINUED (Note 4)

|        |             |                                    |                    |               |
|--------|-------------|------------------------------------|--------------------|---------------|
| Single | MC33171DG   | T <sub>A</sub> = -40 °C to +85 °C  | SO-8 (Pb-Free)     | 98 Units/Rail |
| Single | MC33171PG   | T <sub>A</sub> = -40 °C to +85 °C  | PDIP (Pb-Free)     | 50 Units/Rail |
| Dual   | MC33172DG   | T <sub>A</sub> = -40 °C to +85 °C  | SO-8 (Pb-Free)     | 98 Units/Rail |
| Dual   | MC33172PG   | T <sub>A</sub> = -40 °C to +85 °C  | PDIP (Pb-Free)     | 50 Units/Rail |
| Dual   | MC33172VDG  | T <sub>A</sub> = -40 °C to +125 °C | SO-8 (Pb-Free)     | 98 Units/Rail |
| Quad   | MC33174DG   | T <sub>A</sub> = -40 °C to +85 °C  | SO-14 (Pb-Free)    | 55 Units/Rail |
| Quad   | MC33174DTBG | T <sub>A</sub> = -40 °C to +85 °C  | TSSOP-14 (Pb-Free) | 96 Units/Rail |
| Quad   | MC33174PG   | T <sub>A</sub> = -40 °C to +85 °C  | PDIP (Pb-Free)     | 25 Units/Rail |
| Quad   | MC33174VDG  | T <sub>A</sub> = -40 °C to +125 °C | SO-14 (Pb-Free)    | 55 Units/Rail |
| Quad   | MC33174VPG  | T <sub>A</sub> = -40 °C to +125 °C | PDIP (Pb-Free)     | 25 Units/Rail |

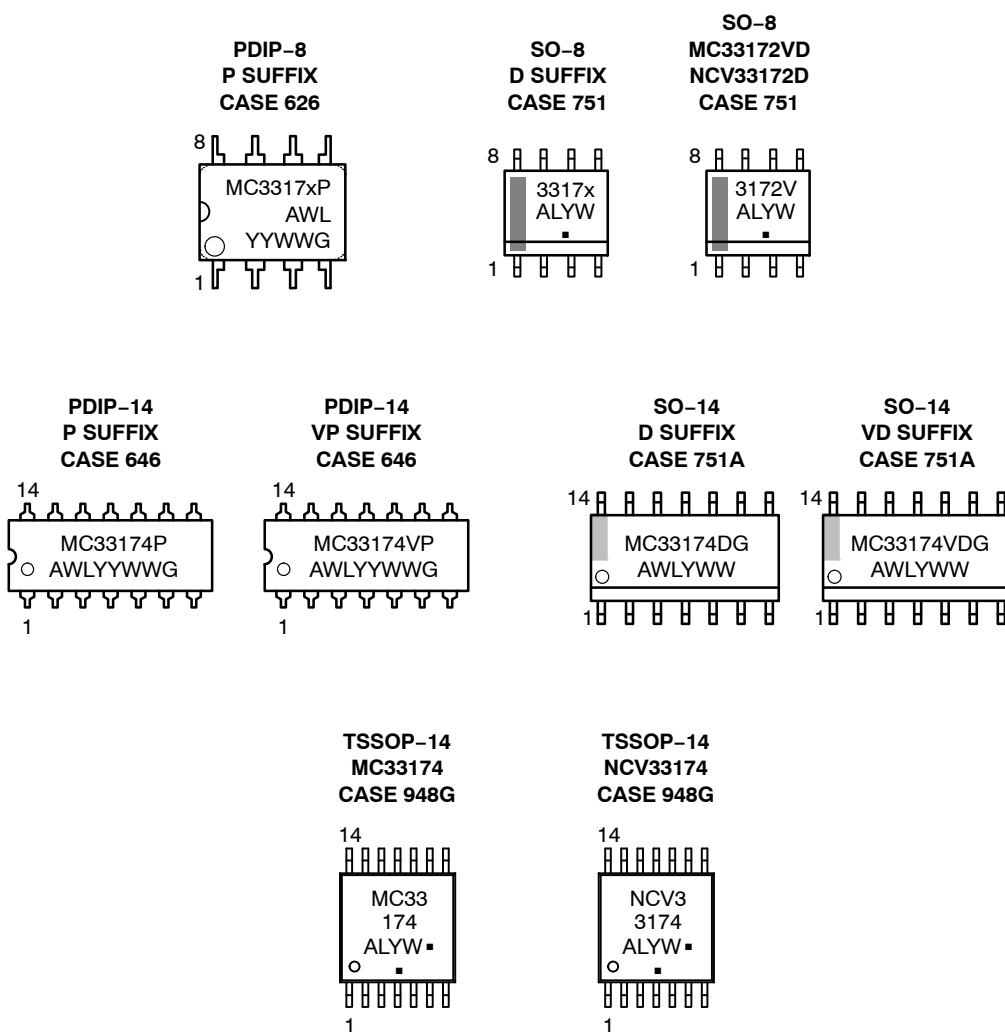
<sup>†</sup> For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

\* NCV prefix for automotive and other applications requiring site and change controls.

4. **DISCONTINUED:** These devices are not available. Please contact your **onsemi** representative for information. The most current information on these devices may be available on [www.onsemi.com](http://www.onsemi.com).

# MC33171, 2, 4, NCV33172, 4

## MARKING DIAGRAMS



x = 1 or 2  
 A = Assembly Location  
 WL, L = Wafer Lot  
 YY, Y = Year  
 WW, W = Work Week  
 G or ■ = Pb-Free Package  
 (Note: Microdot may be in either location)

## MC33171, 2, 4, NCV33172, 4

### REVISION HISTORY

| Revision | Description of Changes                                                                                                                                                                                 | Date       |
|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|
| 14       | Rebranded the Data Sheet to <b>onsemi</b> format.<br>MC33171DG, MC33171PG, MC33172DG, MC33172PG, MC33172VDG, MC33174DG,<br>MC33174DTBG, MC33174PG, MC33174VDG, MC33174VPG OPNs Marked as Discontinued. | 07/31/2025 |

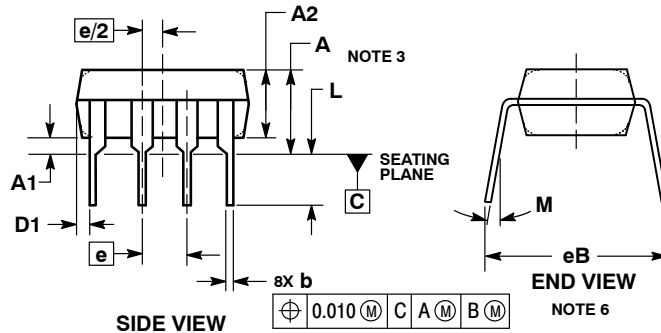
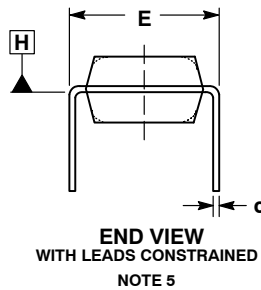
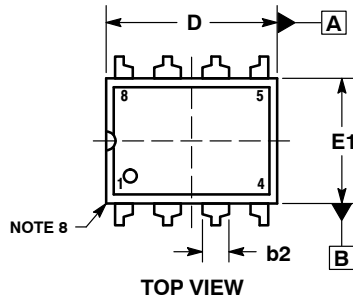
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



SCALE 1:1

PDIP-8  
CASE 626-05  
ISSUE P

DATE 22 APR 2015

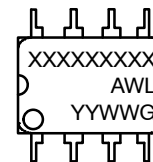


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

|     | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
| DIM | MIN       | MAX   | MIN         | MAX   |
| A   | ---       | 0.210 | ---         | 5.33  |
| A1  | 0.015     | ---   | 0.38        | ---   |
| A2  | 0.115     | 0.195 | 2.92        | 4.95  |
| b   | 0.014     | 0.022 | 0.35        | 0.56  |
| b2  | 0.060 TYP | ---   | 1.52 TYP    | ---   |
| C   | 0.008     | 0.014 | 0.20        | 0.36  |
| D   | 0.355     | 0.400 | 9.02        | 10.16 |
| D1  | 0.005     | ---   | 0.13        | ---   |
| E   | 0.300     | 0.325 | 7.62        | 8.26  |
| E1  | 0.240     | 0.280 | 6.10        | 7.11  |
| e   | 0.100 BSC | ---   | 2.54 BSC    | ---   |
| eB  | ---       | 0.430 | ---         | 10.92 |
| L   | 0.115     | 0.150 | 2.92        | 3.81  |
| M   | ---       | 10°   | ---         | 10°   |

GENERIC  
MARKING DIAGRAM\*



- XXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

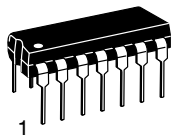
\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

- PIN 1. AC IN  
2. DC + IN  
3. DC - IN  
4. AC IN  
5. GROUND  
6. OUTPUT  
7. AUXILIARY  
8. V<sub>CC</sub>

|                  |             |                                                                                                                                                                                     |
|------------------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DOCUMENT NUMBER: | 98ASB42420B | Electronic versions are uncontrolled except when accessed directly from the Document Repository.<br>Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION:     | PDIP-8      | PAGE 1 OF 1                                                                                                                                                                         |

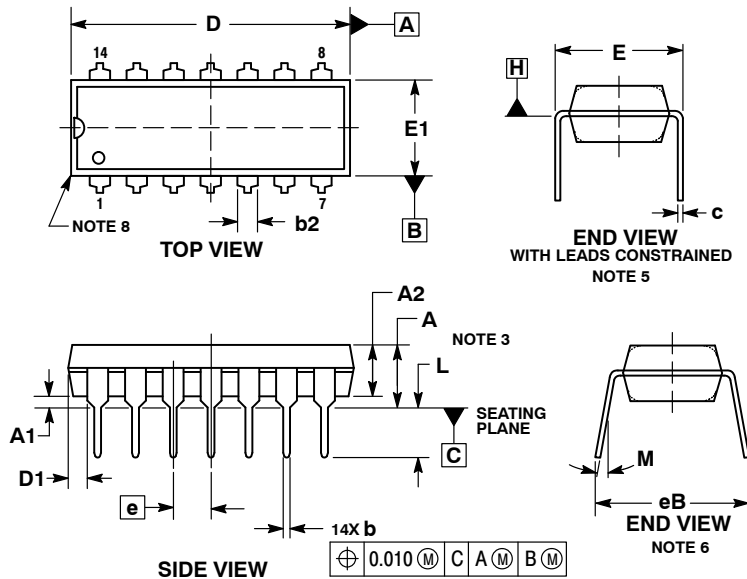
onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.



SCALE 1:1

**PDIP-14**  
**CASE 646-06**  
**ISSUE 5**

DATE 22 APR 2015



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

| DIM | INCHES             |       | MILLIMETERS |       |
|-----|--------------------|-------|-------------|-------|
|     | MIN                | MAX   | MIN         | MAX   |
| A   | ---                | 0.210 | ---         | 5.33  |
| A1  | 0.015              | ---   | 0.38        | ---   |
| A2  | 0.115              | 0.195 | 2.92        | 4.95  |
| b   | 0.014              | 0.022 | 0.35        | 0.56  |
| b2  | 0.060 TYP 1.52 TYP |       |             |       |
| C   | 0.008              | 0.014 | 0.20        | 0.36  |
| D   | 0.735              | 0.775 | 18.67       | 19.69 |
| D1  | 0.005              | ---   | 0.13        | ---   |
| E   | 0.300              | 0.325 | 7.62        | 8.26  |
| E1  | 0.240              | 0.280 | 6.10        | 7.11  |
| e   | 0.100 BSC          |       | 2.54 BSC    |       |
| eB  | ---                | 0.430 | ---         | 10.92 |
| L   | 0.115              | 0.150 | 2.92        | 3.81  |
| M   | ---                | 10°   | ---         | 10°   |

**GENERIC**  
**MARKING DIAGRAM\***



XXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

|                         |                    |                                                                                                                                                                                     |
|-------------------------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>DOCUMENT NUMBER:</b> | <b>98ASB42428B</b> | Electronic versions are uncontrolled except when accessed directly from the Document Repository.<br>Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| <b>DESCRIPTION:</b>     | <b>PDIP-14</b>     | <b>PAGE 1 OF 2</b>                                                                                                                                                                  |

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

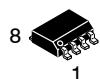
PDIP-14  
CASE 646-06  
ISSUE S

DATE 22 APR 2015

|                                                                                                                                                                                                                                                                                                           |                                                                                                                                                                                                                                                                                                                  |                                                                                                                                                                                                                                               |                                                                                                                                                                                                                                                                                                            |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| STYLE 1:<br>PIN 1. COLLECTOR<br>2. BASE<br>3. EMITTER<br>4. NO<br>CONNECTION<br>5. EMITTER<br>6. BASE<br>7. COLLECTOR<br>8. COLLECTOR<br>9. BASE<br>10. EMITTER<br>11. NO<br>CONNECTION<br>12. EMITTER<br>13. BASE<br>14. COLLECTOR                                                                       | STYLE 2:<br>CANCELLED                                                                                                                                                                                                                                                                                            | STYLE 3:<br>CANCELLED                                                                                                                                                                                                                         | STYLE 4:<br>PIN 1. DRAIN<br>2. SOURCE<br>3. GATE<br>4. NO<br>CONNECTION<br>5. GATE<br>6. SOURCE<br>7. DRAIN<br>8. DRAIN<br>9. SOURCE<br>10. GATE<br>11. NO<br>CONNECTION<br>12. GATE<br>13. SOURCE<br>14. DRAIN                                                                                            |
| STYLE 5:<br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE<br>4. NO CONNECTION<br>5. SOURCE<br>6. DRAIN<br>7. GATE<br>8. GATE<br>9. DRAIN<br>10. SOURCE<br>11. NO CONNECTION<br>12. SOURCE<br>13. DRAIN<br>14. GATE                                                                                                 | STYLE 6:<br>PIN 1. COMMON CATHODE<br>2. ANODE/CATHODE<br>3. ANODE/CATHODE<br>4. NO CONNECTION<br>5. ANODE/CATHODE<br>6. NO CONNECTION<br>7. ANODE/CATHODE<br>8. ANODE/CATHODE<br>9. ANODE/CATHODE<br>10. NO CONNECTION<br>11. ANODE/CATHODE<br>12. ANODE/CATHODE<br>13. NO CONNECTION<br>14. COMMON ANODE        | STYLE 7:<br>PIN 1. NO CONNECTION<br>2. ANODE<br>3. ANODE<br>4. NO CONNECTION<br>5. ANODE<br>6. NO CONNECTION<br>7. ANODE<br>8. ANODE<br>9. ANODE<br>10. NO CONNECTION<br>11. ANODE<br>12. ANODE<br>13. NO CONNECTION<br>14. COMMON<br>CATHODE | STYLE 8:<br>PIN 1. NO CONNECTION<br>2. CATHODE<br>3. CATHODE<br>4. NO CONNECTION<br>5. CATHODE<br>6. NO CONNECTION<br>7. CATHODE<br>8. CATHODE<br>9. CATHODE<br>10. NO CONNECTION<br>11. CATHODE<br>12. CATHODE<br>13. NO CONNECTION<br>14. COMMON ANODE                                                   |
| STYLE 9:<br>PIN 1. COMMON CATHODE<br>2. ANODE/CATHODE<br>3. ANODE/CATHODE<br>4. NO CONNECTION<br>5. ANODE/CATHODE<br>6. ANODE/CATHODE<br>7. COMMON ANODE<br>8. COMMON ANODE<br>9. ANODE/CATHODE<br>10. ANODE/CATHODE<br>11. NO CONNECTION<br>12. ANODE/CATHODE<br>13. ANODE/CATHODE<br>14. COMMON CATHODE | STYLE 10:<br>PIN 1. COMMON<br>CATHODE<br>2. ANODE/CATHODE<br>3. ANODE/CATHODE<br>4. ANODE/CATHODE<br>5. ANODE/CATHODE<br>6. NO CONNECTION<br>7. COMMON ANODE<br>8. COMMON<br>CATHODE<br>9. ANODE/CATHODE<br>10. ANODE/CATHODE<br>11. ANODE/CATHODE<br>12. ANODE/CATHODE<br>13. NO CONNECTION<br>14. COMMON ANODE | STYLE 11:<br>PIN 1. CATHODE<br>2. CATHODE<br>3. CATHODE<br>4. CATHODE<br>5. CATHODE<br>6. CATHODE<br>7. CATHODE<br>8. ANODE<br>9. ANODE<br>10. ANODE<br>11. ANODE<br>12. ANODE<br>13. ANODE<br>14. ANODE                                      | STYLE 12:<br>PIN 1. COMMON CATHODE<br>2. COMMON ANODE<br>3. ANODE/CATHODE<br>4. ANODE/CATHODE<br>5. ANODE/CATHODE<br>6. COMMON ANODE<br>7. COMMON CATHODE<br>8. ANODE/CATHODE<br>9. ANODE/CATHODE<br>10. ANODE/CATHODE<br>11. ANODE/CATHODE<br>12. ANODE/CATHODE<br>13. ANODE/CATHODE<br>14. ANODE/CATHODE |

|                  |             |                                                                                                                                                                                     |
|------------------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DOCUMENT NUMBER: | 98ASB42428B | Electronic versions are uncontrolled except when accessed directly from the Document Repository.<br>Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION:     | PDIP-14     | PAGE 2 OF 2                                                                                                                                                                         |

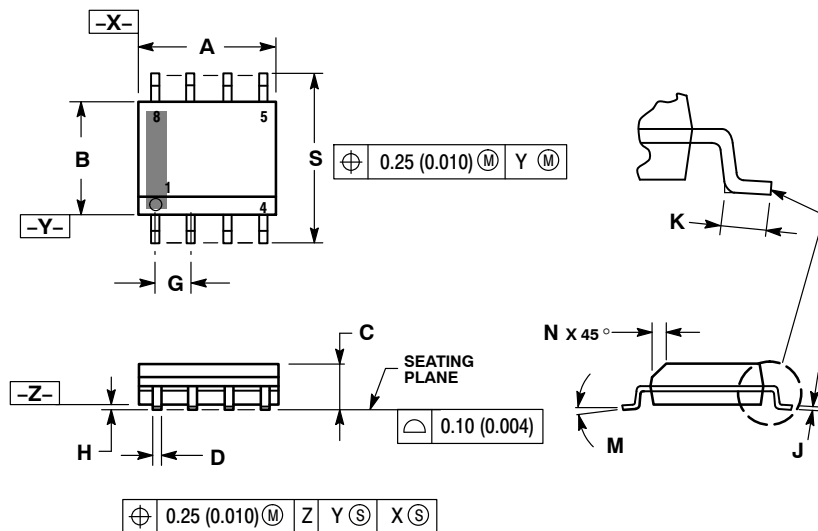
onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.



SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

DATE 16 FEB 2011

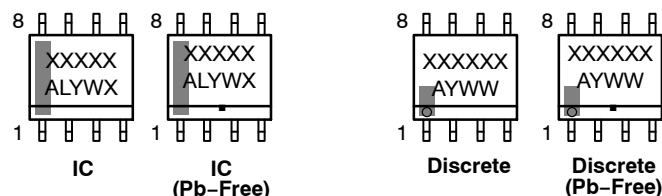
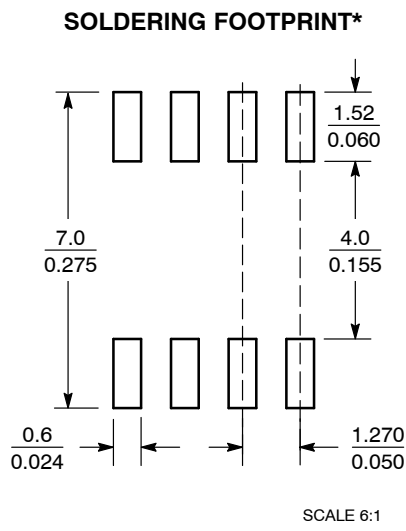


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.80        | 5.00 | 0.189     | 0.197 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.053     | 0.069 |
| D   | 0.33        | 0.51 | 0.013     | 0.020 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 0.10        | 0.25 | 0.004     | 0.010 |
| J   | 0.19        | 0.25 | 0.007     | 0.010 |
| K   | 0.40        | 1.27 | 0.016     | 0.050 |
| M   | 0°          | 8°   | 0°        | 8°    |
| N   | 0.25        | 0.50 | 0.010     | 0.020 |
| S   | 5.80        | 6.20 | 0.228     | 0.244 |

GENERIC  
MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

|                  |             |                                                                                                                                                                                     |
|------------------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DOCUMENT NUMBER: | 98ASB42564B | Electronic versions are uncontrolled except when accessed directly from the Document Repository.<br>Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION:     | SOIC-8 NB   | PAGE 1 OF 2                                                                                                                                                                         |

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

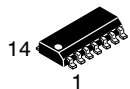
**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

|                                                                                                                                                                                                   |                                                                                                                                                                                          |                                                                                                                                                                                    |                                                                                                                                                                                                        |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>STYLE 1:</b><br>PIN 1. EMITTER<br>2. COLLECTOR<br>3. COLLECTOR<br>4. EMITTER<br>5. EMITTER<br>6. BASE<br>7. BASE<br>8. EMITTER                                                                 | <b>STYLE 2:</b><br>PIN 1. COLLECTOR, DIE, #1<br>2. COLLECTOR, #1<br>3. COLLECTOR, #2<br>4. COLLECTOR, #2<br>5. BASE, #2<br>6. EMITTER, #2<br>7. BASE, #1<br>8. EMITTER, #1               | <b>STYLE 3:</b><br>PIN 1. DRAIN, DIE #1<br>2. DRAIN, #1<br>3. DRAIN, #2<br>4. DRAIN, #2<br>5. GATE, #2<br>6. SOURCE, #2<br>7. GATE, #1<br>8. SOURCE, #1                            | <b>STYLE 4:</b><br>PIN 1. ANODE<br>2. ANODE<br>3. ANODE<br>4. ANODE<br>5. ANODE<br>6. ANODE<br>7. ANODE<br>8. COMMON CATHODE                                                                           |
| <b>STYLE 5:</b><br>PIN 1. DRAIN<br>2. DRAIN<br>3. DRAIN<br>4. DRAIN<br>5. GATE<br>6. GATE<br>7. SOURCE<br>8. SOURCE                                                                               | <b>STYLE 6:</b><br>PIN 1. SOURCE<br>2. DRAIN<br>3. DRAIN<br>4. SOURCE<br>5. SOURCE<br>6. GATE<br>7. GATE<br>8. SOURCE                                                                    | <b>STYLE 7:</b><br>PIN 1. INPUT<br>2. EXTERNAL BYPASS<br>3. THIRD STAGE SOURCE<br>4. GROUND<br>5. DRAIN<br>6. GATE 3<br>7. SECOND STAGE Vd<br>8. FIRST STAGE Vd                    | <b>STYLE 8:</b><br>PIN 1. COLLECTOR, DIE #1<br>2. BASE, #1<br>3. BASE, #2<br>4. COLLECTOR, #2<br>5. COLLECTOR, #2<br>6. EMITTER, #2<br>7. EMITTER, #1<br>8. COLLECTOR, #1                              |
| <b>STYLE 9:</b><br>PIN 1. EMITTER, COMMON<br>2. COLLECTOR, DIE #1<br>3. COLLECTOR, DIE #2<br>4. EMITTER, COMMON<br>5. EMITTER, COMMON<br>6. BASE, DIE #2<br>7. BASE, DIE #1<br>8. EMITTER, COMMON | <b>STYLE 10:</b><br>PIN 1. GROUND<br>2. BIAS 1<br>3. OUTPUT<br>4. GROUND<br>5. GROUND<br>6. BIAS 2<br>7. INPUT<br>8. GROUND                                                              | <b>STYLE 11:</b><br>PIN 1. SOURCE 1<br>2. GATE 1<br>3. SOURCE 2<br>4. GATE 2<br>5. DRAIN 2<br>6. DRAIN 2<br>7. DRAIN 1<br>8. DRAIN 1                                               | <b>STYLE 12:</b><br>PIN 1. SOURCE<br>2. SOURCE<br>3. SOURCE<br>4. GATE<br>5. DRAIN<br>6. DRAIN<br>7. DRAIN<br>8. DRAIN                                                                                 |
| <b>STYLE 13:</b><br>PIN 1. N.C.<br>2. SOURCE<br>3. SOURCE<br>4. GATE<br>5. DRAIN<br>6. DRAIN<br>7. DRAIN<br>8. DRAIN                                                                              | <b>STYLE 14:</b><br>PIN 1. N-SOURCE<br>2. N-GATE<br>3. P-SOURCE<br>4. P-GATE<br>5. P-DRAIN<br>6. P-DRAIN<br>7. N-DRAIN<br>8. N-DRAIN                                                     | <b>STYLE 15:</b><br>PIN 1. ANODE 1<br>2. ANODE 1<br>3. ANODE 1<br>4. ANODE 1<br>5. CATHODE, COMMON<br>6. CATHODE, COMMON<br>7. CATHODE, COMMON<br>8. CATHODE, COMMON               | <b>STYLE 16:</b><br>PIN 1. EMITTER, DIE #1<br>2. BASE, DIE #1<br>3. EMITTER, DIE #2<br>4. BASE, DIE #2<br>5. COLLECTOR, DIE #2<br>6. COLLECTOR, DIE #2<br>7. COLLECTOR, DIE #1<br>8. COLLECTOR, DIE #1 |
| <b>STYLE 17:</b><br>PIN 1. VCC<br>2. V2OUT<br>3. V1OUT<br>4. TXE<br>5. RXE<br>6. VEE<br>7. GND<br>8. ACC                                                                                          | <b>STYLE 18:</b><br>PIN 1. ANODE<br>2. ANODE<br>3. SOURCE<br>4. GATE<br>5. DRAIN<br>6. DRAIN<br>7. CATHODE<br>8. CATHODE                                                                 | <b>STYLE 19:</b><br>PIN 1. SOURCE 1<br>2. GATE 1<br>3. SOURCE 2<br>4. GATE 2<br>5. DRAIN 2<br>6. MIRROR 2<br>7. DRAIN 1<br>8. MIRROR 1                                             | <b>STYLE 20:</b><br>PIN 1. SOURCE (N)<br>2. GATE (N)<br>3. SOURCE (P)<br>4. GATE (P)<br>5. DRAIN<br>6. DRAIN<br>7. DRAIN<br>8. DRAIN                                                                   |
| <b>STYLE 21:</b><br>PIN 1. CATHODE 1<br>2. CATHODE 2<br>3. CATHODE 3<br>4. CATHODE 4<br>5. CATHODE 5<br>6. COMMON ANODE<br>7. COMMON ANODE<br>8. CATHODE 6                                        | <b>STYLE 22:</b><br>PIN 1. I/O LINE 1<br>2. COMMON CATHODE/VCC<br>3. COMMON CATHODE/VCC<br>4. I/O LINE 3<br>5. COMMON ANODE/GND<br>6. I/O LINE 4<br>7. I/O LINE 5<br>8. COMMON ANODE/GND | <b>STYLE 23:</b><br>PIN 1. LINE 1 IN<br>2. COMMON ANODE/GND<br>3. COMMON ANODE/GND<br>4. LINE 2 IN<br>5. LINE 2 OUT<br>6. COMMON ANODE/GND<br>7. COMMON ANODE/GND<br>8. LINE 1 OUT | <b>STYLE 24:</b><br>PIN 1. BASE<br>2. EMITTER<br>3. COLLECTOR/ANODE<br>4. COLLECTOR/ANODE<br>5. CATHODE<br>6. CATHODE<br>7. COLLECTOR/ANODE<br>8. COLLECTOR/ANODE                                      |
| <b>STYLE 25:</b><br>PIN 1. VIN<br>2. N/C<br>3. REXT<br>4. GND<br>5. IOUT<br>6. IOUT<br>7. IOUT<br>8. IOUT                                                                                         | <b>STYLE 26:</b><br>PIN 1. GND<br>2. dv/dt<br>3. ENABLE<br>4. ILIMIT<br>5. SOURCE<br>6. SOURCE<br>7. SOURCE<br>8. VCC                                                                    | <b>STYLE 27:</b><br>PIN 1. ILIMIT<br>2. OVLO<br>3. UVLO<br>4. INPUT+<br>5. SOURCE<br>6. SOURCE<br>7. SOURCE<br>8. DRAIN                                                            | <b>STYLE 28:</b><br>PIN 1. SW_TO_GND<br>2. DASIC_OFF<br>3. DASIC_SW_DET<br>4. GND<br>5. V_MON<br>6. VBULK<br>7. VBULK<br>8. VIN                                                                        |
| <b>STYLE 29:</b><br>PIN 1. BASE, DIE #1<br>2. EMITTER, #1<br>3. BASE, #2<br>4. EMITTER, #2<br>5. COLLECTOR, #2<br>6. COLLECTOR, #2<br>7. COLLECTOR, #1<br>8. COLLECTOR, #1                        | <b>STYLE 30:</b><br>PIN 1. DRAIN 1<br>2. DRAIN 1<br>3. GATE 2<br>4. SOURCE 2<br>5. SOURCE 1/DRAIN 2<br>6. SOURCE 1/DRAIN 2<br>7. SOURCE 1/DRAIN 2<br>8. GATE 1                           |                                                                                                                                                                                    |                                                                                                                                                                                                        |

|                         |                    |                                                                                                                                                                                     |
|-------------------------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>DOCUMENT NUMBER:</b> | <b>98ASB42564B</b> | Electronic versions are uncontrolled except when accessed directly from the Document Repository.<br>Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| <b>DESCRIPTION:</b>     | <b>SOIC-8 NB</b>   | <b>PAGE 2 OF 2</b>                                                                                                                                                                  |

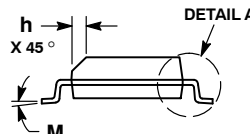
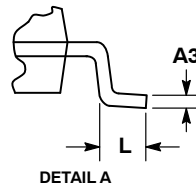
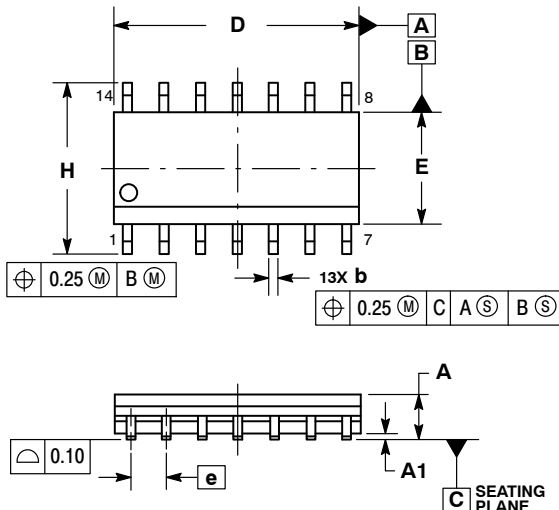
**onsemi** and **onsemi** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.



SCALE 1:1

SOIC-14 NB  
CASE 751A-03  
ISSUE L

DATE 03 FEB 2016

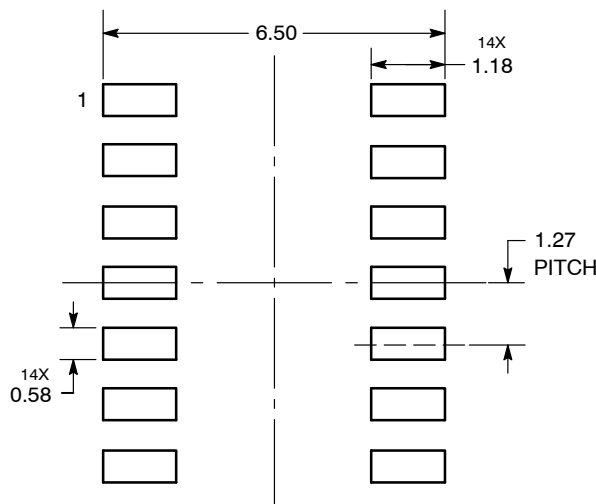


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 1.35        | 1.75 | 0.054     | 0.068 |
| A1  | 0.10        | 0.25 | 0.004     | 0.010 |
| A3  | 0.19        | 0.25 | 0.008     | 0.010 |
| b   | 0.35        | 0.49 | 0.014     | 0.019 |
| D   | 8.55        | 8.75 | 0.337     | 0.344 |
| E   | 3.80        | 4.00 | 0.150     | 0.157 |
| e   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 5.80        | 6.20 | 0.228     | 0.244 |
| h   | 0.25        | 0.50 | 0.010     | 0.019 |
| L   | 0.40        | 1.25 | 0.016     | 0.049 |
| M   | 0°          | 7°   | 0°        | 7°    |

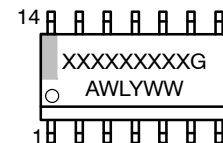
SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC  
MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

|                  |             |                                                                                                                                                                                     |
|------------------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DOCUMENT NUMBER: | 98ASB42565B | Electronic versions are uncontrolled except when accessed directly from the Document Repository.<br>Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION:     | SOIC-14 NB  | PAGE 1 OF 2                                                                                                                                                                         |

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

SOIC-14  
CASE 751A-03  
ISSUE L

DATE 03 FEB 2016

STYLE 1:  
PIN 1. COMMON CATHODE  
2. ANODE/CATHODE  
3. ANODE/CATHODE  
4. NO CONNECTION  
5. ANODE/CATHODE  
6. NO CONNECTION  
7. ANODE/CATHODE  
8. ANODE/CATHODE  
9. ANODE/CATHODE  
10. NO CONNECTION  
11. ANODE/CATHODE  
12. ANODE/CATHODE  
13. NO CONNECTION  
14. COMMON ANODE

STYLE 2:  
CANCELLED

STYLE 3:  
PIN 1. NO CONNECTION  
2. ANODE  
3. ANODE  
4. NO CONNECTION  
5. ANODE  
6. NO CONNECTION  
7. ANODE  
8. ANODE  
9. ANODE  
10. NO CONNECTION  
11. ANODE  
12. ANODE  
13. NO CONNECTION  
14. COMMON CATHODE

STYLE 4:  
PIN 1. NO CONNECTION  
2. CATHODE  
3. CATHODE  
4. NO CONNECTION  
5. CATHODE  
6. NO CONNECTION  
7. CATHODE  
8. CATHODE  
9. CATHODE  
10. NO CONNECTION  
11. CATHODE  
12. CATHODE  
13. NO CONNECTION  
14. COMMON ANODE

STYLE 5:  
PIN 1. COMMON CATHODE  
2. ANODE/CATHODE  
3. ANODE/CATHODE  
4. ANODE/CATHODE  
5. ANODE/CATHODE  
6. NO CONNECTION  
7. COMMON ANODE  
8. COMMON CATHODE  
9. ANODE/CATHODE  
10. ANODE/CATHODE  
11. ANODE/CATHODE  
12. ANODE/CATHODE  
13. NO CONNECTION  
14. COMMON ANODE

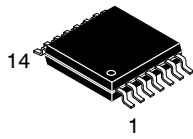
STYLE 6:  
PIN 1. CATHODE  
2. CATHODE  
3. CATHODE  
4. CATHODE  
5. CATHODE  
6. CATHODE  
7. CATHODE  
8. ANODE  
9. ANODE  
10. ANODE  
11. ANODE  
12. ANODE  
13. ANODE  
14. ANODE

STYLE 7:  
PIN 1. ANODE/CATHODE  
2. COMMON ANODE  
3. COMMON CATHODE  
4. ANODE/CATHODE  
5. ANODE/CATHODE  
6. ANODE/CATHODE  
7. ANODE/CATHODE  
8. ANODE/CATHODE  
9. ANODE/CATHODE  
10. ANODE/CATHODE  
11. COMMON CATHODE  
12. COMMON ANODE  
13. ANODE/CATHODE  
14. ANODE/CATHODE

STYLE 8:  
PIN 1. COMMON CATHODE  
2. ANODE/CATHODE  
3. ANODE/CATHODE  
4. NO CONNECTION  
5. ANODE/CATHODE  
6. ANODE/CATHODE  
7. COMMON ANODE  
8. COMMON ANODE  
9. ANODE/CATHODE  
10. ANODE/CATHODE  
11. NO CONNECTION  
12. ANODE/CATHODE  
13. ANODE/CATHODE  
14. COMMON CATHODE

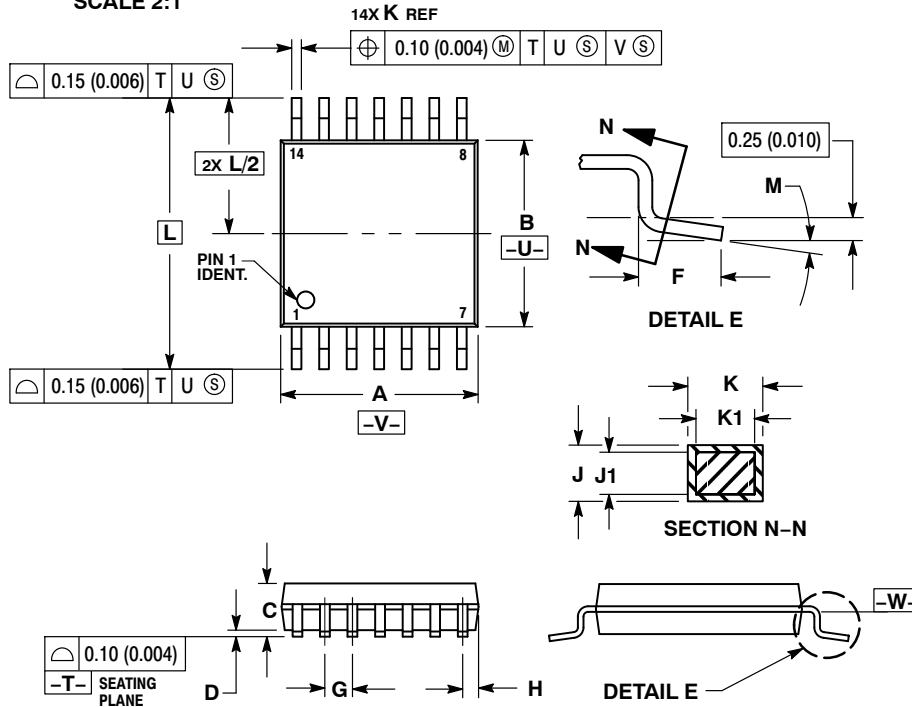
|                  |             |                                                                                                                                                                                     |
|------------------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DOCUMENT NUMBER: | 98ASB42565B | Electronic versions are uncontrolled except when accessed directly from the Document Repository.<br>Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION:     | SOIC-14 NB  | PAGE 2 OF 2                                                                                                                                                                         |

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.


**TSSOP-14 WB**  
**CASE 948G**  
**ISSUE C**

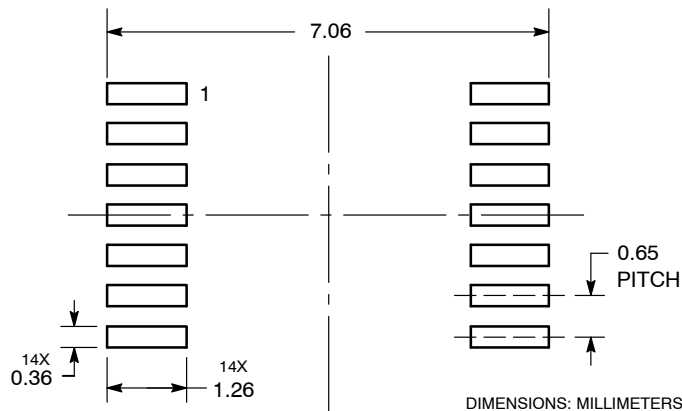
DATE 17 FEB 2016

SCALE 2:1

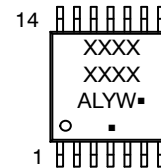

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.50        | 0.60 | 0.020     | 0.024 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

**RECOMMENDED  
SOLDERING FOOTPRINT\***


\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC  
MARKING DIAGRAM\***


A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

**DOCUMENT NUMBER:** 98ASH70246A

Electronic versions are uncontrolled except when accessed directly from the Document Repository.  
Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.

**DESCRIPTION:** TSSOP-14 WB

**PAGE 1 OF 1**

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at  
[www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)