



CYPRESS

RoboClock®
CY7B9950

2.5/3.3V, 200-MHz High-Speed Multi-Phase PLL Clock Buffer

Features

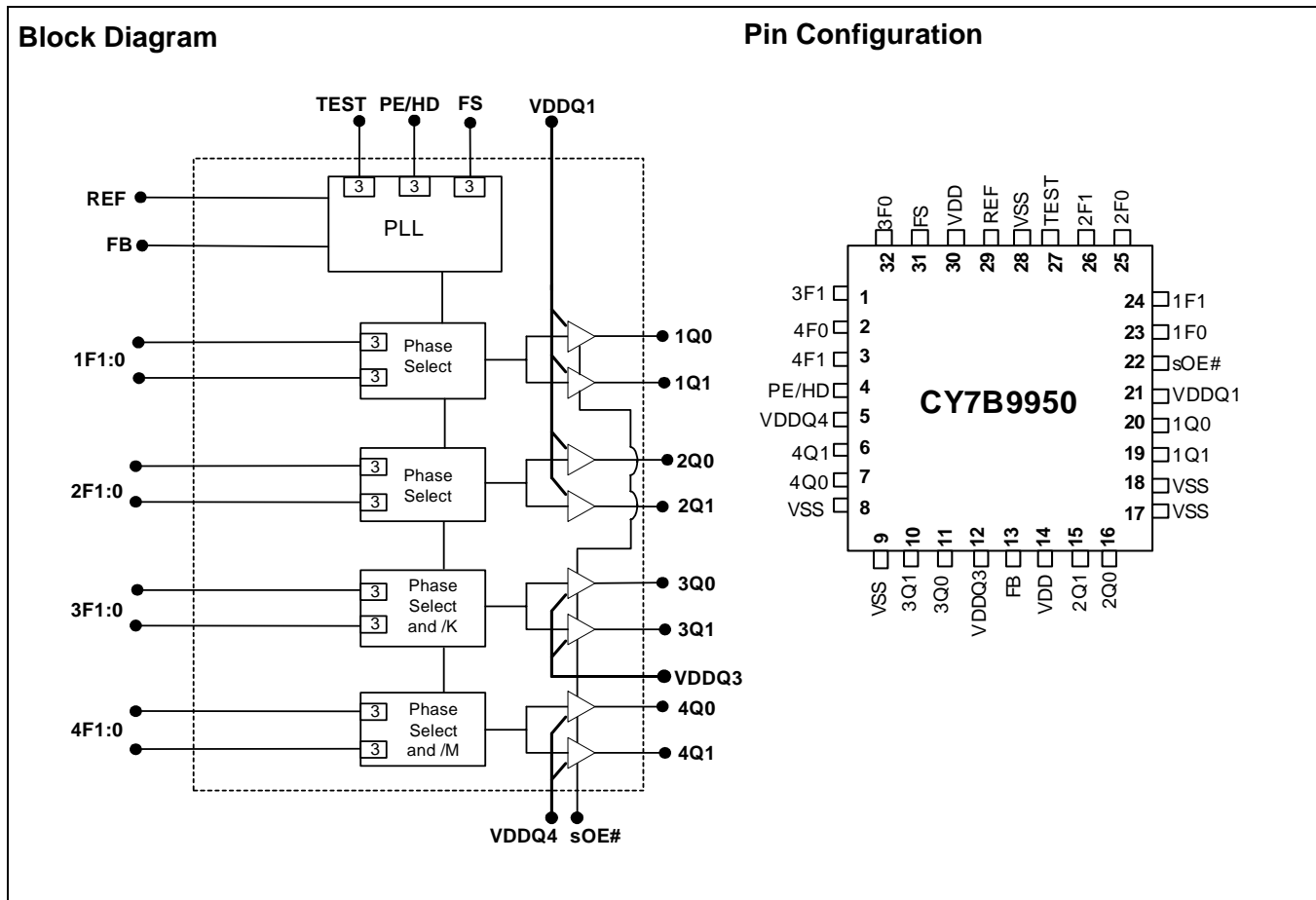
- 2.5V or 3.3V operation
- Split output bank power supplies
- Output frequency range: 6 MHz to 200 MHz
- Output-output skew < 100 ps
- Cycle-cycle jitter < 100 ps
- ± 2% max output duty cycle
- Selectable output drive strength
- Selectable positive or negative edge synchronization
- Eight LVTTTL outputs driving 50Ω terminated lines
- LVC MOS/LVTTL over-voltage-tolerant reference input
- Phase adjustments in 625-/1250-ps steps up to ±7.5 ns
- 2x, 4x multiply and (1/2)x, (1/4)x divide ratios
- Spread-Spectrum-compatible
- Industrial temp. range: -40°C to +85°C
- 32-pin TQFP package

Description

The CY7B9950 RoboClock® is a low-voltage, low-power, eight-output, 200-MHz clock driver. It features output phase programmability which is necessary to optimize the timing of high-performance computer and communication systems.

The user can program the phase of the output banks through nF[0:1] pins. The adjustable phase feature allows the user to skew the outputs to lead or lag the reference clock. Any one of the outputs can be connected to feedback input to achieve different reference frequency multiplication and divide ratios and zero input-output delay.

The device also features split output bank power supplies which enable the user to run two banks (1Qn and 2Qn) at a power supply level different from that of the other two banks (3Qn and 4Qn). Additionally, the three-level PE/HD pin controls the synchronization of the output signals to either the rising or the falling edge of the reference clock and selects the drive strength of the output buffers. The high drive option (PE/HD = MID) increases the output current from ± 12 mA to ± 24 mA (3.3V).



Pin Description

| Pin | Name | I/O ^[1] | Type | Description |
|------------------------------|----------------------------------|--------------------|---------------|--|
| 29 | REF | I | LVTTTL/LVCMOS | Reference Clock Input. |
| 13 | FB | I | LVTTTL | Feedback Input. |
| 27 | TEST | I | Three-level | When MID or HIGH, Disables Phase-locked Loop (PLL) (except for conditions of <i>note 3</i>). REF goes to outputs of Bank 1 and Bank 2. REF goes to outputs of Bank 3 and Bank 4 through output dividers K and M. Set LOW for normal operation. |
| 22 | sOE# | I, PD | Two-level | Synchronous Output Enable. When HIGH, it stops clock outputs (except 2Q0 and 2Q1) in a LOW state (for PE = H or M) – 2Q0 and 2Q1 may be used as the feedback signal to maintain phase lock. When TEST is held at MID level and sOE# is HIGH, the nF[1:0] pins act as output disable controls for individual banks when nF[1:0] = LL. Set sOE# LOW for normal operation. |
| 4 | PE/HD | I, PU | Three-level | Selects Positive or Negative Edge Control and High or Low output drive strength. When LOW/HIGH the outputs are synchronized with the negative/positive edge of the reference clock, respectively. When at MID level, the output drive strength is increased and the outputs synchronize with the positive edge of the reference clock (see <i>Table 6</i>). |
| 24, 23, 26, 25, 1, 32, 3, 2 | nF[1:0] | I | Three-level | Select frequency and phase of the outputs (see <i>Tables 1, 2, 3, 4, and 5</i>). |
| 31 | FS | I | Three-level | Selects VCO operating frequency range (see <i>Table 4</i>). |
| 19, 20, 15, 16, 10, 11, 6, 7 | nQ[1:0] | O | LVTTTL | Four banks of two outputs (see <i>Tables 1, 2, and 3</i>). |
| 21 | V _{DDQ1} ^[2] | PWR | Power | Power supply for Bank 1 and Bank 2 output buffers (see <i>Table 7</i> for supply level constraints). |
| 12 | V _{DDQ3} ^[2] | PWR | Power | Power supply for Bank 3 output buffers (see <i>Table 7</i> for supply level constraints). |
| 5 | V _{DDQ4} ^[2] | PWR | Power | Power supply for Bank 4 output buffers (see <i>Table 7</i> for supply level constraints). |
| 14,30 | V _{DD} ^[2] | PWR | Power | Power supply for internal circuitry (see <i>Table 7</i> for supply level constraints). |
| 8,9,17,18, 28 | V _{SS} | PWR | Power | Ground. |

Device Configuration

The outputs of the CY7B9950 can be configured to run at frequencies ranging from 6 to 200 MHz. Banks 3 and 4 output dividers are controlled by 3F[1:0] and 4F[1:0] as indicated in *Table 1* and *Table 2*, respectively.

Table 1. Output Divider Settings — Bank 3

| 3F[1:0] | K — Bank3 Output Divider |
|----------------------|--------------------------|
| LL | 2 |
| HH | 4 |
| Other ^[4] | 1 |

Table 2. Output Divider Settings — Bank 4

| 4F[1:0] | M — Bank4 Output Divider |
|----------------------|--------------------------|
| LL | 2 |
| Other ^[4] | 1 |

Notes:

- “PD” indicates an internal pull-down and “PU” indicates an internal pull-up. “3” indicates a three-level input buffer
- A bypass capacitor (0.1µF) should be placed as close as possible to each positive power pin (< 0.2”). If these bypass capacitors are not close to the pins their high-frequency filtering characteristic will be cancelled by the lead inductance of the traces.
- When TEST = MID and sOE# = HIGH, PLL remains active with nF[1:0] = LL functioning as an output disable control for individual output banks. Skew selections remain in effect unless nF[1:0] = LL.
- These states are used to program the phase of the respective banks (see *Table 5*).

The three-level FS control pin setting determines the nominal operating frequency range of the divide-by-one outputs of the device. The CY7B9950 PLL operating frequency range that corresponds to each FS level is given in *Table 3*.

Table 3. Frequency Range Select

| FS | PLL Frequency Range |
|----|---------------------|
| L | 24 to 50 MHz |
| M | 48 to 100 MHz |
| H | 96 to 200 MHz |

Selectable output skew is in discrete increments of time unit (t_U). The value of t_U is determined by the FS setting and the maximum nominal frequency. The equation to be used to determine the t_U value is as follows: $t_U = 1 / (f_{NOM} \times MF)$

where MF is a multiplication factor, which is determined by the FS setting as indicated in *Table 4*.

Table 4. MF Calculation

| FS | MF | f _{NOM} at which t _U is 1.0 ns(MHz) |
|----|----|---|
| L | 32 | 31.25 |
| M | 16 | 62.5 |
| H | 8 | 125 |

Table 5. Output Skew Settings

| nF[1:0] | Skew (1Q[0:1],2Q[0:1]) | Skew (3Q[0:1]) | Skew (4Q[0:1]) |
|-------------------|------------------------|------------------|-------------------------|
| LL ^[5] | -4t _U | Divide By 2 | Divide By 2 |
| LM | -3t _U | -6t _U | v6t _U |
| LH | -2t _U | -4t _U | -4t _U |
| ML | -1t _U | -2t _U | v2t _U |
| MM | Zero Skew | Zero Skew | Zero Skew |
| MH | +1t _U | +2t _U | +2t _U |
| HL | +2t _U | +4t _U | +4t _U |
| HM | +3t _U | +6t _U | +6t _U |
| HH | +4t _U | Divide By 4 | Inverted ^[6] |

In addition to determining whether the outputs synchronize to the rising or the falling edge of the reference signal, the 3-level PE/HD pin controls the output buffer drive strength as indicated in *Table 6*.

The CY7B9950 features split power supply buses for Banks 1 and 2, Bank 3 and Bank 4, which enables the user to obtain both 3.3V and 2.5V output signals from one device. The core power supply (VDD) must be set a level that is equal or higher than on any one of the output power supplies.

Table 6. PE/HD Settings

| PE/HD | Synchronization | Output Drive Strength ^[7] |
|-------|-----------------|--------------------------------------|
| L | Negative | Low Drive |
| M | Positive | High Drive |
| H | Positive | Low Drive |

Notes:

5. LL disables outputs if TEST = MID and sOE# = HIGH.
6. When 4Q[0:1] are set to run inverted (HH mode), sOE# disables these outputs HIGH when PE/HD = HIGH or MID, sOE# disables them LOW when PE/HD = LOW.
7. Please refer to "DC Parameters" section for I_{OH}/I_{OL} specifications.
8. V_{DDQ1/3/4} must not be set at a level higher than that of V_{DD}. They can be set at different levels from each other, e.g., V_{DD} = 3.3V, V_{DDQ1} = 3.3V, V_{DDQ3} = 2.5V and V_{DDQ4} = 2.5V.

Table 7. Power Supply Constraints

| V _{DD} | V _{DDQ1} ^[8] | V _{DDQ3} ^[8] | V _{DDQ4} ^[8] |
|-----------------|----------------------------------|----------------------------------|----------------------------------|
| 3.3V | 3.3V or 2.5V | 3.3V or 2.5V | 3.3V or 2.5V |
| 2.5V | 2.5V | 2.5V | 2.5V |

Governing Agencies

The following agencies provide specifications that apply to the CY7B9950. The agency name and relevant specification is listed below.

Table 8.

| Agency Name | Specification |
|-------------|--|
| JEDEC | JESD 51 (Theta JA) JESD 65 (Skew, Jitter) |
| IEEE | 1596.3 (Jitter Specs) |
| UL-194_V0 | 94 (Moisture Grading) |
| MIL | 883E Method 1012.1 (Therma Theta JC) |

Absolute Maximum Conditions

| Parameter | Description | Condition | Min. | Max. | Unit |
|----------------------|-----------------------------------|-----------------------------|-----------------------|-----------------------|------|
| V _{DD} | Operating Voltage | Functional @ 2.5V ± 5% | 2.375 | 2.625 | V |
| V _{DD} | Operating Voltage | Functional @ 3.3V ± 10% | 2.97 | 3.63 | V |
| V _{IN(MIN)} | Input Voltage | Relative to V _{SS} | V _{SS} - 0.3 | - | V |
| V _{IN(MAX)} | Input Voltage | Relative to V _{DD} | - | V _{DD} + 0.3 | V |
| T _S | Temperature, Storage | Non-functional | -65 | +150 | °C |
| T _A | Temperature, Operating Ambient | Functional | -40 | +85 | °C |
| T _J | Temperature, Junction | Functional | - | 155 | °C |
| ∅ _{JC} | Dissipation, Junction to Case | Mil-Spec 883E Method 1012.1 | - | 42 | °C/W |
| ∅ _{JA} | Dissipation, Junction to Ambient | JEDEC (JESD 51) | - | 105 | °C/W |
| ESD _{HBM} | ESD Protection (Human Body Model) | MIL-STD-883, Method 3015 | 2000 | - | V |
| UL-94 | Flammability Rating | @ 1/8 in. | V-0 | | |
| MSL | Moisture Sensitivity Level | | 1 | | |
| F _{IT} | Failure in Time | Manufacturing Testing | 10 | | ppm |

DC Electrical Specifications @ 2.5V

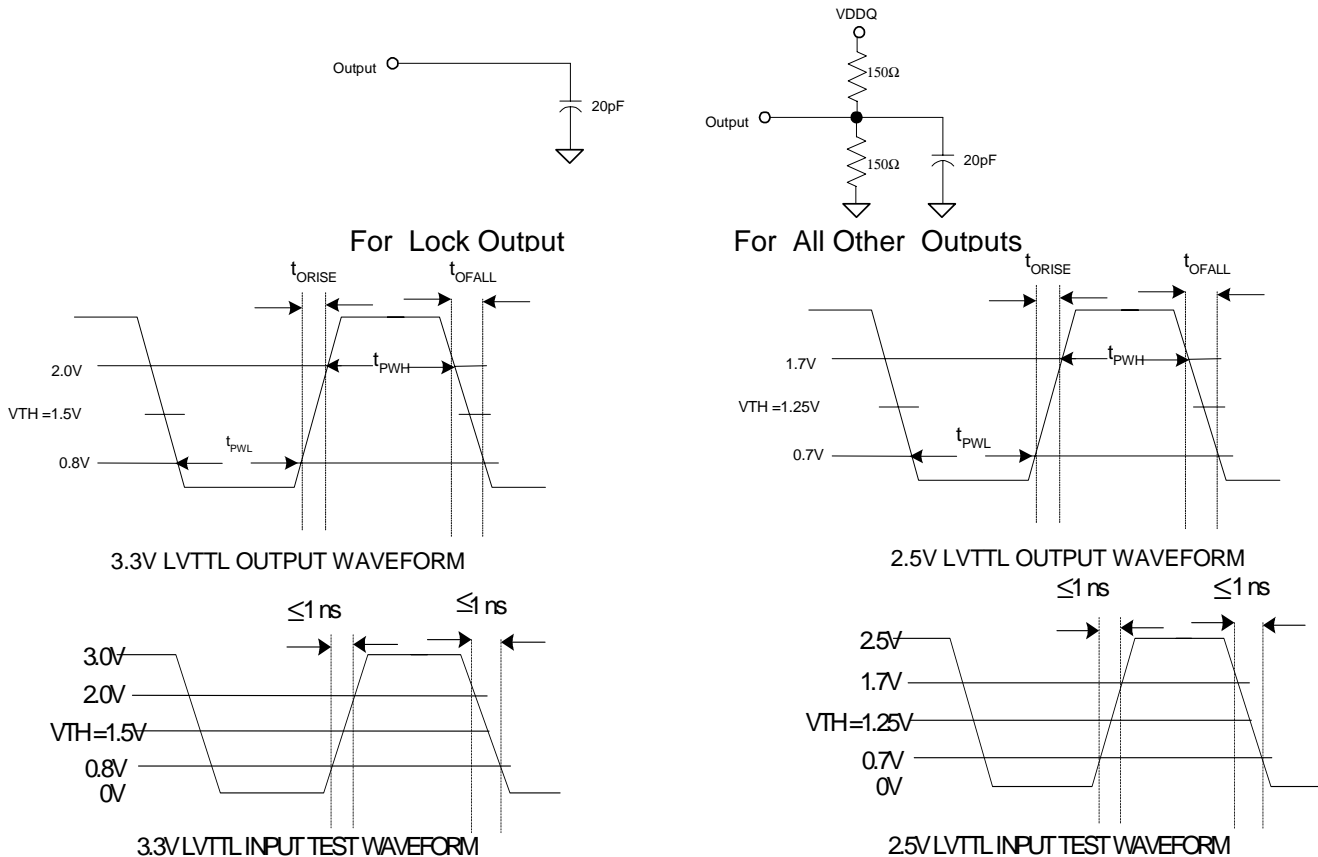
| Parameter | Description | Conditions | Min. | Max. | Unit | |
|---------------------------------|--------------------------|---|---|--------------------------|------|----|
| V _{DD} | 2.5 Operating Voltage | 2.5V ± 5% | 2.375 | 2.625 | V | |
| V _{IL} | Input LOW Voltage | REF, FB and sOE# Inputs | - | 0.7 | V | |
| V _{IH} | Input HIGH Voltage | | 1.7 | - | V | |
| V _{IHH} ^[9] | Input HIGH Voltage | 3-Level Inputs (TEST, FS, nF[1:0], PE/HD) (These pins are normally wired to V _{DD} , GND or unconnected.) | V _{DD} - 0.4 | - | V | |
| V _{IMM} ^[9] | Input MID Voltage | | V _{DD} /2 - 0.2 | V _{DD} /2 + 0.2 | V | |
| V _{ILL} ^[9] | Input LOW Voltage | | - | 0.4 | V | |
| I _{IL} | Input Leakage Current | V _{IN} = V _{DD} /G _{ND} , V _{DD} = max. (REF and FB inputs) | -5 | 5 | μA | |
| I ₃ | 3-Level Input DC Current | HIGH, V _{IN} = V _{DD} | 3-Level Inputs (TEST, FS, nF[1:0], DS[1:0], PD#/DIV, PE/HD) | - | 200 | μA |
| | | MID, V _{IN} = V _{DD} /2 | | -50 | 50 | μA |
| | | LOW, V _{IN} = V _{SS} | | -200 | - | μA |
| I _{PU} | Input Pull-up Current | V _{IN} = V _{SS} , V _{DD} = max. | -25 | - | μA | |
| I _{PD} | Input Pull-down Current | V _{IN} = V _{DD} , V _{DD} = max., (sOE#) | - | 100 | μA | |
| V _{OL} | Output LOW Voltage | I _{OL} = 12 mA (PE/HD = L/H), (nQ[0:1]) | - | 0.4 | V | |
| | | I _{OL} = 20 mA (PE/HD = MID), (nQ[0:1]) | - | 0.4 | V | |
| V _{OH} | Output HIGH Voltage | I _{OH} = -12 mA (PE/HD = L/H), (nQ[0:1]) | 2.0 | - | V | |
| | | I _{OH} = -20 mA (PE/HD = MID), (nQ[0:1]) | 2.0 | - | V | |
| I _{DDQ} | Quiescent Supply Current | V _{DD} = max., TEST = MID, REF = LOW, sOE# = LOW, outputs not loaded | - | 2 | mA | |
| I _{DD} | Dynamic Supply Current | @ 100 MHz | 150 | | mA | |
| C _{IN} | Input Pin Capacitance | | 4 | | pF | |

Note:

9. These inputs are normally wired to V_{DD}, GND or unconnected. Internal termination resistors bias unconnected inputs to V_{DD}/2.

DC Specifications @ 3.3V

| Parameter | Description | Condition | Min. | Max. | Unit | |
|-----------------|--------------------------|--|--|------------------|---------------|---------------|
| V_{DD} | 3.3 Operating Voltage | $3.3V \pm 10\%$ | 2.97 | 3.63 | V | |
| V_{IL} | Input LOW Voltage | REF, FB and sOE# Inputs | – | 0.8 | V | |
| V_{IH} | Input HIGH Voltage | | 2.0 | – | V | |
| $V_{IHH}^{[9]}$ | Input HIGH Voltage | | 3-Level Inputs | $V_{DD} - 0.6$ | – | V |
| $V_{IMM}^{[9]}$ | Input MID Voltage | (TEST, FS, nF[1:0], PE/HD) (These pins are normally wired to V_{DD} , GND or unconnected.) | $V_{DD}/2 - 0.3$ | $V_{DD}/2 + 0.3$ | V | |
| $V_{ILL}^{[9]}$ | Input LOW Voltage | | – | 0.6 | V | |
| I_{IL} | Input Leakage Current | $V_{IN} = V_{DD}/G_{ND}, V_{DD} = \text{max.}$ (REF and FB inputs) | –5 | 5 | μA | |
| I_3 | 3-Level Input DC Current | HIGH, $V_{IN} = V_{DD}$ | 3-Level Inputs (TEST, FS, nF[1:0], DS[1:0], PD#/DIV, PE/HD) | – | 200 | μA |
| | | MID, $V_{IN} = V_{DD}/2$ | | –50 | 50 | μA |
| | | LOW, $V_{IN} = V_{SS}$ | | –200 | – | μA |
| I_{PU} | Input Pull-up Current | $V_{IN} = V_{SS}, V_{DD} = \text{max.}$ | –100 | – | μA | |
| I_{PD} | Input Pull-down Current | $V_{IN} = V_{DD}, V_{DD} = \text{max.}$, (sOE#) | – | 100 | μA | |
| V_{OL} | Output LOW Voltage | $I_{OL} = 12 \text{ mA}$ (PE/HD = L/H), (nQ[0:1]) | – | 0.4 | V | |
| | | $I_{OL} = 24 \text{ mA}$ (PE/HD = MID), (nQ[0:1]) | – | 0.4 | V | |
| V_{OH} | Output HIGH Voltage | $I_{OH} = -12 \text{ mA}$ (PE/HD = L/H), (nQ[0:1]) | 2.4 | – | V | |
| | | $I_{OH} = -24 \text{ mA}$ (PE/HD = MID), (nQ[0:1]) | 2.4 | – | V | |
| I_{DDQ} | Quiescent Supply Current | $V_{DD} = \text{max.}$, TEST = MID, REF = LOW, sOE# = LOW, outputs not loaded | – | 2 | mA | |
| I_{DD} | Dynamic Supply Current | @ 100 MHz | 230 | | mA | |
| C_{IN} | Input Pin Capacitance | | 4 | | pF | |

AC Test Loads and Waveforms


AC Input Specifications

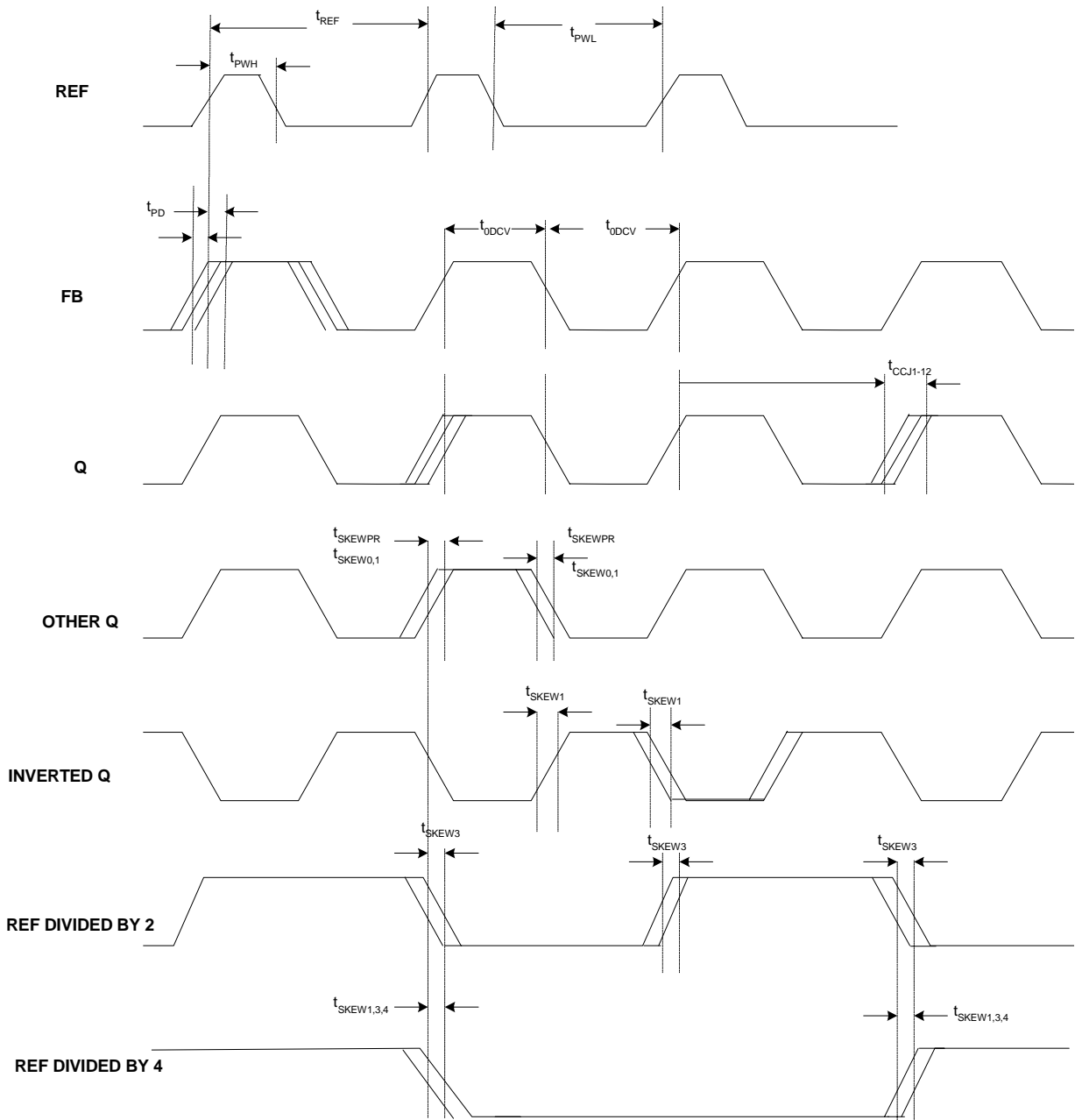
| Parameter | Description | Condition | Min. | Max. | Unit |
|-------------|---------------------------|-------------|------|------|------|
| T_{R,T_F} | Input Rise/Fall Time | 0.8V – 2.0V | – | 10 | ns/V |
| T_{PWC} | Input Clock Pulse | HIGH or LOW | 2 | – | ns |
| T_{DCIN} | Input Duty Cycle | | 10 | 90 | % |
| F_{REF} | Reference Input Frequency | FS = LOW | 6 | 50 | MHz |
| | | FS = MID | 12 | 100 | |
| | | FS = HIGH | 24 | 200 | |

Switching Characteristics

| Parameter | Description | Condition | Min. | Max. | Unit |
|--------------|--|---|------|------|------|
| F_{OR} | Output Frequency Range | | 6 | 200 | MHz |
| VCO_{LR} | VCO Lock Range | | 200 | 400 | MHz |
| VCO_{LBW} | VCO Loop Bandwidth | | 0.25 | 3.5 | MHz |
| t_{SKEWPR} | Matched-Pair Skew ^[10] | Skew between the earliest and the latest output transitions within the same bank. | – | 100 | ps |
| t_{SKEW0} | Output-Output Skew ^[10] | Skew between the earliest and the latest output transitions among all outputs at $0t_U$. | – | 200 | ps |
| t_{SKEW1} | | Skew between the earliest and the latest output transitions among all outputs for which the same phase delay has been selected. | – | 200 | ps |
| t_{SKEW2} | | Skew between the nominal output rising edge to the inverted output falling edge | – | 500 | ps |
| t_{SKEW3} | Output-Output Skew ^[10] | Skew between non-inverted outputs running at different frequencies | – | 500 | ps |
| t_{SKEW4} | | Skew between nominal to inverted outputs running at different frequencies | – | 500 | ps |
| t_{SKEW5} | | Skew between nominal outputs at different power supply levels | – | 650 | ps |
| t_{PART} | Part-Part Skew | Skew between the outputs of any two devices under identical settings and conditions ($V_{DDQ}, V_{DD}, temp, air\ flow, frequency, etc.$) | – | 750 | ps |
| t_{PD0} | Ref-FB Propagation Delay ^[11] | | –250 | +250 | ps |
| t_{ODCV} | Output Duty Cycle | $F_{out} < 100\text{ MHz}$, measured at $V_{DD}/2$ | 48 | 52 | % |
| | | $F_{out} > 100\text{ MHz}$, measured at $V_{DD}/2$ | 45 | 55 | |
| t_{PWH} | Output High Time Deviation from 50% | Measured at 2.0V for $V_{DD} = 3.3V$ and at 1.7V for $V_{DD} = 2.5V$. | – | 1.5 | ns |
| t_{PWL} | Output Low Time Deviation from 50% | Measured at 0.8V for $V_{DD} = 3.3V$ and at 0.7V for $V_{DD} = 2.5V$. | – | 2.0 | ns |
| t_R/t_F | Output Rise/Fall Time | Measured at 0.8V – 2.0V for $V_{DD} = 3.3V$ and 0.7V–1.7V for $V_{DD} = 2.5V$ | 0.15 | 1.5 | ns |
| t_{LOCK} | PLL lock time ^[12,13] | | – | 0.5 | ms |
| t_{CCJ} | Cycle-Cycle Jitter | Divide by 1 output frequency, FS = L, FB = divide by 1,2,4 | – | 100 | ps |
| | | Divide by 1 output frequency, FS = M/H, FB = divide by 1,2,4 | – | 150 | ps |

Notes:

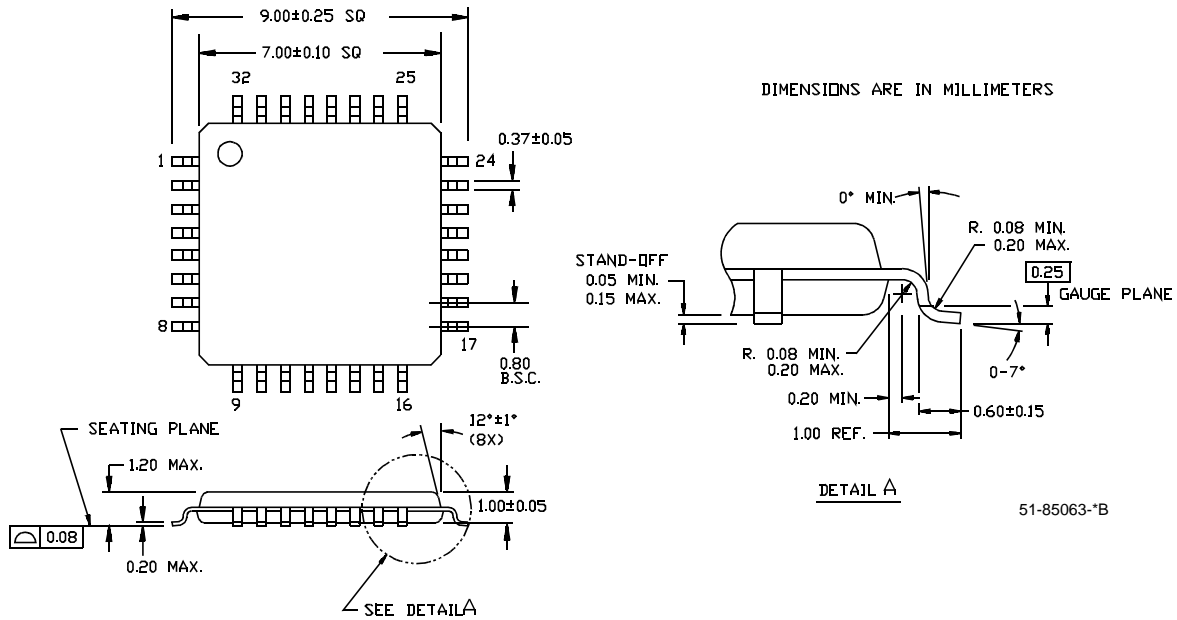
- Test load = 20 pF, terminated to $V_{CC}/2$. All outputs are equally loaded.
- t_{PD} is measured at 1.5V for $V_{DD} = 3.3V$ and at 1.25V for $V_{DD} = 2.5V$ with REF rise/fall times of 0.5 ns between 0.8V – 2.0V.
- t_{LOCK} is the time that is required before outputs synchronize to REF. This specification is valid with stable power supplies which are within normal operating limits.
- Lock detector circuit may be unreliable for input frequencies lower than 4 MHz, or for input signals which contain significant jitter.

AC Timing Definitions

Ordering Information

| Part Number | Package Type | Product Flow |
|-------------|-------------------------|--------------------------|
| CY7B9950AC | 32 TQFP | Commercial, 0° to 70°C |
| CY7B9950ACT | 32 TQFP – Tape and Reel | Commercial, 0° to 70°C |
| CY7B9950AI | 32 TQFP | Industrial, -40° to 85°C |
| CY7B9950AIT | 32 TQFP – Tape and Reel | Industrial, -40° to 85°C |

Package Drawing and Dimension

32-lead Thin Plastic Quad Flatpack 7 x 7 x 1.0 mm A32



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Document History Page

| Document Title: RoboClock® CY7B9950 2.5/3.3V, 200-MHz High-Speed Multi-Phase PLL Clock Buffer | | | | |
|---|---------|------------|-----------------|---|
| Document Number: 38-07338 | | | | |
| Rev. | ECN No. | Issue Date | Orig. of Change | Description of Change |
| ** | 121663 | 11/25/02 | RGL | New Data Sheet |
| *A | 122548 | 12/12/02 | RGL | Removed the PD#/DIV and DS[1:0] pins in V_{IHH} , V_{IMM} and V_{ILL} for both 2.5V and 3.3V DC Electrical Specs tables |
| *B | 124646 | 03/05/03 | RGL | Corrected the description of Pin 27(TEST) in the Pin Description table Corrected the description of Pin 12 (V_{DDQ}) in the Pin Description table Corrected the Min and Max values of V_{DD} from 2.25/2.75 to 2.375/2.625 Volts in the Absolute Maximum Conditions table |