Digital video encoder (DENC2-SQ)

SAA7187

FEATURES

- Monolithic CMOS 5V device
- Digital PAL/NTSC encoder
- System Pixel Frequency selectable for 12.27 MHz (60 Hz fields) or 14.75 MHz (50 Hz fields)
- 24-bit wide YUV Input port or
- 16-bit wide YUV Input port or
- Input data format Cb,Y,Cr,Y,... (CCIR 656 like)
- IIC Bus control port
- MPU parallel control port
- Encoder can be master or slave
- Programmable horizontal and vertical input synchronization phase
- Programmable horizontal sync output phase
- OSD overlay with LUTs (8*3 bytes)
- 'Line 21' Closed Caption encoder
- Cross colour reduction
- DACs running at two times oversampling with 10 bits resolution
- Controlled rise-/fall times of output syncs and blanking
- Down mode of DACs
- CVBS and S-Video output simultaneously.
- PLCC68 package

Quick Reference Data

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage range	4.5	5.0	5.5	V
V_{DDA}	analog supply voltage range	4.75	5.0	5.25	V
I_{DDD}	supply current digital	-	175	210	mA
I_{DDA}	supply current analog	-	50	55	mA
V_i	input signal levels	TTL - compatible			V
V_o	analog output signals, Y, C and CVBS without load (peak to peak value)	-	2	-	V
R_L	load resistance	80	-	-	Ω
ILE	LF integral linearity error	-	-	± 2	LSB
DLE	LF differential linearity error	-	-	± 1	LSB
T_{amb}	operating ambient temperature range	0	-	70	°C

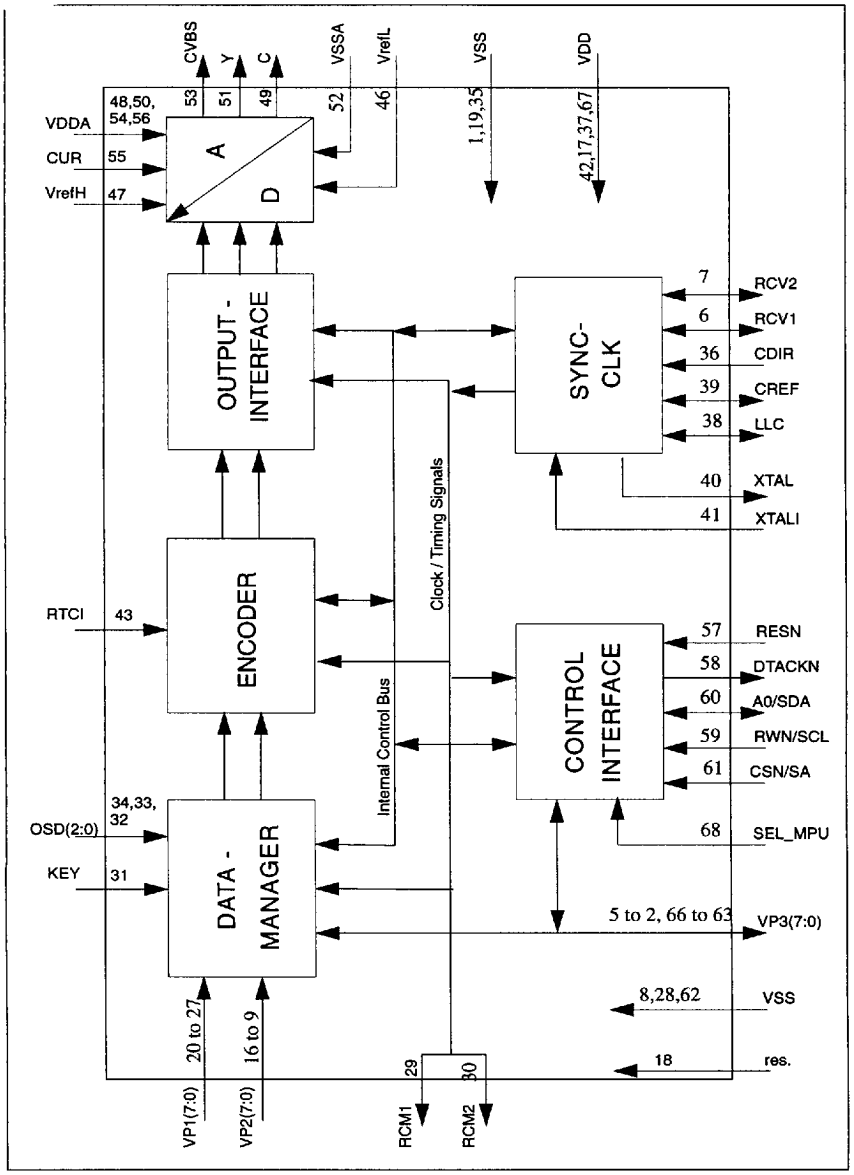
General Description

The Digital Video Encoder 2 (DENC2-SQ) encodes digital YUV video data to an NTSC or PAL CVBS or S-Video signal.

The circuit accepts differently formatted YUV data with 640 or 768 active pixels per line. It includes a sync/clock generator as well as on chip D/A converters.

The circuit is compatible to the DIG. TV2 chip family (Square Pixel).

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7187	68	PLCC	plastic	SOT188



PINNING

SYMBOL	PIN	DESCRIPTION
VSS	1	Digital negative supply voltage (Ground)
VP3(4)	2	Upper 4 bits of the VP3 Port. If Pin 68 (SEL_MPU) is high, this is the data bus of the parallel MPU interface. If it is low, there can be multiplexed UV lines (422) or the U-signal (444) of the Video input
VP3(5)	3	
VP3(6)	4	
VP3(7)	5	
RCV1	6	Raster Control 1 for Video port. Depending on the synchronization mode, this pin receives/provides a VS/FS/FSEQ signal.
RCV2	7	Raster Control 2 for Video port. Depending on the synchronization mode, this pin receives/provides a HS/HREF/CBL signal
VSS	8	Digital negative supply voltage (Ground)
VP2(0)	9	Video Port VP2. In 444 input mode, this is input for the V-signal
VP2(1)	10	
VP2(2)	11	
VP2(3)	12	
VP2(4)	13	
VP2(5)	14	
VP2(6)	15	
VP2(7)	16	
VDD	17	Digital positive supply voltage.
res.	18	reserved, do not connect.
VSS	19	Digital negative supply voltage (Ground)
VP1(7)	20	Video Port VP1. This is an input for CCIR-656 compatible, multiplexed video data, or during other input modes, this is the Y-signal.
VP1(6)	21	
VP1(5)	22	
VP1(4)	23	
VP1(3)	24	
VP1(2)	25	
VP1(1)	26	
VP1(0)	27	
VSS	28	Digital negative supply voltage (Ground)
RCM1	29	Raster Control Master 1. This pin provides a VS/FS/FSEQ signal
RCM2	30	Raster Control Master 2. This pin provides a programmable HS pulse
KEY	31	Key signal for OSD. It is high-active.
OSD(0)	32	On Screen Display data. This is the index for the internal OSD lookup table.
OSD(1)	33	
OSD(2)	34	
VSS	35	Digital negative supply voltage (Ground)
CDIR	36	Clock direction. If the CDIR input is high, the circuit receives a clock signal, otherwise LLC and CREF are generated by the internal crystal oscillator.
VDD	37	Digital positive supply voltage.

PINNING

SYMBOL	PIN	DESCRIPTION
LLC	38	Line Locked clock. This is the 24.54 MHz / 29.5 MHz master clock for the encoder. The direction is set by the CDIR pin.
CREF	39	Clock Reference signal. This is the clock qualifier for DIG-TV2 compatible signals.
XTAL	40	Crystal oscillator output (to crystal).
XTALI	41	Crystal oscillator input (from crystal). If the oscillator is not used, this pin should be connected to ground.
VDD	42	Digital positive supply voltage.
RTCI	43	Real Time Control Input. If the clock is provided by a SAA7191B, RTCI should be connected to the RTCO pin of the decoder to improve the signal quality.
AP	44	Test pin. Connect to digital ground for normal operation.
SP	45	Test pin. Connect to digital ground for normal operation.
VREFL	46	Lower reference voltage for the D/A converters.
VREFH	47	Upper reference voltage for the D/A converters.
VDDA	48	Analog positive supply voltage for the D/A converters and output amplifiers.
C	49	Analog output of the chrominace signal.
VDDA	50	Analog positive supply voltage for the D/A converters and output amplifiers.
Y	51	Analog output of the luminance signal.
VSSA	52	Analog negative supply voltage for the D/A converters and output amplifiers (Ground).
CVBS	53	Analog output of the CVBS signal.
VDDA	54	Analog positive supply voltage for the D/A converters and output amplifiers.
CUR	55	Current input for the output amplifiers, connect 15 kOhm to VDDA
VDDA	56	Analog positive supply voltage for the D/A converters and output amplifiers.
RESN	57	Reset input, low active. After reset is applied, all outputs are in tristate/input mode. The IIC receiver waits for the start condition.
DTACKN	58	Data acknowledge output of the parallel MPU interface; low-active, otherwise high-impedance.
RWN/SCL	59	If pin 68 (SEL_MPU) is high, this is the read/write signal of the parallel MPU interface, otherwise it is the IIC serial clock line.
A0/SDA	60	If pin 68 (SEL_MPU) is high, this is the address signal of the parallel MPU interface, otherwise it is the IIC serial data line.
CSN/SA	61	If pin 68 (SEL_MPU) is high, this is the chip select signal of the parallel MPU interface, otherwise it is the IIC slave address select pin: Low : Slave address = 88h; High : Slave address = 8Ch
VSS	62	Digital negative supply voltage (Ground)
VP3(0)	63	Lower 4 bits of the VP3 Port. If Pin 68 (SEL_MPU) is high, this is the data bus of the parallel MPU interface. If it is low, there can be multiplexed UV lines (422) or the U-signal (444) of the Video input
VP3(1)	64	
VP3(2)	65	
VP3(3)	66	
VDD	67	Digital positive supply voltage.
SEL_MPU	68	Select MPU interface. If it is high, the parallel MPU interface is active, otherwise the IIC bus interface will be used.

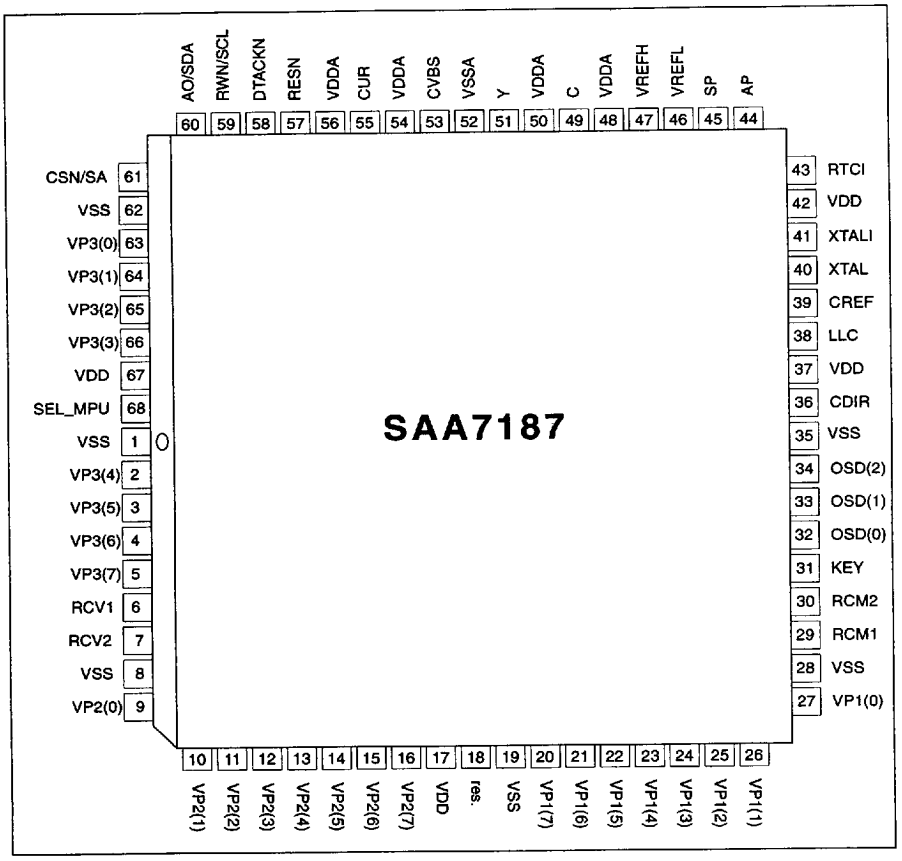


Fig. 2: Pinning Diagram

Functional Description

The digital Video Encoder (DENC2-SQ) encodes digital luminance and chrominance into analog CVBS- and simultaneously S - Video (Y/C) signals. NTSC-M and PAL B/G standards as well as sub-standards are supported.

The basic encoder function consists of subcarrier generation and colour modulation as well as insertion of synchronization signals. Luminance and chrominance signals are filtered according to the standard requirements RS-170-A and CCIR-624.

For ease of analog post filtering the signals are two times oversampled w.r.t. pixel clock before digital-to-analog conversion.

For total filter transfer characteristics see figs 3, 4, 5 and 6 for 60 Hz field rate, and figs 7, 8, 9 and 10 for 50 Hz field rate. The DACs are realized with full 10 bit resolution. The encoder provides three 8 bit wide data ports, that serve different applications.

The VP1 port accepts 8 lines multiplexed Cb-Y-Cr data (CCIR-656 mode), or Y-data only (444 mode).

The VP2 port accepts Cr-data in 444 input mode.

The VP3 port accepts Cb-data (444 input mode) or multiplexed Cb/Cr-data (422 input mode. If not used for video input data, it also can handle the data of an 8 bit wide microprocessor interface, alternatively.

Minimum suppression of output chroma alias components around 1 MHz due to high frequency 444 input data is better than 12 dB.

The 8 bit multiplexed Cb-Y-Cr formats are CCIR-656 (D1 format) compatible, but the SAV, EAV e.t.c. codes are not decoded.

A crystal-stable master clock (LLC) of 24.54 or 29.5 MHz, which is twice the linelocked pixel clock, needs to be sup-

plied externally. Optionally, a crystal oscillator input/output pair of pins and an on-chip clock driver is provided. Additionally, a DMSD2 compatible clock interface, using CREF (input or output) and RTC (see data sheet SAA 7191B) is available.

The DENC2-SQ synthesizes all necessary internal signals, colour subcarrier frequency, as well as synchronization signals, from that clock. DENC2-SQ can be timing master or slave.

The IC contains Closed Caption and Extended Data Services Encoding (Line 21); it also supports OSD via KEY and three bit overlay techniques by a 24*8 LUT.

The IC can be programmed via I2C or 8-bit MPU interface, but only one interface configuration can be active at a time; if 422 or 444 input format is being used, only the I2C interface can be selected.

A lot of possibilities is provided for setting of different video parameters like Black- and Blanking level control, colour subcarrier frequency, variable burst amplitude etc.

During Reset (RESN=low) and after Reset released, all digital I/O stages are set to input mode. A Reset forces the control interfaces to abort any running bus transfer and to set register 3Ah to contents 00h, register 61h to contents 15h, and register 6Ch to contents 00h. All other control registers are not influenced by a Reset.

Data Manager

In the Data Manager, the de-multiplexing scheme is chosen acc. to the input format.

Depending on hardware conditions (signals on pins KEY and OSD(2-0), and software programming either data from the VP ports or from the OSD port are selected to be encoded to CVBS and Y/C signals.

Optionally, the OSD colour look-up tables located in this block, can be read out in a pre-defined sequence (8 steps per active video line), achieving e.g. a colour bar test pattern generator without need for an external data source. The colour bar function is under software control, only.

Encoder

Video Path:

The encoder generates out of Y,U,V base band signals output signals luminance and colour subcarrier, suitable for use as CVBS or separate Y and C signals.

Luminance is modified in gain as well as in offset (latter programmable in a certain range to enable different black level set-ups).After having been inserted a fixed sync level, acc. to standard composite sync schemes, a variable blanking level, programmable also in a certain range, is inserted.

Transients of both sync pulses and start/stop of blanking are reduced compared to overall luminance bandwidth.

In order to enable easy analog post filtering, luminance is interpolated from square pixel data rate to twice that rate (24.54 or 29.5 MHz, respectively), providing luminance in 10 bit resolution. For transfer characteristic of the luminance interpolation filter see figs. 5 and 6 for 60 Hz field rate and figs. 9 and 10 for 50 Hz field rate.

Chrominance is modified in gain (programmable separately for U and V), standard dependent burst is inserted, before base band colour signals are interpolated properly to 24.54/29.5 MHz data rate. One of the interpolation stages can be by-passed, thus providing a higher colour bandwidth, which can be made use of for Y/C output. For transfer characteristics of the chrominance interpolation filter see figs. 3 and 4 for 60 Hz field rate and figs.7 and 8 for 50 Hz field rate.

The amplitude of inserted burst is programmable in a certain range, suitable for standard signals as well as for special effects. Behind the succeeding quadrature modulator, colour in 10 bit resolution is provided on subcarrier.

The numeric ratio between Y and C output is acc. to standards.

Closed Caption Encoder:

By means of this circuit, data acc. to the specification of Closed Caption or Extended Data Service, delivered by the control interface, can be encoded (LINE21). Two dedicated pairs of bytes (two bytes per field), each pair preceded by run-in clocks and framing code, are possible.

The actual line number where data are to be encoded in, can be modified in a certain range.

Data clock frequency is acc. to definition for NTSC-M standard 32 times horizontal line frequency.

Data LOW at the output of the DACs corresponds to 0 IRE, data HIGH at the output of the DACs corresponds to about 50 IRE.

It is also possible to encode Closed Caption Data for 50 Hz field frequencies at 32 times horizontal line frequency.

Output Interface

In the output interface encoded Y and C signals are converted from digital to analog in 10 bit resolution both. Y and C signals are combined to a 10 bit wide CVBS-signal, as well; in front of the summation point, the luminance signal can optionally be fed through a further filter stage, suppressing components in the range of subcarrier frequency. Thus, a kind of Cross Colour reduction is provided, useful in a standard TV set with CVBS input.

Slopes of synchronization pulses are not affected with any Cross Colour reduction active.

Three different filter characteristics or bypass are available, see fig. 5 for 60 Hz field rate and fig. 9 for 50 Hz field rate.

The CVBS output occurs with the same processing delay as the Y,C outputs do. Absolute amplitudes at the input of the DAC for CVBS is reduced by 15/16 w.r.t. Y- and C- DACs to make optimized use of conversion ranges.

Outputs of all DACs can be set together via software control to minimum output voltage for either purpose.

Synchronization

The synchronization of the DENC2-SQ is able to operate in two modes:

In the slave mode, the circuit accepts sync pulses at the bi-directional RCV1 port. The timing and trigger behaviour related to the video signal on VP ports can be influenced by programming the polarity and on-chip delay of RCV1. Active slope of RCV1 defines the vertical phase and optionally the odd/even-and colour frame phase to be initialized, it can be used also to set the horizontal phase.

If the horizontal phase shall not be influenced by RCV1, a horizontal pulse needs to be supplied at the RCV2 pin. Timing and trigger behaviour can be influenced for RCV2, as well.

If there are missing pulses at RCV1 and/or RCV2, the time base of DENC2-SQ runs free, thus an arbitrary number of sync slopes may miss, but no additional pulses (such with wrong phase) must occur.

If the vertical and horizontal phase is derived from RCV1, RCV2 can be used for horizontal or composite blanking input or output.

In the master mode, the time base of the circuit runs free continuously. On the RCV1 port, the IC can output:

- a Vertical Sync signal (VS) with 3 or 2.5 lines duration, or
- an ODD/EVEN signal which is low in odd fields, or
- a field sequence signal (FSEQ) which is high in the first of 4 resp. 8 fields.

On the RCV2 port, the IC can provide a horizontal pulse with programmable start and stop phase; this pulse can be inhibited in the vertical blanking period to build up e.g. a composite blanking signal.

The phase of the pulses output on RCV1 or RCV2 are related on the VP ports, polarity of both signals is selectable.

On the RCM1 port the same types of signals as on RCV1 (as output) are available; on RCM2 the IC provides a horizontal pulse with programmable start and stop phase.

The length of a field as well as start and end of its active part can be programmed. The active part of a field always starts at the beginning of a line.

Control Interface

DENC2-SQ contains two control interfaces: An IIC slave transceiver and 8 bit parallel microprocessor interface. The interfaces cannot be used simultaneously.

The IIC bus interface is a standard slave transceiver, supporting 7 bit slave addresses and 100 $^{kBit}/_{sec}$ guaranteed transfer rate. It uses 8 bit subaddressing with auto-increment function. All registers are write-only, except one readable status byte.

Two IIC slave addresses can be selected (pin SEL_MPU must be low!):

88h: Low at pin 61

8Ch: High at pin 61

The parallel interface is defined by

D(7-0) data bus

CSN low-active chip select signal

RWN read/write not signal, low for a write cycle

DTACKN 680XX style data acknowledge (hand-shake), active low

A0 register select, low selects address, high selects data

The parallel interface uses two registers, one auto-incremental containing the current address of a control register (equals subaddress with IIC control), one containing actual data. The currently addressed register is mapped to the corresponding control register.

Via a read access to the address register, the status byte can be read optionally; no other read access is provided.

Input levels and formats

DENC2-SQ expects digital YUV data with levels (digital codes) acc to CCIR601:

Deviating amplitudes of the colour difference signals can be compensated by independent gain control setting, while gain for luminance is set to pre-defined values, distinguishable for 7.5 IRE setup or without setup.

Reference levels are measured with a colour bar, 100% white, 100% amplitude, 100% saturation.

When the IC is operating with input data acc. to CCIR656, programming can be done alternatively via the parallel interface using VP3 port for data transfer.

For other input modes, the IIC interface has to be used for programming.

CCIR signal component levels

Signal	IRE	dig. level	Code
Y	0	16	straight binary
	50	126	
	100	235	
Cb	bottom peak	16	straight binary
	colourless	128	
	top peak	240	
Cr	bottom peak	16	straight binary
	colourless	128	
	top peak	240	

The 8 bit multiplexed format (CCIR656 like)

Time	0	1	2	3	4	5	6	7
Sample	Cb_0	Y_0	Cr_0	Y_1	Cb_2	Y_2	Cr_2	Y_3
Lum. pixel number	0		1		2		3	
Colour pixel number	0				2			

The 16 bit multiplexed format (DTV2 format)

Time	0	1	2	3	4	5	6	7
Sample Y - line	Y_0		Y_1		Y_2		Y_3	
Sample UV - line	Cb_0		Cr_0		Cb_2		Cr_2	
Lum. pixel number	0		1		2		3	
Colour pixel number	0				2			

The 24 bit direct 444 format

Time	0	1	2	3	4	5	6	7
Sample Y - line	Y_0		Y_1		Y_2		Y_3	
Sample U - line	Cb_0		Cb_1		Cb_2		Cb_3	
Sample V - line	Cr_0		Cr_1		Cr_2		Cr_3	
Lum. pixel number	0		1		2		3	
Colour pixel number	0		1		2		3	

Bit allocation map

Slave Receiver [Slave Address 88h or 8Ch]

REGISTER FUNCTION	SUB-ADDR	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
NULL	00	0	0	0	0	0	0	0	0
				.....					
NULL	39	0	0	0	0	0	0	0	0
Input_Port_Control	3A	CBENB	0	0	0	VY2C	VUV2C	FMT1	FMT0
OSD_LUT_Y0	42	OSDY07	OSDY06	OSDY05	OSDY04	OSDY03	OSDY02	OSDY01	OSDY00
OSD_LUT_U0	43	OSDU07	OSDU06	OSDU05	OSDU04	OSDU03	OSDU02	OSDU01	OSDU00
OSD_LUT_V0	44	OSDV07	OSDV06	OSDV05	OSDV04	OSDV03	OSDV02	OSDV01	OSDV00
				.....					
OSD_LUT_Y7	57	OSDY77	OSDY76	OSDY75	OSDY74	OSDY73	OSDY72	OSDY71	OSDY70
OSD_LUT_U7	58	OSDU77	OSDU76	OSDU75	OSDU74	OSDU73	OSDU72	OSDU71	OSDU70
OSD_LUT_V7	59	OSDV77	OSDV76	OSDV75	OSDV74	OSDV73	OSDV72	OSDV71	OSDV70
Chroma_Phase	5A	CHPS7	CHPS6	CHPS5	CHPS4	CHPS3	CHPS2	CHPS1	CHPS0
Gain_U	5B	GAINU7	GAINU6	GAINU5	GAINU4	GAINU3	GAINU2	GAINU1	GAINU0
Gain_V	5C	GAINV7	GAINV6	GAINV5	GAINV4	GAINV3	GAINV2	GAINV1	GAINV0
Gain_U_MSB, Black_Lev	5D	GAINU8	0	BLCKL5	BLCKL4	BLCKL3	BLCKL2	BLCKL1	BLCKL0
Gain_V_MSB, Blank_Lev	5E	GAINV8	0	BLNNL5	BLNNL4	BLNNL3	BLNNL2	BLNNL1	BLNNL0
NULL	5F	0	0	0	0	0	0	0	0
X-Col_Select	60	CCRS1	CCRS0	0	0	0	0	0	0
Standard_Control	61	0	DOWN	INPI1	YGS	RTCE	SCBW	PAL	FISE
Burst_Amplitude	62	SQP	BSTA6	BSTA5	BSTA4	BSTA3	BSTA2	BSTA1	BSTA0
Subcarrier_0	63	FSC07	FSC06	FSC05	FSC04	FSC03	FSC02	FSC01	FSC00
Subcarrier_1	64	FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC09	FSC08
Subcarrier_2	65	FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16
Subcarrier_3	66	FSC31	FSC30	FSC29	FSC28	FSC27	FSC26	FSC25	FSC24
Line21_Odd_0	67	L21O07	L21O06	L21O05	L21O04	L21O03	L21O02	L21O01	L21O00
Line21_Odd_1	68	L21O17	L21O16	L21O15	L21O14	L21O13	L21O12	L21O11	L21O10
Line21_Even_0	69	L21E07	L21E06	L21E05	L21E04	L21E03	L21E02	L21E01	L21E00
Line21_Even_1	6A	L21E17	L21E16	L21E15	L21E14	L21E13	L21E12	L21E11	L21E10
CC_Line	6B	0	0	0	SCCLN4	SCCLN3	SCCLN2	SCCLN1	SCCLN0
RCV_Port_Control	6C	SRCV11	SRCV10	TRCV2	ORCV1	PRCV1	CBLF	ORCV2	PRCV2
RCM, CC-Mode	6D	0	0	0	0	SRCM11	SRCM10	CCEN1	CCEN0
H-Trigger	6E	HTRIG7	HTRIG6	HTRIG5	HTRIG4	HTRIG3	HTRIG2	HTRIG1	HTRIG0
H-Trigger	6F	0	0	0	0	0	HTRIG10	HTRIG09	HTRIG08

Slave Receiver [Slave Address 88h or 8Ch]

REGISTER FUNCTION	SUB-ADDR	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Fsc_Res_Mode, V-Trigger	70	PHRES1	PHRES0	SBLBN	VTRIG4	VTRIG3	VTRIG2	VTRIG1	VTRIG0
Beg_Master_Request	71	BMRQ7	BMRQ6	BMRQ5	BMRQ4	BMRQ3	BMRQ2	BMRQ1	BMRQ0
End_Master_Request	72	EMRQ7	EMRQ6	EMRQ5	EMRQ4	EMRQ3	EMRQ2	EMRQ1	EMRQ0
MSBs_Mast_Request	73	0	EMRQ10	EMRQ9	EMRQ8	0	BMRQ10	BMRQ9	BMRQ8
NULL	74	0	0	0	0	0	0	0	0
NULL	75	0	0	0	0	0	0	0	0
NULL	76	0	0	0	0	0	0	0	0
Begin_RCV2_out	77	BRCV7	BRCV6	BRCV5	BRCV4	BRCV3	BRCV2	BRCV1	BRCV0
End_RCV2_out	78	ERCV7	ERCV6	ERCV5	ERCV4	ERCV3	ERCV2	ERCV1	ERCV0
MSBs_RCV2_out	79	0	ERCV10	ERCV09	ERCV08	0	BRCV10	BRCV09	BRCV08
Field_Length	7A	FLEN7	FLEN6	FLEN5	FLEN4	FLEN3	FLEN2	FLEN1	FLEN0
First_Act_Line	7B	FAL7	FAL6	FAL5	FAL4	FAL3	FAL2	FAL1	FAL0
Last_Act_Line	7C	LAL7	LAL6	LAL5	LAL4	LAL3	LAL2	LAL1	LAL0
MSBs_Field_Ctrl	7D	0	0	LAL8	FAL8	0	0	FLEN9	FLEN8

I^2C-Bus Format

S	Slave Address	A	Subaddress	A	DATA0	A	--------	DATAn	A	P

Portion	Meaning
S	start condition
Slave Address	1000100X or 1000110X
A	acknowledge, generated by the slave
Subaddress(*)	subaddress byte
DATA	data byte
--------	continued data bytes and A's
P	stop condition
	X: read/write control bit; X=0 is order to write; X=1 is order to read, no subaddressing with read.

(*) if more than 1 byte DATA is transmitted, then auto-increment of the subaddress is performed.

Slave Receiver

Subaddress 3A:

FMT	Select input data format		
	FMT1	FMT0	function
	0	0	input data YUV 444, 24 lines, Y on VP1, Cr on VP2, Cb on VP3 (default after reset)
	0	1	input data YUV 422, 16 lines, Y on VP1, multiplexed CbCr on VP3
	1	0	input data YUV 422, 8 lines, multiplexed acc. to CCIR-656 on VP1
	1	1	input data YUV 422, 8 lines, multiplexed acc. to CCIR-656 on VP1
VUV2C	0	Cb/Cr data input to VP ports are two's complement (default after reset)	
	1	Cb/Cr data input to VP ports are straight binary	
VY2C	0	Y data input to VP1 port are two's complement (default after reset)	
	1	Y data input to VP1 port are straight binary	
CBENB	0	Data from input ports are encoded (default after reset)	
	1	Colour Bar with programmable colours (entries of OSD-LUTs) is encoded The LUTs are read in upward order from index 0 to index 7.	

Subaddress 42 .. 59:

OSDY
OSDU
OSDV

Contents of OSD Look-up tables. All 8 entries are 8 bits. Data representation is acc. to CCIR 601 [Y,Cb,Cr], but two's complement, e.g. for a 100/100 [upper number] or 100/75 [lower number] Colour Bar:

Colour	OSDY	OSDU	OSDV	index (for normal colour bar with CBENB = 1)
White	107(6Bh) 107(6Bh)	0(00h) 0(00h)	0(00h) 0(00h)	0
Yellow	82(52h) 34(22h)	144(90h) 172(ACh)	18(12h) 14(0Eh)	1
Cyan	42(2Ah) 03(03h)	38(26h) 29(1Dh)	144(90h) 172(ACh)	2
Green	17(11h) 240(F0h)	182(B6h) 200(C8h)	162(A2h) 185(B9h)	3
Magenta	234(EAh) 212(D4h)	74(4Ah) 56(38h)	94(5Eh) 71(47h)	4
Red	209(D1h) 193(C1h)	218(DAh) 227(E3h)	112(70h) 84(54h)	5
Blue	169(A9h) 163(A3h)	112(70h) 84(54h)	238(EEh) 242(F2h)	6
Black	144(90h) 144(90h)	0(00h) 0(00h)	0(00h) 0(00h)	7

Subaddress 5A:

CHPS	Phase of encoded colour subcarrier (including burst) relative to H - sync. Can be adjusted in steps of 360/256 degrees.

Subaddress 5B, 5D:

GAINU	Variable gain for Cb signal (Input Representation acc. to CCIR 601) White - Black = 92.5 IRE White - Black = 92.5 IRE GAINU=0 Output subcarrier of U contribution = 0 GAINU=118 (76h) Output subcarrier of U contribution = nominal GAINU = -2.17 * nominal ... nominal ... 2.16 * nominal White - Black = 100 IRE GAINU= 0 Output subcarrier of U contribution = 0 GAINU=125 (7Dh) Output subcarrier of U contribution = nominal GAINU = -2.05 * nominal ... nominal ... 2.04 * nominal

Subaddress 5C, 5E:

GAINV	Variable gain for Cr signal (Input Representation acc. to CCIR 601) White - Black = 92.5 IRE GAINV= 0 Output subcarrier of V contribution = 0 GAINV=165 (A5h) Output subcarrier of V contribution = nominal GAINV = -1.55 * nominal ... nominal ... 1.55 * nominal White-Black = 100 IRE GAINV= 0 Output subcarrier of V contribution = 0 GAINV=175 (AFh) Output subcarrier of V contribution = nominal GAINV = -1.46 * nominal ... nominal ... 1.46 * nominal

Subaddress 5D:

BLCKL	Variable Black Level (Input Representation acc. to CCIR 601) White - Sync = 140 IRE BLCKL= 0 Output Black Level = 24 IRE BLCKL= 63 (3Fh) Output Black Level = 49 IRE Output Black Level/IRE = BLCKL * 25/63 + 24 Recommended Value: BLCKL = 60 (3Ch) (normal) White-Sync = 143 IRE BLCKL= 0 Output Black Level = 24 IRE BLCKL= 63 (3Fh) Output Black Level = 50 IRE Output Black Level/IRE = BLCKL * 26/63 + 24 Recommended Value: BLCKL = 45 (2Dh) (normal)

Subaddress 5E:

BLNNL	Variable Blanking Level White - Sync = 140 IRE BLNNL= 0 Output Blanking Level = 17 IRE BLNNL= 63 (3Fh) Output Blanking Level = 42 IRE Output Blanking Level/IRE = BLNNL * 25/63 + 17 Recommended Value: BLNNL = 58 (3Ah) (normal) White - Sync = 143 IRE BLNNL= 0 Output Blanking Level = 17 IRE BLNNL= 63 (3Fh) Output Blanking Level = 43 IRE Output Blanking Level/IRE = BLNNL * 26/63 + 17 Recommended Value: BLNNL = 63 (3Fh) (normal)

Subaddress 60:

CCRS	Select cross colour reduction filter in luminance		
	CCRS1	CCRS0	function
	0	0	No Cross Colour Reduction (for transfer characteristic of luminance see figs. 5, 9)
	0	1	Cross Colour Reduction #1 active (for transfer characteristic see figs. 5, 9)
	1	0	Cross Colour Reduction #2 active (for transfer characteristic see figs. 5, 9)
	1	1	Cross Colour Reduction #3 active (for transfer characteristic see figs. 5, 9)

Subaddress 61:

FISE	0	944 total pixel clocks per line
	1	780 total pixel clocks per line (default after reset)
PAL	0	NTSC Encoding (non-alternating V-component) (default after reset)
	1	PAL Encoding (alternating V-component)
SCBW	0	Enlarged Bandwidth for Chrominance Encoding (for overall transfer characteristic of chrominance in base-band representation see figs. 3 and 4, 7 and 8).
	1	Standard Bandwidth for Chrominance Encoding (for overall transfer characteristic of chrominance in base-band representation see figs. 3 and 4, 7 and 8). (default after reset)
RTCE	0	No Real Time Control of generated Subcarrier Frequency (default after reset)
	1	Real Time Control of generated Subcarrier Frequency through SAA7191B (timing see fig. 13)
YGS	0	Luminance Gain for White-Black 100 IRE
	1	Luminance Gain for White-Black 92.5 IRE incl. 7.5 IRE Set-up of Black (default after reset)
INPI	0	PAL Switch phase is nominal (default after reset)
	1	PAL Switch phase is inverted compared to nominal
DOWN	0	DACs in normal operational mode (default after reset)
	1	DACs forced to lowest output voltage

Subaddress 62:

BSTA	Amplitude of Colour Burst (Input Representation acc. to CCIR 601) White-Black = 92.5 IRE, Burst = 40 IRE, NTSC-Encoding BSTA = 0 .. 1.25 * nominal Recommended Value: BSTA = 102(66h) White-Black = 92.5 IRE, Burst = 40 IRE, PAL-Encoding BSTA = 0 .. 1.76 * nominal Recommended Value: BSTA = 72(48h) White-Black = 100 IRE, Burst = 43 IRE, NTSC-Encoding BSTA = 0 .. 1.20 * nominal Recommended Value: BSTA = 106(6Ah) White-Black = 100 IRE, Burst = 43 IRE, PAL-Encoding BSTA = 0 .. 1.67 * nominal Recommended Value: BSTA = 75(4Bh)
SQP	0 not supported in current version, do not use 1 Subcarrier Real Time Control from 7191B Digital Colour Decoder

Note to subaddresses 5B,5C,5D,5E,62: All IRE values are rounded

Subaddress 63 .. 66 :

FSC0 ... FSC3	Four bytes to program subcarrier frequency $FSC = round\left(\frac{F(fsc)}{F(llc)} \times 2^{32}\right)$ $F(fsc)$ Subcarrier frequency (in multiples of line frequency) $F(llc)$ Clock frequency (in multiples of line frequency) FSC3 Most significant byte FSC0 Least significant byte
	Examples: NTSC-M: $F(fsc) = 227.5$, $F(llc) = 1560$ ==> FSC = 626349397 (25555555h) PAL-B/G: $F(fsc) = 283.7516$, $F(llc) = 1888$ ==> FSC = 645499916 (26798C0Ch)

Subaddress 67 .. 6A:

L21O0	First Byte of Captioning Data, Odd Field
L21O1	Second Byte of Captioning Data, Odd Field
L21E0	First Byte of Extended Data, Even Field
L21E1	Second Byte of Extended Data, Even Field
	LSBs of the respective bytes are encoded immediately after run-in and framing code, the MSBs of the respective bytes have to carry the parity bit, acc. to the definition of line 21 encoding format.

Subaddress 6B

SCCLN	Selects the actual line, where Closed Caption or Extended Data are encoded. Line = (SCCLN + 4) for M-systems Line = (SCCLN + 1) for other systems

Subaddress 6C:

PRCV2	0	Polarity of RCV2 as output is high-active, rising edge is taken when input, respectively (default after reset).
	1	Polarity of RCV2 as output is low-active, falling edge is taken when input, respectively
ORCV2	0	Pin RCV2 is switched to input (default after reset).
	1	Pin RCV2 is switched to output
CBLF	0	If ORCV2=high, pin RCV2 provides a HREF signal (Horizontal Reference Pulse that is high during active portion of line, also during Vertical Blanking Interval). (default after reset) If ORCV2=low, signal input to RCV2 is used for horizontal synchronization only (if TRCV2 = 1). (default after reset)
	1	If ORCV2=high, pin RCV2 provides a CBN signal (Reference Pulse that is high during active video, excluding Vertical Blanking Interval). If ORCV2=low, signal input to RCV2 is used for horizontal synchronization (if TRCV2 = 1)as well as an internal blanking signal
PRCV1	0	Polarity of RCV1 as output is high-active, rising edge is taken when input, respectively. (default after reset)
	1	Polarity of RCV1 as output is low-active, falling edge is taken when input, respectively.
ORCV1	0	Pin RCV1 is switched to input (default after reset).
	1	Pin RCV1 is switched to output.
TRCV2	0	Horizontal synchronization is taken from RCV1 port. (default after reset)
	1	Horizontal synchronization is taken from RCV2 port.
SRCV1	Defines signal type on pin RCV1	

SRCV11	SRCV10	as output	as input	
0	0	VS	VS	Vertical Sync each field (default after reset)
0	1	FS	FS	Frame Sync (_odd/even)
1	0	FSEQ	FSEQ	Field SEQuence, Vertical sync every fourth (FISE=1) or eighth field (FISE=0)
1	1	n.a.	n.a.	

Subaddress 6D:

CCEN	Enables individual Line 21 Encoding	

CCEN1	CCEN0	
0	0	Line 21 Encoding OFF
0	1	Enables Encoding in field 1 (odd)
1	0	Enables Encoding in field 2 (even)
1	1	Enables Encoding in both fields

SRCM — Defines signal type on pin RCM1

SRCM1	SRCM0	as output	
0	0	VS	Vertical Sync each field
0	1	FS	Frame Sync (_odd/even)
1	0	FESQ	Field SEQuence, Vertical sync every fourth (FISE=1) or eight field (FISE=0)
1	1	n.a.	

Subaddress 6E .. 6F:

HTRIG	Sets the Horizontal TRIGger phase related to signal on RCV1 or RCV2 input. Values above 1559 (FISE=1) or 1887 [FISE=0] are not allowed. Increasing HTRIG decreases delays of all internally generated timing signals. Reference mark: Analog output horizontal sync (leading slope) coincides with active edge of RCV used for triggering at HTRIG = 031h [033h]

Subaddress 70:

VTRIG		Sets the Vertical TRIGger phase related to signal on RCV1 input. Increasing VTRIG decreases delays of all internally generated timing signals, measured in half lines Variation range of VTRIG = 0 .. 31(1Fh)
SBLBN	0	Vertical Blanking is defined by programming of FAL and LAL.
	1	Vertical Blanking is forced automatically at least during field synchronization and equalization pulses. Note: If Cross-Colour Reduction is programmed, it is active between FAL and LAL in both cases.
PHRES		Selects the phase reset mode of the colour subcarrier generator

PHRES1	PHRES0	
0	0	no reset
0	1	reset every two lines
1	0	reset every eight fields
1	1	reset every four fields

Subaddress 71 .. 73:

BMRQ	Begin of Master ReQuest signal (RCM2). Values above 1559 (FISE=1) or 1887 [FISE=0] are not allowed. First active pixel at analog outputs (corresp. input pixel coinciding with RCM2) at BMRQ=0E1h [130h]
EMRQ	End of Master ReQuest signal (RCM2). Values above 1559 (FISE=1) or 1887 [FISE=0] are not allowed. Last active pixel at analog outputs (corresp. input pixel coinciding with RCM2) at EMRQ=5E9h [72Ah]

Subaddress 77 .. 79:

BRCV	Begin of output signal on RCV2 pin. Values above 1559 (FISE=1) or 1887 [FISE=0] are not allowed. First active pixel at analog outputs (corresp. input pixel coinciding with RCV2) at BRCV=0E1h [130h]
ERCV	End of output signal on RCV2 pin. Values above 1559 (FISE=1) or 1887 [FISE=0] are not allowed. Last active pixel at analog outputs (corresp. input pixel coinciding with RCV2) at ERCV=5E9h [72Ah]

Subaddress 7A .. 7D:

FLEN	LENgth of a Field = FLEN + 1, measured in half lines Valid range is limited to 524 . . 1022 (FISE=1) resp. 624 .. 1022 (FISE=0), FLEN should be even
FAL	First Active Line, measured in lines. FAL=0 coincides with the first field synchronization pulse.
LAL	Last Active Line, measured in lines LAL=0 coincides with the first field synchronization pulse.

Slave Transmitter

Slave Transmitter [Slave Address 89h or 8Dh]

REGISTER FUNCTION	SUB-ADDR	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Status Byte	-	VER2	VER1	VER0	CCRDE	CCRDO	FSQ2	FSQ1	FSQ0

no subaddress

VER	Version id of the device. It will be changed with all versions of the IC that have different programming models Current Version is 000 bin.
CCRDE	Closed caption bytes of the even field have been encoded. The bit is reset after information has been written to the subbaddresses 69, 6A. It is set immediately after the data have been encoded.
CCRDO	Closed caption bytes of the odd field have been encoded. The bit is reset after information has been written to the subbaddresses 67, 68. It is set immediately after the data have been encoded.
FSQ	State of the internal field sequence counter. Bit 0 (FSQ0) gives the odd/even information. (Odd=Low, Even=High)

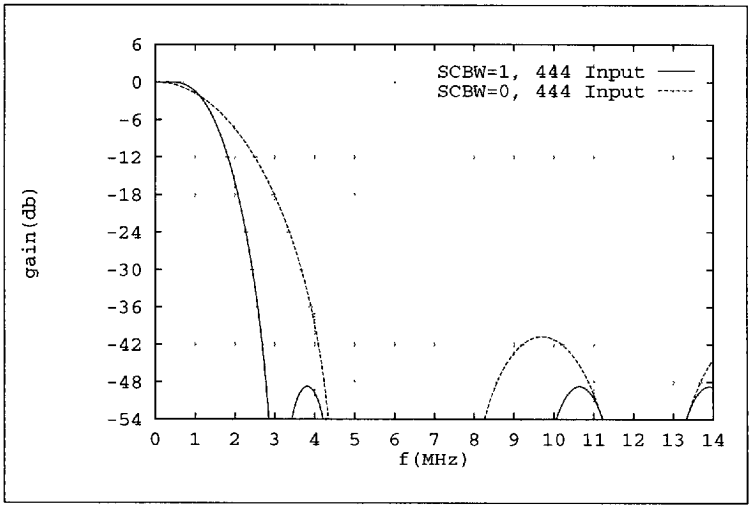


Fig. 3: Chrominance transfer characteristic [60 Hz]

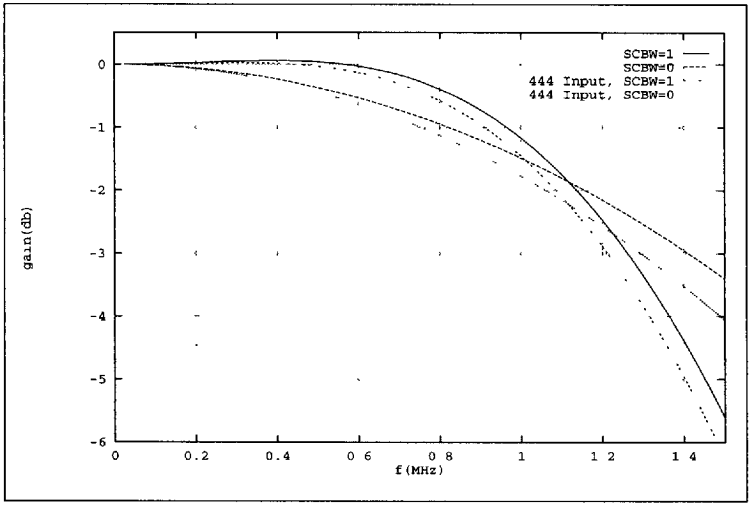


Fig. 4: Chrominance transfer characteristic [60 Hz]

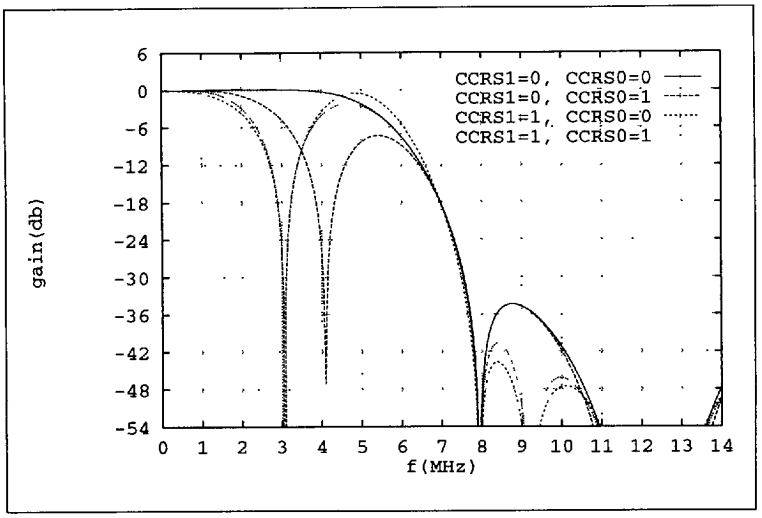


Fig. 5: Luminance transfer characteristic [60 Hz]

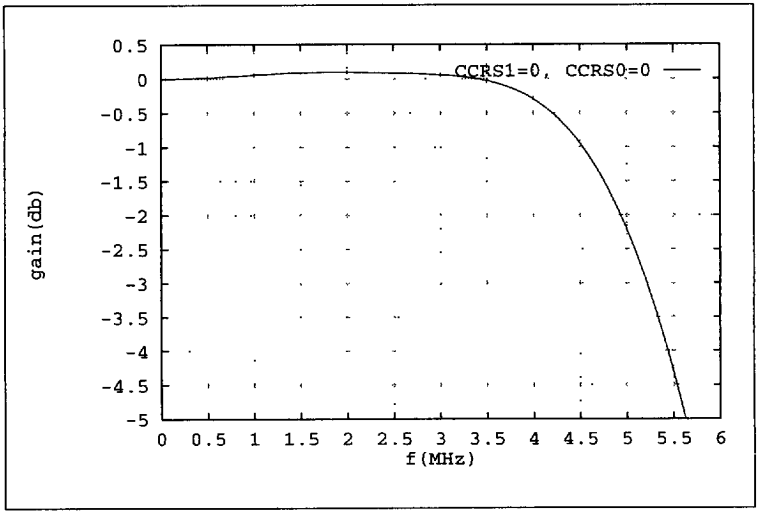


Fig. 6: Luminance transfer characteristic [60 Hz]

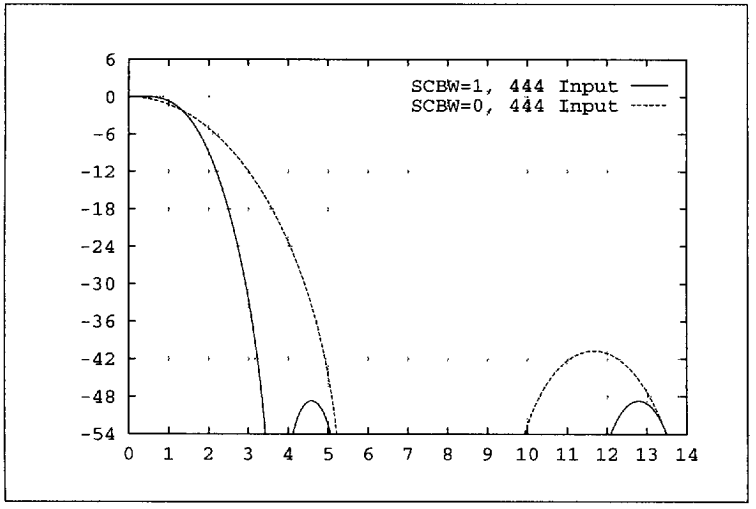


Fig. 7: Chrominance transfer characteristic [50 Hz]

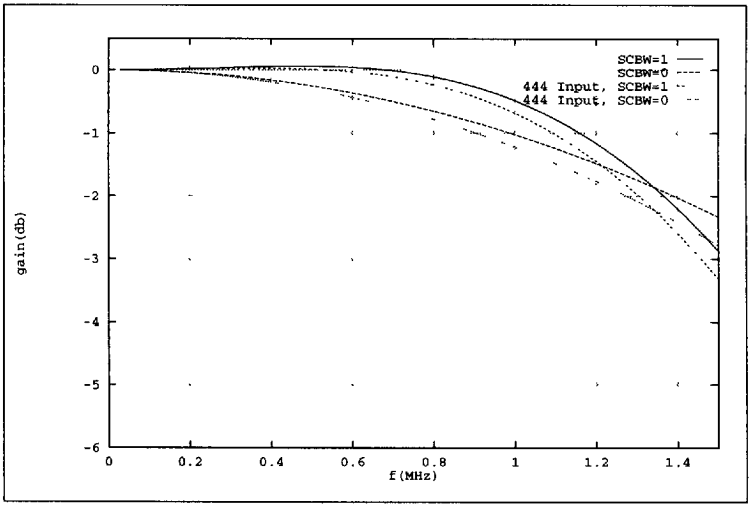


Fig. 8: Chrominance transfer characteristic [50 Hz]

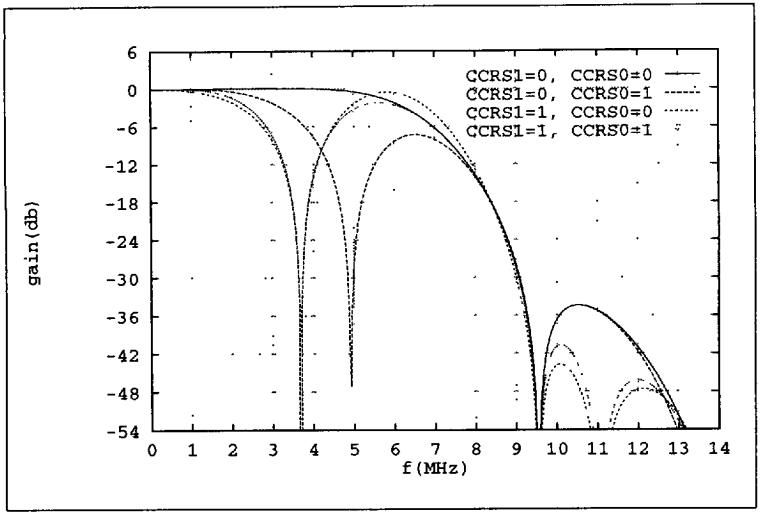


Fig. 9: Luminance transfer characteristic [50 Hz]

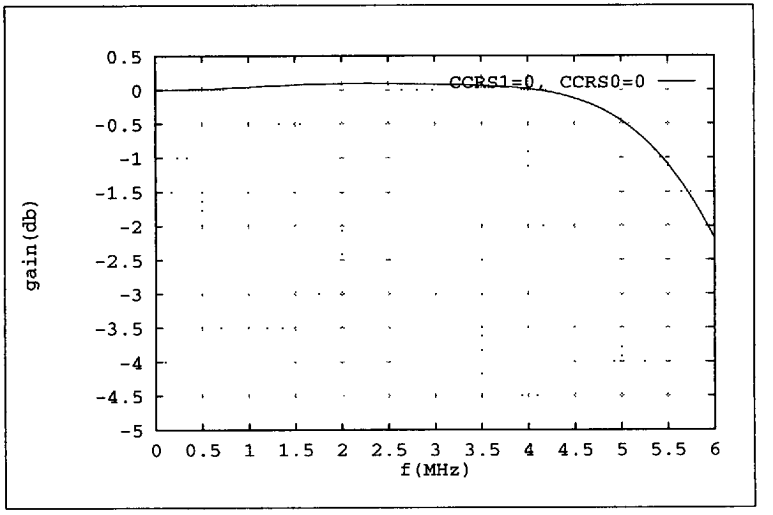


Fig. 10: Luminance transfer characteristic [50 Hz]

Electrical Characteristics

Conditions: T_{amb} = 0 .. 70 °C; V_{DDD}= 4.5 .. 5.5 V unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
Supply					
V_{DDD}	supply voltage range digital		4.5	5.5	V
V_{DDA}	supply voltage range analog		4.75	5.25	V
I_{DDD}	supply current	1)	-	210	mA
I_{DDA}	supply current	1)	-	55	mA
Inputs					
V_{IL}	input voltage LOW (except SDA, SCL, AP, SP, XTALI)		-0.5	0.8	V
V_{IH}	input voltage HIGH (except SDA, SCL, AP, SP, XTALI)		2.0	V_{DDD}+0.5	V
V_{IH}	input voltage HIGH (LLC)	pin 38, only	2.4	V_{DDD}+0.5	V
I_{LI}	input leakage current		-	1	µA
C_I	input capacitance	clocks	-	10	pF
C_I	input capacitance	data		8	pF
C_I	input capacitance	I/O at high impedance		8	pF
Outputs					
V_{OL}	output voltage LOW (except XTAL, SDA)	2)	0	0.6	V
V_{OH}	output voltage HIGH (except XTAL,DTACKN, SDA)	2)	2.4	V_{DDD}+0.5	V
V_{OH}	output voltage HIGH (LLC)	2) pin 38, only	2.6	V_{DDD}+0.5	V
I^2C Bus SDA and SCL					
V_{IL}	input voltage LOW		-0.5	1.5	V
V_{IH}	input voltage HIGH		3.0	V_{DDD}+0.5	V
I_I	input current	V_I= low or high		+/-10	µA
V_{OL}	SDA output voltage	I_O= 3 mA		0.4	V
I_O	output current	during acknowl.	3		mA
Clock timing					
t_{LLC}	cycle time LLC	3)	31	44	ns
δ	duty factor t_{LLCh} / t_{LLC}	10)	40	60	%
t_r	rise time LLC	3)	-	5	ns
t_f	fall time LLC	3)	-	6	ns
Input timing					
t_{SUC}	input data setup time (CREF)		6	-	ns
t_{HDC}	input data hold time (CREF)		3	-	ns
t_{SU}	input data setup time (any other except SEL_MPU, CDIR, RWN/SCL, A0/SDA, CSN/SA, RESN, AP, SP)		6	-	ns

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
t_{HD}	input data hold time (any other except SEL_MPU, CDIR, RWN/SCL, A0/SDA, CSN/SA, RESN, AP, SP)		3	-	ns
Crystal Oscillator					
f_n	nominal frequency (usually 24.545454 MHz or 29.5 MHz)	3rd harmonic	-	30	MHz
Df/f_n	permissible deviation fn	9)	-50	+50	10^{-6}
	crystal specification:				
	temperature range Tamb		0	70	C
	load capacitance C_L		8	-	pF
	series resonance resistance R_S			80	Ω
	motional capacitance C_1	typically	1.5-20%	1.5+20%	fF
	parallel capacitance C_0	typically	3.5-20%	3.5+20%	pF
MPU interface timing					
t_{AS}	address setup time	5)	9	-	ns
t_{AH}	address hold time		0	-	ns
t_{RWS}	read/write setup time	5)	9	-	ns
t_{RWH}	read/write hold time		0	-	ns
t_{DD}	data valid from CSN (read)	6), 7), 8), n=9	-	440	ns
t_{DF}	data bus floating from CSN (read)	6), 7), n=5	-	275	ns
t_{DS}	data bus setup time (write)	5)	9	-	ns
t_{DH}	data bus hold time (write)	5)	9	-	ns
t_{ACS}	acknowledge delay from CSN	6), 7), n=11	-	520	ns
t_{CSD}	CSN high from acknowledge		0	-	ns
t_{DAT}	DTACKN floating from CSN high	6), 7), n=7	-	360	ns
Data and reference signal output timing					
C_L	output load capacitance		7.5	40	pF
t_{OH}	output hold time		4	-	ns
t_{OD}	output delay time (CREF in output mode)		-	25	ns
C, Y, and CVBS outputs					
Vo	output signal (peak to peak value)	4)	1.9	2.1	V
R_I	internal serial resistance		18	35	Ω
R_L	output load resistance		80	-	Ω
B	output signal bandwidth (D/A-converters)	-3dB	10	-	MHz
ILE	LF integral linearity error (D/A-converters)		-	± 2	LSB
DLE	LF differential linearity error (D/A-converters)		-	± 1	LSB

Notes:

1) at maximum supply voltages and with high-activity input signals

2) The levels have to be measured with load circuits of 1.2 kΩ to 3.0 V (standard TTL load), C_L = 25pF.

3) The data is for both, input and output direction.

4) for full digital range, without load, V_{DDA} = 5.0 V. The typical voltage swing is 2.0 V, the typical minimum output voltage (digital zero at DAC) is 0.2 V.

5) The value is calculated via equation (1)

6) The value depends on the clock frequency. The numbers given are calculated with f_{LLC} = 24.54 MHz

7) The values are calculated via equation (2)

8) The falling edge of DTACKN will always occur 1 * LLC after data is valid.

9) If internal oscillator is used, crystal deviation of fn is directly proportional to the deviation of subcarrier frequency and line/ field frequency.

10) With LLC in input mode. In output mode, with a crystal connected to XTAL/ XTALI typically 50 %.

Equations:

(1) $t = t_{SU} + t_{HD}$

(2) $t_{dmax} = t_{OD} + n*t_{LLC} + t_{LLC} + t_{SU}$

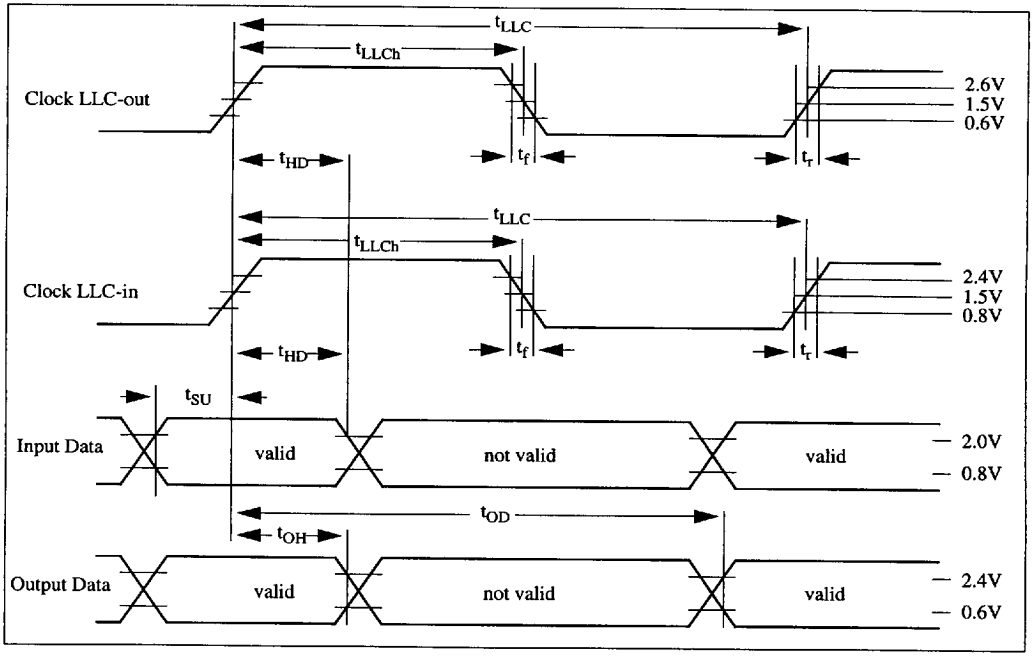


Fig. 11: Clock Data Timing

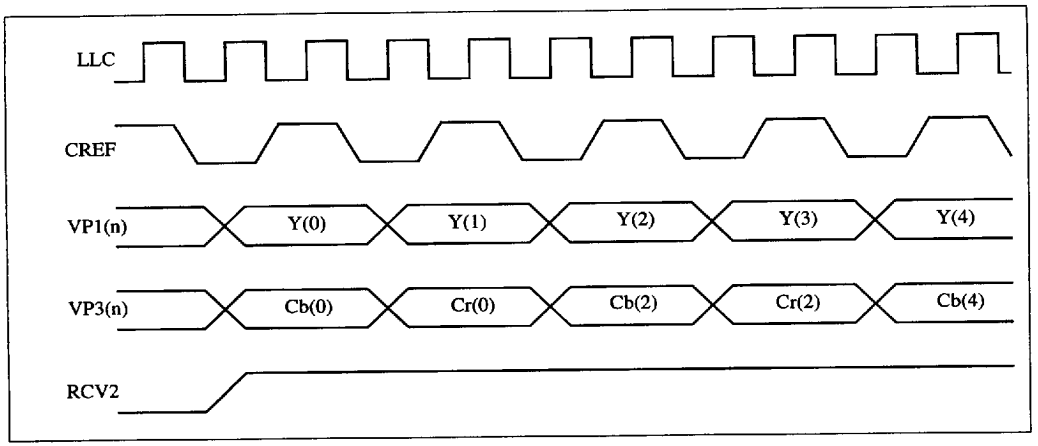


Fig. 12: Dig.TV - Timing

Notes:

1) The data demultiplex phase is coupled to the internal horizontal phase.
2) The CREF signal applies only for the 16 lines DIG-TV format,because these signals are only valid in 12.27/14.75MHz.
3) The phase of the RCV2 signal is programmed to 0E1h [130h for 50 Hz] in this example in output mode (BRCV2)

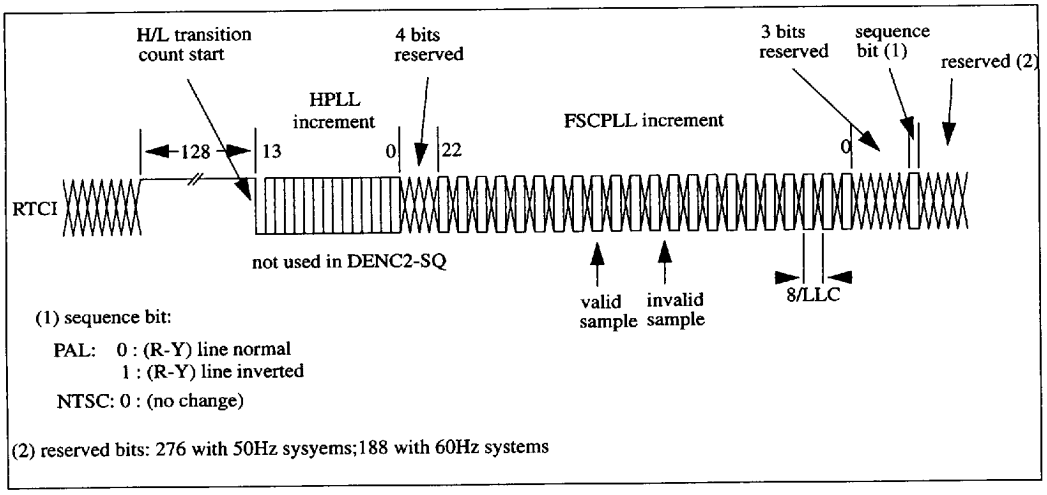


Fig. 13: RTCI timing

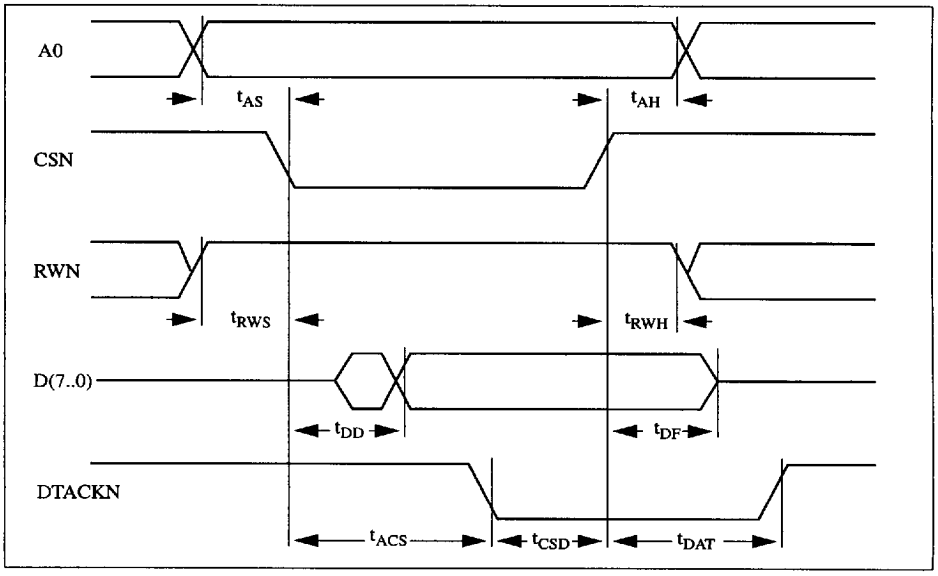


Fig. 14: MPU Interface Timing (Read cycle)

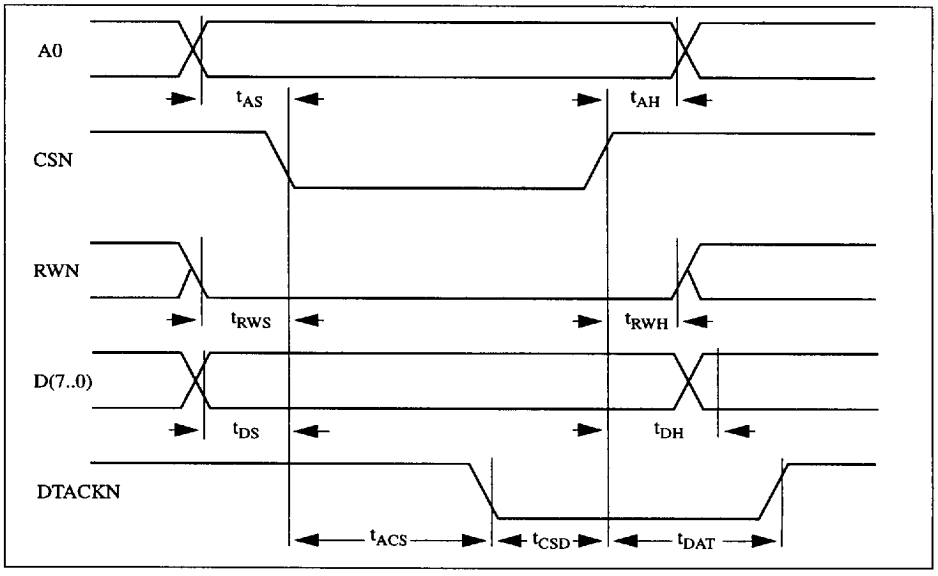


Fig. 15: MPU Interface Timing (Write cycle)

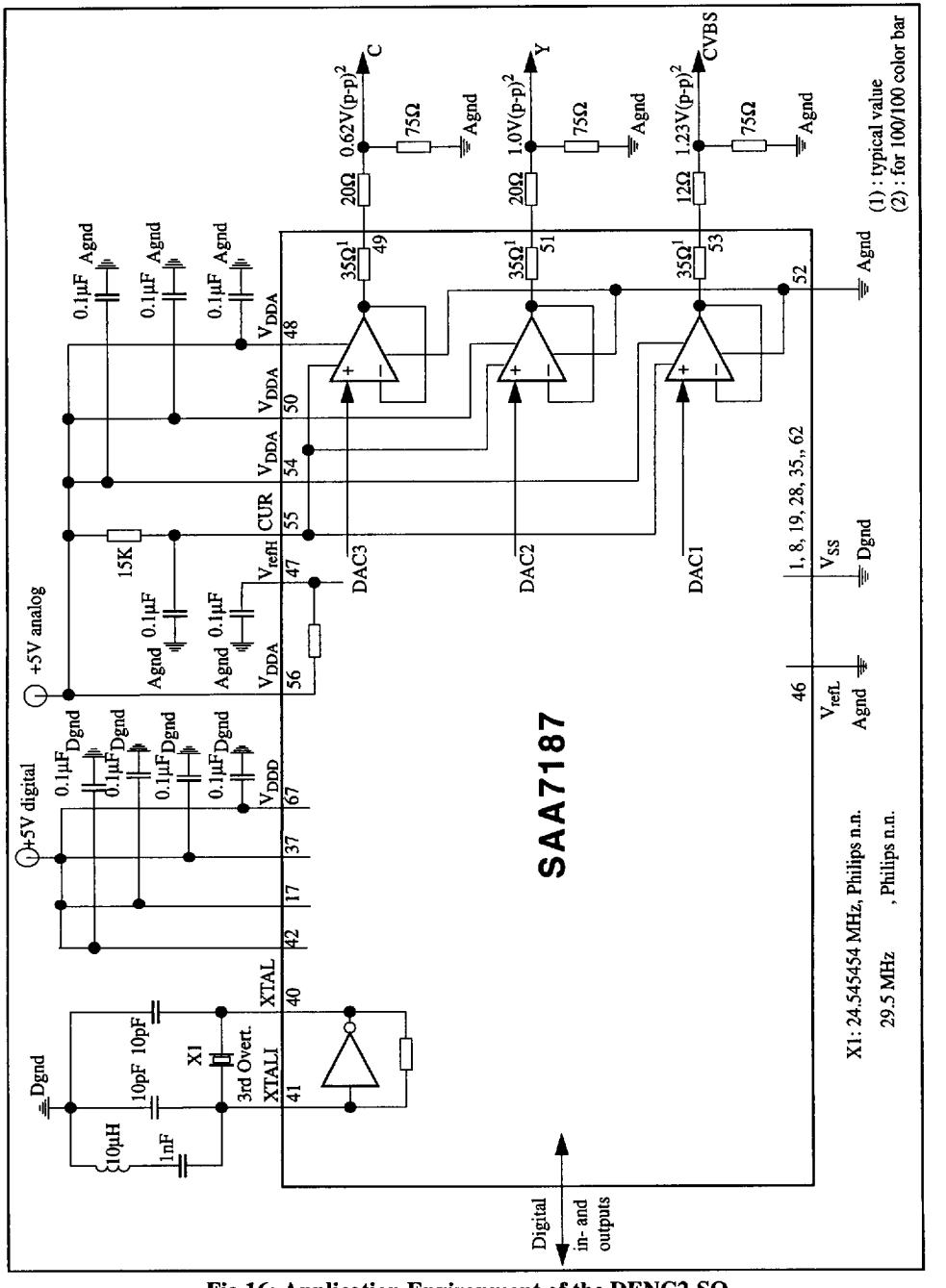


Fig.16: Application Environment of the DENC2-SQ