

TOSHIBA SOLID STATE I/O INTERFACE MODULE

TF1107

DC INPUT MODULE

TOSHIBA TF1107 is DC Line Voltage Input I/O Interface Module and it includes the optical isolator. Using this Module, you can design high reliability and compact system.

- Recommended Input Voltage : $V_{IN}=12\sim24V$
- Input Impedance : $Z_{IN}=3.1k\Omega$
- 1500V AC Optical Isolation
- Wide Supply Voltage : $V_{CC}=5\sim18V$
- Including Delay Time Circuit
- Output is Compatible with TTL and CMOS Logic
- Small Size and Light Weight

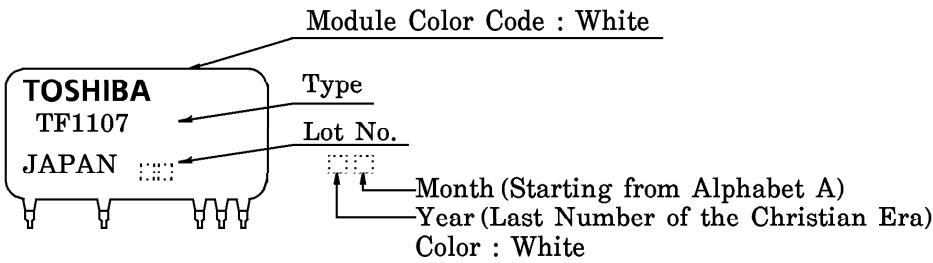
MAXIMUM RATINGS ($T_a = 25^{\circ}C$)
INPUT (DC LINE VOLTAGE)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Input Voltage (DC)	V_{IN}	30	V
Input Current (DC)	I_{IN}	10	mA
Operating Frequency Range	f	65	Hz

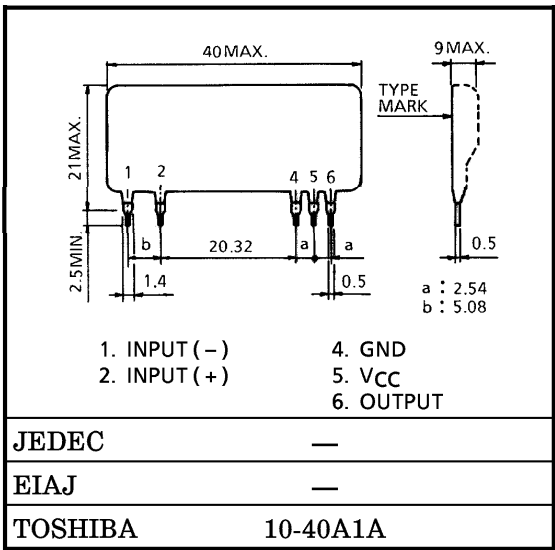
OUTPUT (LOGIC CONTROL)

Logic Supply Voltage	V_{CC}	20	V
Output Voltage	V_{OUT}	$-0.5\sim V_{CC}+0.5$	V
Output Current	I_{OUT}	6	mA
Isolation Voltage (Input-Output) (AC)	BV_S/AC	1500 (1min)	V
Operating Temperature Range	T_{opr}	$-20\sim80$	$^{\circ}C$
Storage Temperature Range	T_{stg}	$-20\sim80$	$^{\circ}C$
Lead Soldering Temperature (10s)	T_{sol}	260	$^{\circ}C$

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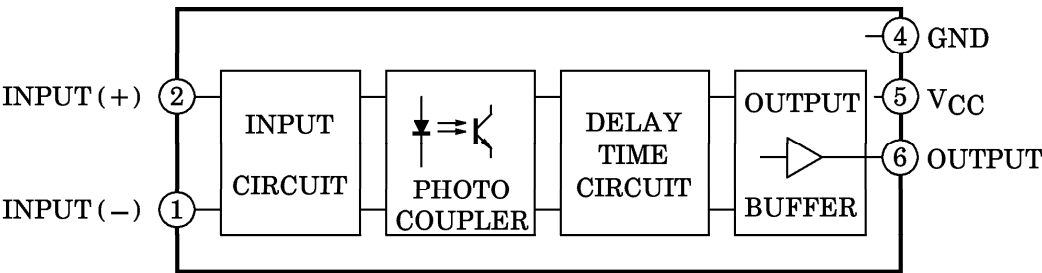


Unit in mm



Weight : 7g

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (Ta = 25°C, VCC = 5V)
INPUT (DC LINE VOLTAGE)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage	"H" Level	VILH	IOUT < 1μA, VOUT > 4.5V	—	7.8	12	V
	"L" Level	VIHL	IOUT < 1μA, VOUT < 0.5V	5	7.5	—	
Input Current	"H" Level	IILH	IOUT < 1μA, VOUT > 4.5V	—	1.4	—	mA
	"L" Level	IIDL	IOUT < 1μA, VOUT < 0.5V	—	1.3	—	
Input Impedance		ZIN	VIN = 24V	—	3.1	—	kΩ

OUTPUT (LOGIC CONTROL)

Output Voltage	"H" Level	VOH	IOUT = -10μA, VIN = 24V	4.5	4.9	—	V
	"L" Level	VOL	IOUT = 2.5mA, VIN = 0V	—	0.3	0.5	
Output Current (sink)		IOUT	VOL = 1.5V, VIN = 0V	6	16	—	mA
Supply Current	"H" Level	ICCH	IOUT < 1μA, VIN = 24V	—	1.0	5	mA
	"L" Level	ICCL	IOUT < 1μA, VIN = 0V	—	1.4	6	
Propagation Delay Time	"H" Level	tPLH	VIN = 0 → 24V	—	4.2	8	ms
	"L" Level	tPHL	VIN = 24 → 0V	—	5.5	10	
Isolation Resistance		RS	V = 1kV, R.H = 40~60%	—	10 ¹⁰	—	Ω

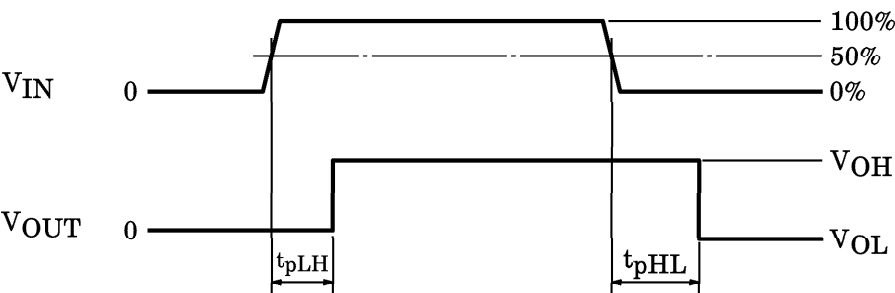


Fig.1 SWITCHING TIME TEST CONDITION

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