

TOSHIBA Multi-Chip Transistor

Silicon NPN Epitaxial Type, Field Effect Transistor Silicon N Channel MOS Type

TPCP8H01

HIGH-SPEED SWITCHING APPLICATIONS

LORD SWITCHING APPLICATIONS

STROBE FLASH APPLICATIONS

- Multi-chip discrete device; built-in NPN transistor for main switch and N-ch MOS FET for drive
- High DC current gain: $h_{FE} = 250$ to 400 ($I_C = 0.5$ A) (NPN transistor)
- Low collector-emitter saturation voltage: $V_{CE(sat)} = 0.13$ V (max) (NPN transistor)
- High-speed switching: $t_f = 25$ ns (typ.) (NPN transistor)

Maximum Ratings ($T_a = 25^\circ\text{C}$)

Transistor

Characteristics		Symbol	Rating	Unit
Collector-base voltage		V_{CBO}	100	V
Collector-emitter voltage		V_{CEX}	80	V
		V_{CEO}	50	
Emitter-base voltage		V_{EBO}	6	V
Collector current	DC (Note 1)	I_C	5.0	A
	Pulse (Note 1)	I_{CP}	7.0	
Base current		I_B	0.5	A
Collector power dissipation (NPN)		P_C (Note 2)	1.0	W
Junction temperature		T_j	150	$^\circ\text{C}$

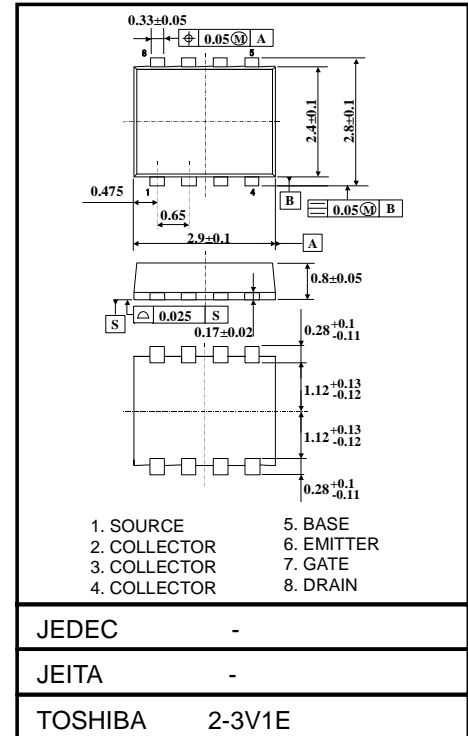
MOS FET

Characteristics		Symbol	Rating	Unit
Drain-Source Voltage		V_{DSS}	20	V
Gate-Source Voltage		V_{GSS}	± 10	V
Drain Current	DC	I_D	100	mA
	Pulse	I_{DP}	200	
Channel Temperature		T_{ch}	150	$^\circ\text{C}$

Note 1: Ensure that the junction (channel) temperature does not exceed 150°C .

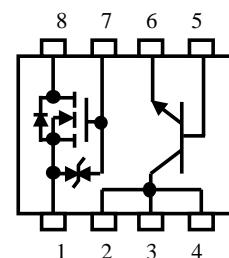
Note 2: Device mounted on a glass-epoxy board (FR-4, $25.4 \times 25.4 \times 1.6$ mm, Cu area: 645 mm^2)

This transistor is an electrostatic-sensitive device. Please handle with caution.



Weight : 0.017g (Typ.)

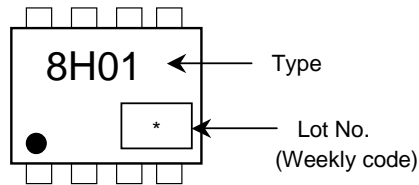
Circuit Configuration



Common maximum rating (Ta = 25°C)

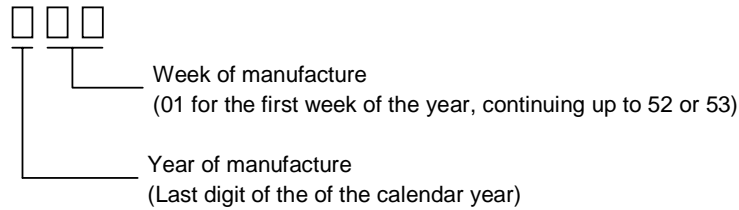
Characteristics	Symbol	Rating	Unit
Storage temperature range	T _{stg}	-55 to 150	°C

Marking (Note 3)



Note 3: The mark “●” on the lower left of the marking indicates Pin 1.

* Weekly code (three digits)

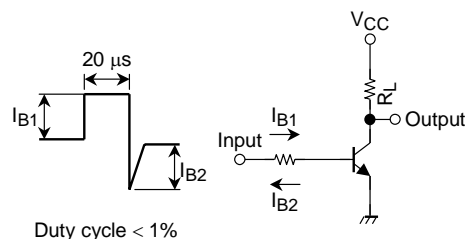


Electrical Characteristics (Ta = 25°C)

Transistor

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Collector cut-off current	I _{CBO}	V _{CB} = 100 V, I _E = 0	—	—	100	nA
Emitter cut-off current	I _{EBO}	V _{EB} = 6 V, I _C = 0	—	—	100	nA
Collector-emitter breakdown voltage	V _{(BR) CEO}	I _C = 10 mA, I _B = 0	50	—	—	V
DC current gain	h _{FE} (1)	V _{CE} = 2 V, I _C = 0.5 A	250	—	400	
	h _{FE} (2)	V _{CE} = 2 V, I _C = 1.6 A	100	—	—	
Collector-emitter saturation voltage	V _{CE (sat)}	I _C = 1.6 A, I _B = 53 mA	—	80	130	mV
Base-emitter saturation voltage	V _{BE (sat)}	I _C = 1.6 A, I _B = 53 mA	—	0.8	1.1	V
Collector output capacitance	C _{ob}	V _{CB} = 10 V, I _E = 0, f = 1 MHz	—	22	—	pF
Switching time	Rise time	t _r	See Figure 1 circuit diagram. V _{CC} ≐ 24 V, R _L = 15 Ω I _{B1} = -I _{B2} = 53 mA		—	ns
	Storage time	t _{stg}			—	
	Fall time	t _f			—	

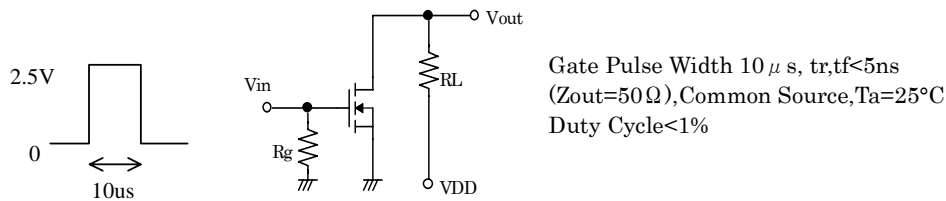
Figure 1 Switching Time Test Circuit & Timing Chart



MOS FET

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	$V_{GS} = \pm 10 \text{ V}, V_{DS} = 0$	—	—	± 1	μA
Drain-Source breakdown voltage		$V_{(BR)DSS}$	$I_D = 0.1 \text{ mA}, V_{GS} = 0$	20	—	—	V
Drain cut-off current		I_{DSS}	$V_{DS} = 20 \text{ V}, V_{GS} = 0$	—	—	1	μA
Gate threshold voltage		V_{th}	$V_{DS} = 3 \text{ V}, I_D = 0.1 \text{ mA}$	0.6	—	1.1	V
Forward transfer admittance		$ Y_{fs} $	$V_{DS} = 3 \text{ V}, I_D = 10 \text{ mA}$	40	—	—	mS
Drain-Source ON resistance		$R_{DS(ON)}$	$I_D = 10 \text{ mA}, V_{GS} = 4.0 \text{ V}$	—	1.5	3	Ω
			$I_D = 10 \text{ mA}, V_{GS} = 2.5 \text{ V}$	—	2.2	4	
			$I_D = 1 \text{ mA}, V_{GS} = 1.5 \text{ V}$	—	5.2	15	
Input capacitance		C_{iss}	$V_{DS} = 3 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	—	9.3	—	pF
Reverse transfer capacitance		C_{rss}		—	4.5	—	
Output capacitance		C_{oss}		—	9.8	—	
Switching time	Turn-on time	t_{on}	See Figure 2 circuit diagram. $V_{DD} \doteq 3 \text{ V}, R_L = 300 \Omega$ $V_{GS} = 0 \text{ to } 2.5 \text{ V}$	—	70	—	ns
	Turn-off time	t_{off}		—	125	—	

Figure 2 Switching Time Test Circuit & Timing Chart



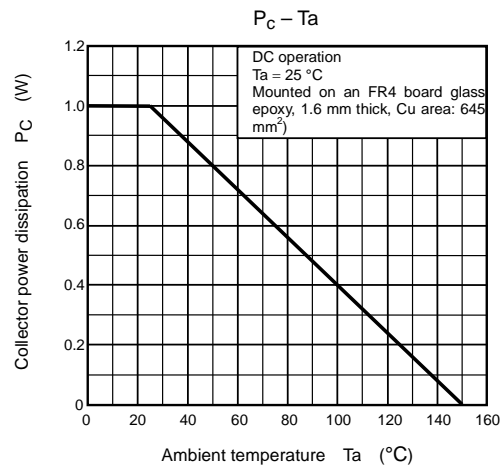
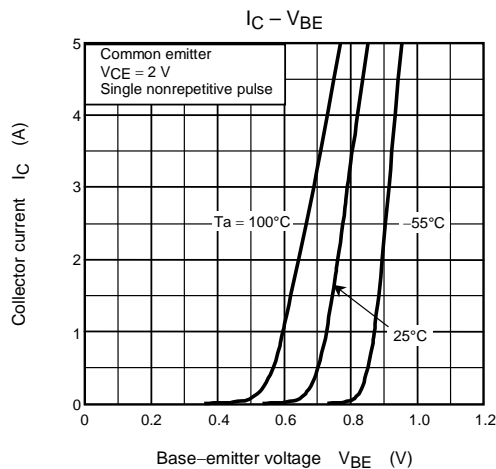
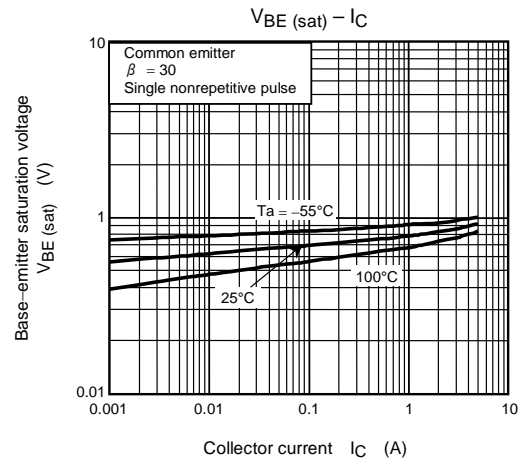
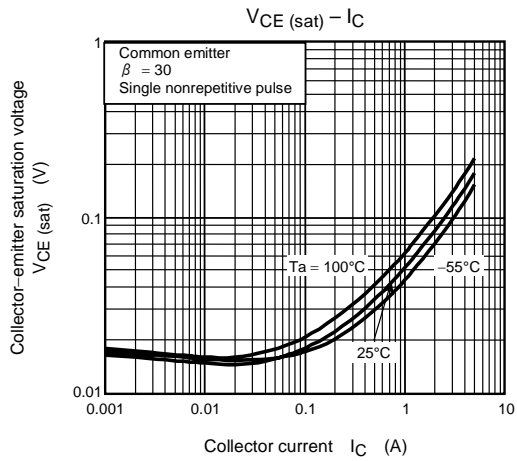
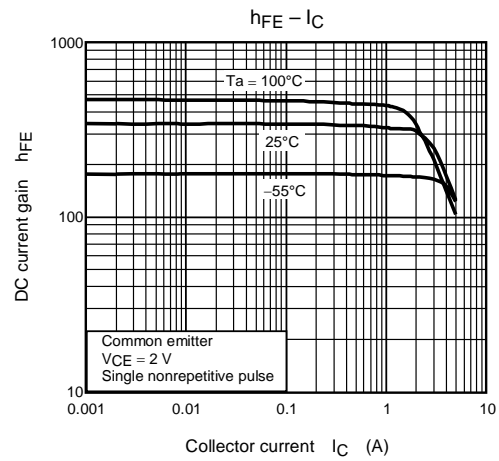
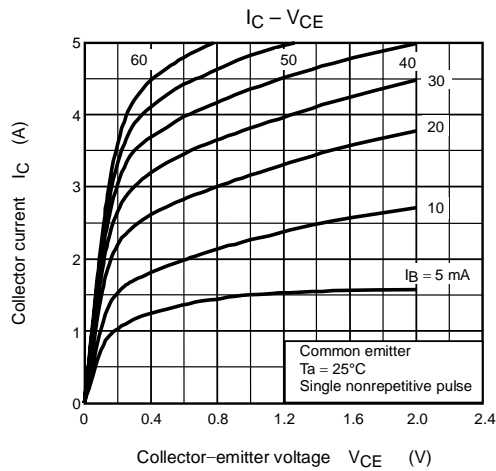
Precautions

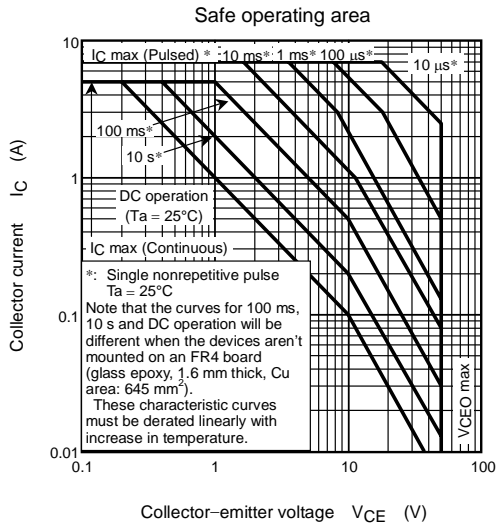
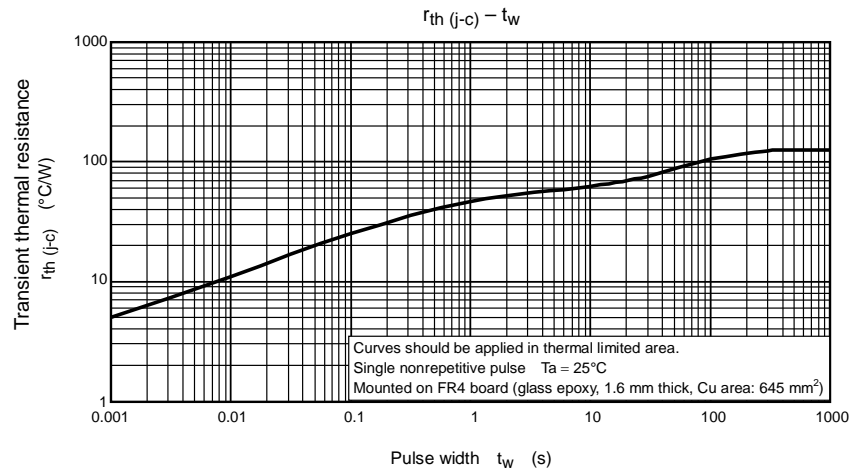
V_{th} can be expressed as the voltage between gate and source when the low operating current value is $I_D = 100 \mu\text{A}$ for this product. For normal switching operation, $V_{GS(on)}$ requires a higher voltage than V_{th} and $V_{GS(off)}$ requires a lower voltage than V_{th} .

(The relationship can be established as follows: $V_{GS(off)} < V_{th} < V_{GS(on)}$)

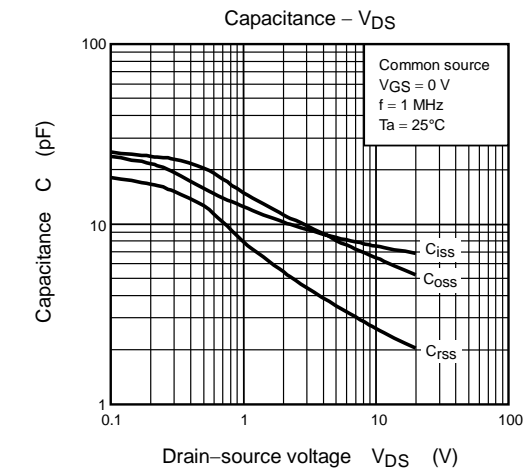
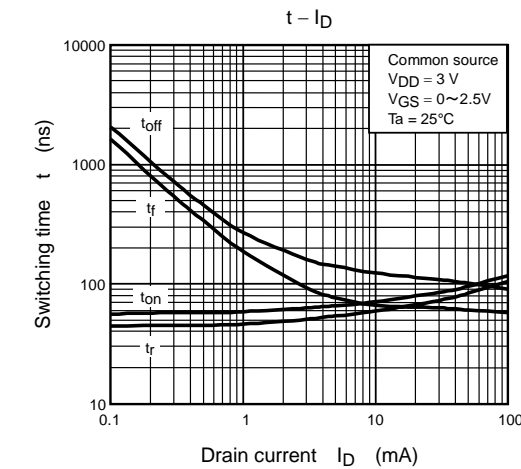
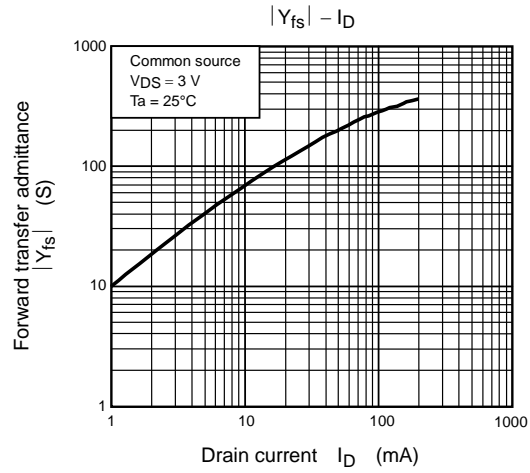
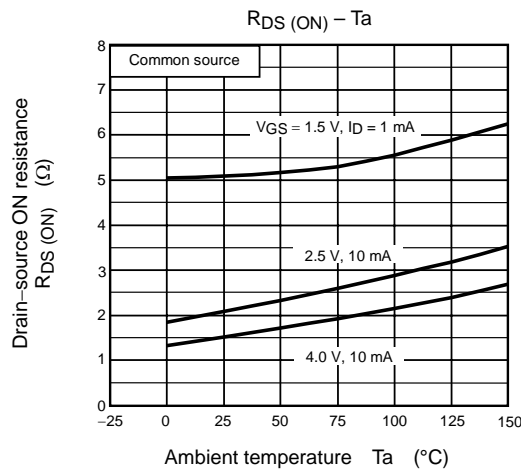
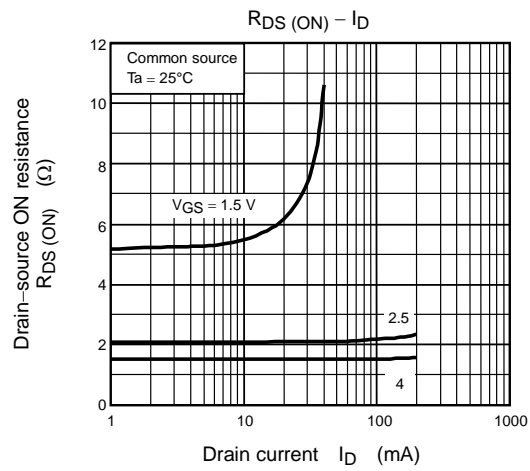
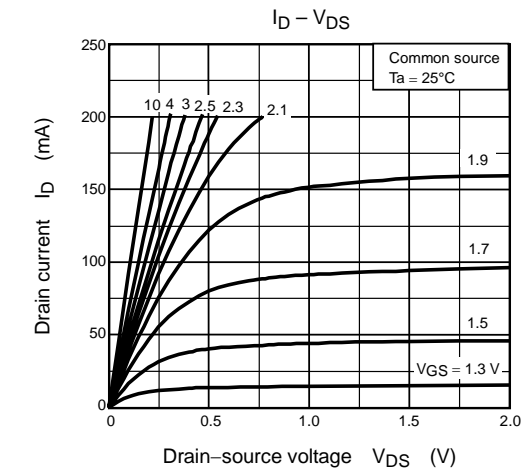
Please take this into consideration when using the device. The V_{GS} recommended voltage for turning on this product is 2.5 V or higher.

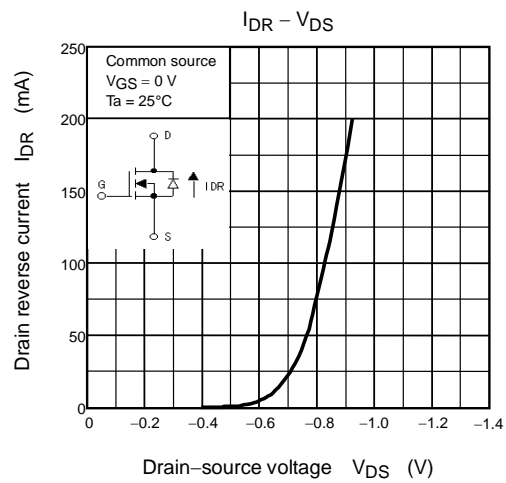
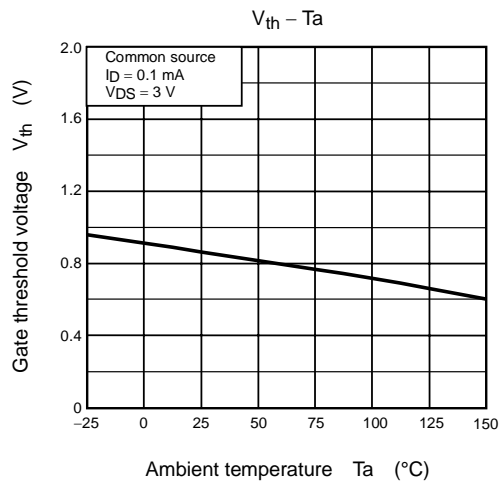
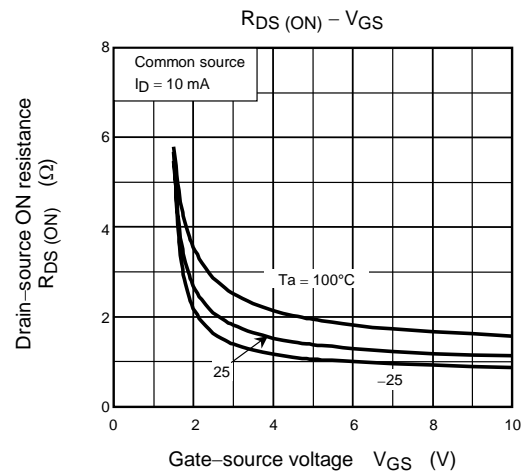
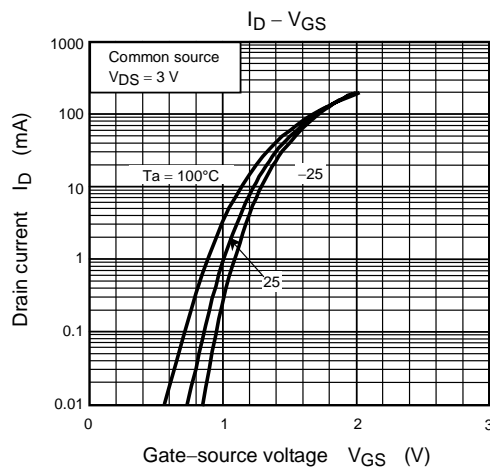
NPN





Nch-MOS





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