Am9044/AM90L44

4096x1 Static RAM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

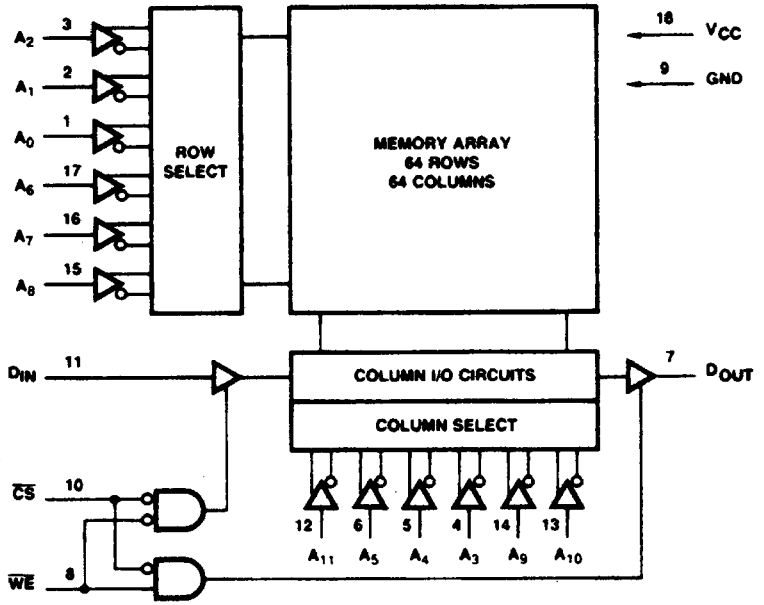
- Low operating and standby power
- Access times down to 200 ns
- Am9044 is a direct plug-in replacement for 4044
- High output drive — 4.0 mA sink current @ 0.4 V
- TTL identical interface logic levels

GENERAL DESCRIPTION

The Am9044/Am90L44 Series are high-performance, static, N-Channel, read/write, random-access memories organized as 4096 x 1. Operation is from a single 5 V supply, and all input/output levels are identical to standard TTL specifications. A Low-power version is available with power savings of about 30%.

Data readout is not destructive and the same polarity as data input. $\overline{CS}$ provides for easy selection of an individual package when the outputs are OR-tied. The outputs of 4.0 mA Am9044 provide increased short-circuit current for improved drive.

BLOCK DIAGRAM



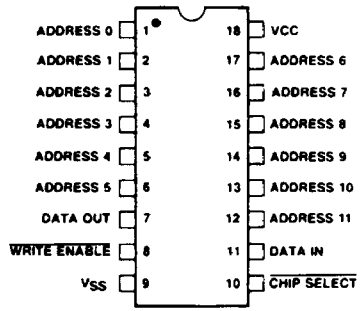
BD000091

4

PRODUCT SELECTOR GUIDE

Part Number			Am9044/Am90L44			
Speed Indicator			B	C	D	E
Maximum Access Time (ns)			450	300	250	200
0 to +70°C	I_{CC} (mA)	Standard	70	70	70	70
		Low-Power	50	50	70	–

CONNECTION DIAGRAM
Top View
DIPs

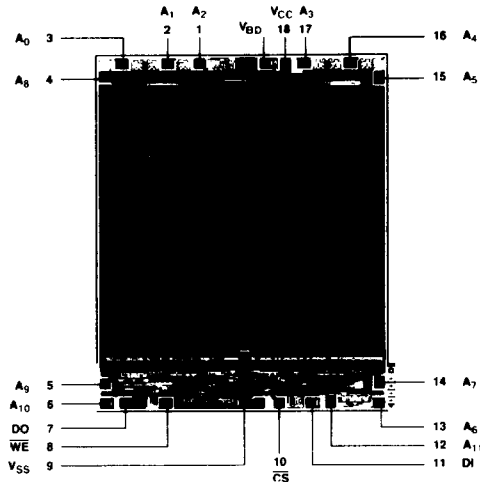


CD000142

Note: Pin 1 is marked for orientation.

METALLIZATION AND PAD LAYOUT

Address Designators	
External	Internal
A_0	A_2
A_1	A_1
A_2	A_0
A_3	A_8
A_4	A_9
A_5	A_{10}
A_6	A_3
A_7	A_4
A_8	A_5
A_9	A_7
A_{10}	A_6
A_{11}	A_{11}

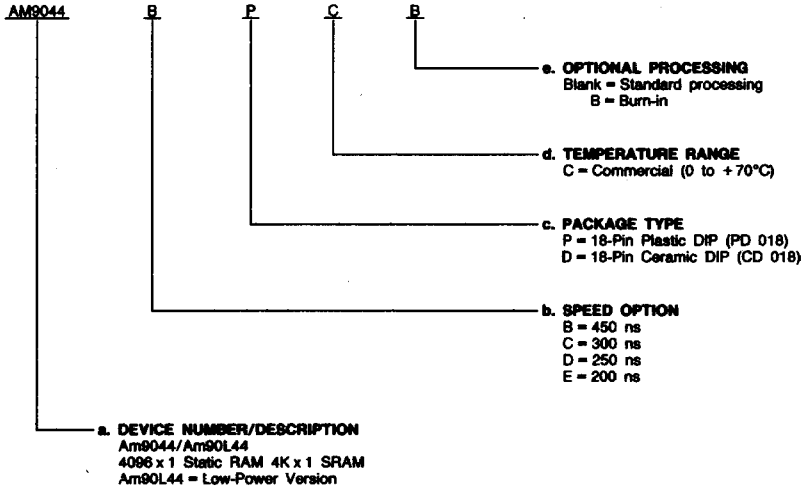


Die Size 0.137" x 0.167"

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
e. Temperature Range
e. Optional Processing



Valid Combinations	
AM9044B	PC, PCB, DC, DCB
AM90L44B	
AM9044C	
AM90L44C	
AM9044D	
AM90L44D	
AM9044E	
AM90L44E	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

$A_0 - A_{11}$ Address Inputs (Inputs)
The address input lines select the memory location from which to read or write.

$\overline{CS}$ Chip Select (Input, Active LOW)
The $\overline{CS}$ line selects the memory device for active operation.

$\overline{WE}$ Write Enable (Input, Active LOW)
When both $\overline{CS}$ and $\overline{WE}$ are LOW, data on the input lines is written to the location presented on the address input lines.

D_{IN} Data In (Input)
This pin is used to enter data during write operations.

D_{OUT} Data Out (Output, Three-State)
The content of the selected memory location is presented on the Data Output line during read operations ($\overline{CS}$ LOW, $\overline{WE}$ HIGH). The line goes three-state during write operations.

V_{CC} Power Supply

V_{SS} Ground

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... 0 to 70°C
Supply Voltage ..... −0.5 V to +7.0 V
All Signal Voltage with
Respect to Ground ..... −0.5 V to +7.0 V
Power Dissipation ..... 1.0 W
DC Output Current ..... 10 mA

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGES (Note 2)

Commercial (C) Devices
Ambient Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified (Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Unit
I_{OH}	Output HIGH Current	V_{OH} = 2.4 V V_{CC} = 4.5 V	T_A = 70°C		−1.0		mA
I_{OL}	Output LOW Current	V_{OL} = 0.4 V	T_A = 70°C		4.0		mA
V_{IH}	Input HIGH Voltage				2.0	V_{CC}	V
V_{IL}	Input LOW Voltage				−0.5	0.8	V
I_{IX}	Input Load Current	$V_{SS} \leq V_{IN} \leq V_{CC}$				10	μA
I_{OZ}	Output Leakage Current	0.4 V ≤ V_O ≤ V_{CC}, Output Disabled	T_A = +70°C		−50	50	μA
I_{CC}	Operating Supply Current	V_{CC} = Max. $\overline{CS} \leq V_{IL}$	T_A = 0°C	Standard Devices		70	mA
				Devices		50	
C_I	Input Capacitance (Note 6)	Test Frequency = 1.0 MHz T_A = 25°C, All pins at 0 V				7.0	pF
C_O	Output Capacitance (Note 6)					7.0	

Notes: 1. Absolute Maximum Ratings are intended for user guidelines and are not tested.
2. For test and correlation purposes, ambient temperature is defined as the "instant-on" case temperature.
3. Test conditions assume signal transition time of 10 ns or less, timing reference levels of 1.5 V, and output loading of the specified I_{OL}/I_{OH} plus 100 pF or 5 pF for T_{CX}, T_{OTD}, T_{OTW} and T_{WO}.
4. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
5. The specified address access time will be valid only when $\overline{CS}$ is LOW soon enough for t_{CO} to elapse.
6. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.
7. Transition is measured from 1.5 V on the input to (V_{OH} − 500 mV) and (V_{OL} + 500 mV) on the output using C_L = 5 pF.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted) (Notes 3 – 6)

No.	Parameter Symbol	Parameter Description	B Devices		C Devices		D Devices		E Devices		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE											
1	t_{RC}	Address Valid to Address Do Not Care Time (Read Cycle Time)	450		300		250		200		
2	t_A	Address Valid to Data Out Valid Delay (Address Access Time)		450		300		250		200	
3	t_{CO}	Chip Select LOW to Data Out Valid (Note 5)		100		100		70		70	
4	t_{CX}	Chip Select LOW to Data Out On (Note 6, 7)	10		10		10		10		
5	t_{OTD}	Chip Select HIGH to Data Out Off (Note 6, 7)		100		80		60		60	
6	t_{OHA}	Output hold time after address change	20		20		20		20		
WRITE CYCLE											
7	t_{WC}	Address Valid to Address Do Not Care Time (Write Cycle Time)	450		300		250		200		
8	t_W	Write Enable LOW to Write Enable HIGH Time (Note 4)	200		150		100		100		
9	t_{WR}	Write Enable HIGH to Address Do Not Care Time	0		0		0		0		
10	t_{OTW}	Write Enable LOW to Data Out Off Delay (Note 6, 7)		100		80		60		60	
11	t_{DW}	Data In Valid to Write Enable HIGH Time	200		150		100		100		
12	t_{DH}	Write Enable HIGH to Data In Do Not Care Time	0		0		0		0		ns
13	t_{AW}	Address Valid to Write Enable LOW Time	0		0		0		0		
14	t_{CW}	Chip Select LOW to Write Enable HIGH Time (Note 4)	200		150		100		100		
15	t_{WO}	Write Enable HIGH To Output Turn On (Note 6, 7)	0	100	0	100	0	70	0	70	

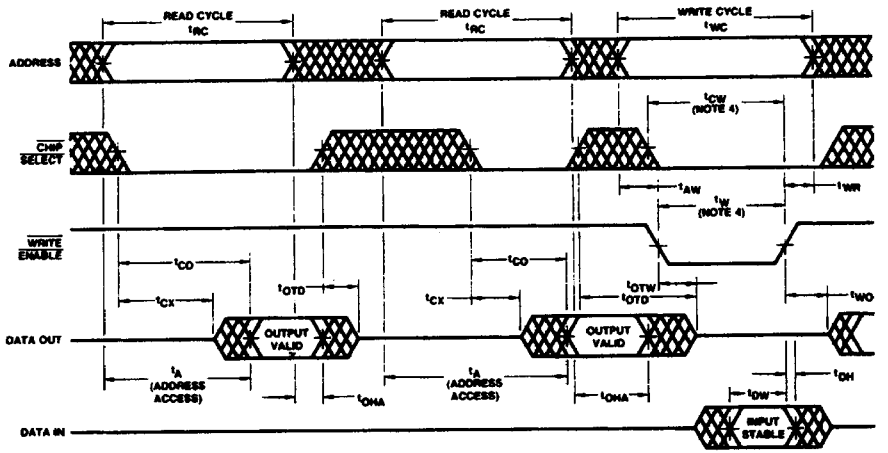
Notes: See notes following DC Characteristics table.

SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
———		
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010

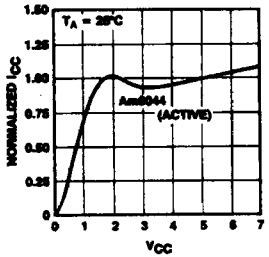


WF000191

Notes: See notes following DC Characteristics table.

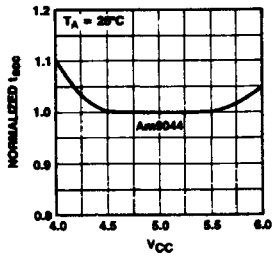
TYPICAL PERFORMANCE CURVES

Normalized Suplly Current Versus Supply Voltage



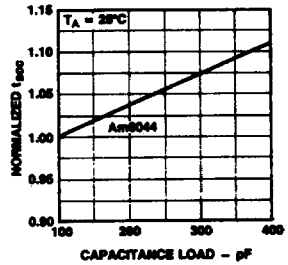
OP000892

Normalized Access Time Versus Supply Voltage



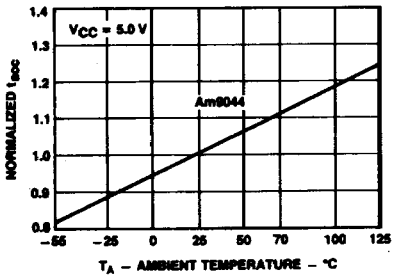
OP000902

Normalized Access Time Versus Output Loading



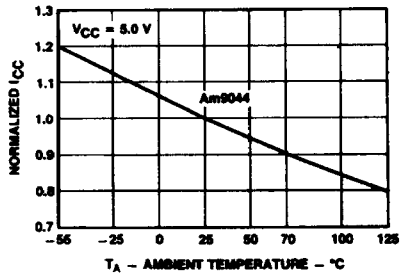
OP000912

Normalized Access Time Versus Ambient Temperature



OP000922

Normalized Supply Current Versus Ambient Temperature



OP000932

4