

# LC75818PT

## 1/8 to 1/10-Duty Dot Matrix LCD Controller & Driver with Key Input Function



**ON Semiconductor®**

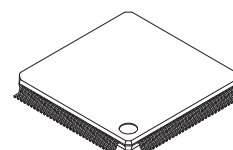
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### Overview

The LC75818PT is 1/8 to 1/10 duty dot matrix LCD display controllers/drivers that support the display of characters, numbers, and symbols. In addition to generating dot matrix LCD drive signals based on data transferred serially from a microcontroller, the LC75818PT also provide on-chip character display ROM and RAM to allow display systems to be implemented easily. These products also provide up to 4 general-purpose output ports and incorporate a key scan circuit that accepts input from up to 30 keys to reduce printed circuit board wiring.

### Features

- Key input function for up to 30 keys  
(A key scan is performed only when a key is pressed.)
- Controls and drives a 5×7, 5×8, or 5×9 dot matrix LCD.
- Supports accessory display segment drive (up to 80 segments)
- Display technique: 1/8 duty 1/4 bias drive (5×7 dots)  
1/9 duty 1/4 bias drive (5×8 dots)  
1/10 duty 1/4 bias drive (5×9 dots)
- Display digits: 16 digits×1 line (5×7 dots, 5×8 dots, 5×9 dots)
- Display control memory
  - CGROM: 240 characters (5×7, 5×8, or 5×9 dots)
  - CGRAM: 16 characters (5×7, 5×8, or 5×9 dots)
  - ADRAM: 16×5 bits
  - DCRAM: 64×8 bits
- Instruction function
  - Display on/off control
  - Display shift function
- Sleep mode can be used to reduce current drain.
- Built-in display contrast adjustment circuit
- The frame frequency of the common and segment output waveforms can be controlled by instructions.
- Serial data I/O supports CCB\* format communication with the system controller.
- Independent LCD driver block power supply  $V_{LCD}$
- A voltage detection type reset circuit is provided to initialize the IC and prevent incorrect display.
- The INH pin is provided. This pin turns off the display, disables key scanning, and forces the general-purpose output ports to the low level.
- RC oscillator circuit



TQFP120 14x14 / TQFP120

\* Computer Control Bus (CCB) is an ON Semiconductor's original bus format and the bus addresses are controlled by ON Semiconductor.

### ORDERING INFORMATION

See detailed ordering and shipping information on page 44 of this data sheet.

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## Specifications

**Absolute Maximum Ratings** at Ta = 25°C, VSS = 0 V

| Parameter                   | Symbol   | Conditions                                             | Ratings           | Unit |
|-----------------------------|----------|--------------------------------------------------------|-------------------|------|
| Maximum supply voltage      | VDD max  | VDD                                                    | −0.3 to +4.2      | V    |
|                             | VLCD max | VLCD                                                   | −0.3 to +11.0     |      |
| Input voltage               | VIN1     | CE, CL, DI, $\overline{\text{INH}}$                    | −0.3 to +4.2      | V    |
|                             |          | CE, CL, DI, $\overline{\text{INH}}$<br>VDD=2.7 to 3.6V | −0.3 to +6.5      |      |
|                             | VIN2     | OSC, KI1 to KI5, TEST                                  | −0.3 to VDD +0.3  |      |
|                             | VIN3     | VLCD1, VLCD2, VLCD3, VLCD4                             | −0.3 to VLCD +0.3 |      |
| Output voltage              | VOU1     | DO                                                     | −0.3 to +6.5      | V    |
|                             | VOU2     | OSC, KS1 to KS6, P1 to P4                              | −0.3 to VDD +0.3  |      |
|                             | VOU3     | VLCD0, S1 to S80, COM1 to COM10                        | −0.3 to VLCD +0.3 |      |
| Output current              | IOU1     | S1 to S80                                              | 300               | μA   |
|                             | IOU2     | COM1 to COM10                                          | 3                 | mA   |
|                             | IOU3     | KS1 to KS6                                             | 1                 |      |
|                             | IOU4     | P1 to P4                                               | 5                 |      |
| Allowable power dissipation | Pd max   | Ta = 85°C                                              | 200               | mW   |
| Operating temperature       | Topr     |                                                        | −40 to +85        | °C   |
| Storage temperature         | Tstg     |                                                        | −55 to +125       | °C   |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Allowable Operating Range** at Ta = −40°C to +85°C, VSS = 0 V

| Parameter                | Symbol | Conditions                                                        | Ratings       |                          |        | unit |
|--------------------------|--------|-------------------------------------------------------------------|---------------|--------------------------|--------|------|
|                          |        |                                                                   | min           | typ                      | max    |      |
| Supply voltage           | VDD    | VDD                                                               | 2.7           |                          | 3.6    | V    |
|                          | VLCD   | VLCD<br>When the display contrast adjustment circuit is used.     | 7.0           |                          | 10.0   |      |
|                          |        | VLCD<br>When the display contrast adjustment circuit is not used. | 4.5           |                          | 10.0   |      |
| Output voltage           | VLCD0  | VLCD0                                                             | VLCD4<br>+4.5 |                          | VLCD   | V    |
| Input voltage            | VLCD1  | VLCD1                                                             |               | 3/4<br>(VLCD0<br>−VLCD4) | VLCD0  | V    |
|                          | VLCD2  | VLCD2                                                             |               | 2/4<br>(VLCD0<br>−VLCD4) | VLCD0  |      |
|                          | VLCD3  | VLCD3                                                             |               | 1/4<br>(VLCD0<br>−VLCD4) | VLCD0  |      |
|                          | VLCD4  | VLCD4                                                             | 0             |                          | 1.5    |      |
| Input high level voltage | VIH1   | CE, CL, DI, $\overline{\text{INH}}$                               | 0.8VDD        |                          | 3.6    | V    |
|                          |        | CE, CL, DI, $\overline{\text{INH}}$<br>VDD = 2.7 to 3.6 V         | 0.8VDD        |                          | 5.5    |      |
|                          | VIH2   | OSC external clock operating mode                                 | 0.8VDD        |                          | VDD    |      |
|                          | VIH3   | KI1 to KI5                                                        | 0.6VDD        |                          | VDD    |      |
| Input low level voltage  | VIL1   | CE, CL, DI, $\overline{\text{INH}}$ , KI1 to KI5                  | 0             |                          | 0.2VDD | V    |
|                          | VIL2   | OSC external clock operating mode                                 | 0             |                          | 0.2VDD |      |
| Output pull-up voltage   | VOUP   | DO                                                                | 0             |                          | 5.5    | V    |

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| Parameter                                         | Symbol          | Conditions                                                                     | Ratings |     |     | unit       |
|---------------------------------------------------|-----------------|--------------------------------------------------------------------------------|---------|-----|-----|------------|
|                                                   |                 |                                                                                | min     | typ | max |            |
| Recommended external resistor for RC oscillation  | Rosc            | OSC RC oscillator operating mode                                               |         | 10  |     | k $\Omega$ |
| Recommended external capacitor for RC oscillation | Cosc            | OSC RC oscillator operating mode                                               |         | 470 |     | pF         |
| Guaranteed range of RC oscillation                | fosc            | OSC RC oscillator operating mode                                               | 150     | 300 | 600 | kHz        |
| External clock operating frequency                | f <sub>CK</sub> | OSC external clock operating mode [Figure 4]                                   | 100     | 300 | 600 | kHz        |
| External clock duty cycle                         | DCK             | OSC external clock operating mode [Figure 4]                                   | 30      | 50  | 70  | %          |
| Data setup time                                   | tds             | CL, DI [Figure 2],[Figure 3]                                                   | 160     |     |     | ns         |
| Data hold time                                    | tdh             | CL, DI [Figure 2],[Figure 3]                                                   | 160     |     |     | ns         |
| CE wait time                                      | tcp             | CE, CL [Figure 2],[Figure 3]                                                   | 160     |     |     | ns         |
| CE setup time                                     | tcs             | CE, CL [Figure 2],[Figure 3]                                                   | 160     |     |     | ns         |
| CE hold time                                      | tch             | CE, CL [Figure 2],[Figure 3]                                                   | 160     |     |     | ns         |
| High level clock pulse width                      | t $\phi$ H      | CL [Figure 2],[Figure 3]                                                       | 160     |     |     | ns         |
| Low level clock pulse width                       | t $\phi$ L      | CL [Figure 2],[Figure 3]                                                       | 160     |     |     | ns         |
| DO output delay time                              | tdc             | DO R <sub>PU</sub> =4.7k $\Omega$ C <sub>L</sub> =10pF *1[Figure 2],[Figure 3] |         |     | 1.5 | $\mu$ s    |
| DO rise time                                      | tdr             | DO R <sub>PU</sub> =4.7k $\Omega$ C <sub>L</sub> =10pF *1[Figure 2],[Figure 3] |         |     | 1.5 | $\mu$ s    |

Note: \*1. Since the DO pin is an open-drain output, these times depend on the values of the pull-up resistor R<sub>PU</sub> and the load capacitance C<sub>L</sub>.

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## Electrical Characteristics for the Allowable Operating Ranges

| Parameter                    | Symbol            | Pins                                             | Conditions                                                     | Ratings                   |                         |                           | unit       |
|------------------------------|-------------------|--------------------------------------------------|----------------------------------------------------------------|---------------------------|-------------------------|---------------------------|------------|
|                              |                   |                                                  |                                                                | min                       | typ                     | max                       |            |
| Hysteresis                   | V <sub>H</sub>    | CE, CL, DI, $\overline{\text{INH}}$ , KI1 to KI5 |                                                                |                           | 0.1V <sub>DD</sub>      |                           | V          |
| Power-down detection voltage | V <sub>DET</sub>  |                                                  |                                                                | 2.0                       | 2.2                     | 2.4                       | V          |
| Input high level current     | I <sub>IH1</sub>  | CE, CL, DI, $\overline{\text{INH}}$              | V <sub>I</sub> = 3.6 V                                         |                           |                         | 5.0                       | $\mu$ A    |
|                              |                   |                                                  | V <sub>I</sub> = 5.5 V<br>V <sub>DD</sub> = 2.7 to 3.6 V       |                           |                         | 5.0                       |            |
|                              | I <sub>IH2</sub>  | OSC                                              | V <sub>I</sub> = V <sub>DD</sub> external clock operating mode |                           |                         | 5.0                       |            |
| Input low level current      | I <sub>IL1</sub>  | CE, CL, DI, $\overline{\text{INH}}$              | V <sub>I</sub> = 0 V                                           | -5.0                      |                         |                           | $\mu$ A    |
|                              | I <sub>IL2</sub>  | OSC                                              | V <sub>I</sub> = 0 V external clock operating mode             | -5.0                      |                         |                           |            |
| Input floating voltage       | V <sub>IF</sub>   | KI1 to KI5                                       |                                                                |                           |                         | 0.05V <sub>DD</sub>       | V          |
| Pull-down resistance         | R <sub>PD</sub>   | KI1 to KI5                                       | V <sub>DD</sub> = 3.3 V                                        | 50                        | 100                     | 250                       | k $\Omega$ |
| Output off leakage current   | I <sub>OFFH</sub> | DO                                               | V <sub>O</sub> = 5.5 V                                         |                           |                         | 6.0                       | $\mu$ A    |
| Output high level voltage    | V <sub>OH1</sub>  | S1 to S80                                        | I <sub>O</sub> = -20 $\mu$ A                                   | V <sub>LCD0</sub><br>-0.6 |                         |                           | V          |
|                              | V <sub>OH2</sub>  | COM1 to COM10                                    | I <sub>O</sub> = -100 $\mu$ A                                  | V <sub>LCD0</sub><br>-0.6 |                         |                           |            |
|                              | V <sub>OH3</sub>  | KS1 to KS6                                       | I <sub>O</sub> = -250 $\mu$ A                                  | V <sub>DD</sub><br>-0.8   | V <sub>DD</sub><br>-0.4 | V <sub>DD</sub><br>-0.1   |            |
|                              | V <sub>OH4</sub>  | P1 to P4                                         | I <sub>O</sub> = -1 mA                                         | V <sub>DD</sub><br>-0.9   |                         |                           |            |
| Output low level voltage     | V <sub>OL1</sub>  | S1 to S80                                        | I <sub>O</sub> = 20 $\mu$ A                                    |                           |                         | V <sub>LCD4</sub><br>+0.6 | V          |
|                              | V <sub>OL2</sub>  | COM1 to COM10                                    | I <sub>O</sub> = 100 $\mu$ A                                   |                           |                         | V <sub>LCD4</sub><br>+0.6 |            |
|                              | V <sub>OL3</sub>  | KS1 to KS6                                       | I <sub>O</sub> = 12.5 $\mu$ A                                  | 0.1                       | 0.4                     | 1.2                       |            |
|                              | V <sub>OL4</sub>  | P1 to P4                                         | I <sub>O</sub> = 1 mA                                          |                           |                         | 0.9                       |            |
|                              | V <sub>OL5</sub>  | DO                                               | I <sub>O</sub> = 1 mA                                          |                           | 0.1                     | 0.3                       |            |

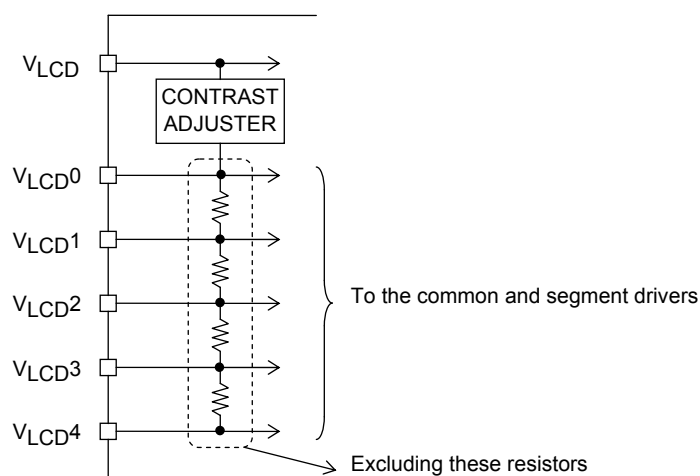
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| Parameter                      | Symbol            | Pins             | Conditions                                                                                                              | Ratings                                                   |     |                                                           | unit |
|--------------------------------|-------------------|------------------|-------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------|-----|-----------------------------------------------------------|------|
|                                |                   |                  |                                                                                                                         | min                                                       | typ | max                                                       |      |
| Output middle level voltage *2 | V <sub>MID1</sub> | S1 to S80        | I <sub>O</sub> = ±20 µA                                                                                                 | 2/4<br>(V <sub>LCD0</sub><br>-V <sub>LCD4</sub> )<br>-0.6 |     | 2/4<br>(V <sub>LCD0</sub><br>-V <sub>LCD4</sub> )<br>+0.6 | V    |
|                                | V <sub>MID2</sub> | COM1 to COM10    | I <sub>O</sub> = ±100 µA                                                                                                | 3/4<br>(V <sub>LCD0</sub><br>-V <sub>LCD4</sub> )<br>-0.6 |     | 3/4<br>(V <sub>LCD0</sub><br>-V <sub>LCD4</sub> )<br>+0.6 |      |
|                                | V <sub>MID3</sub> | COM1 to COM10    | I <sub>O</sub> = ±100 µA                                                                                                | 1/4<br>(V <sub>LCD0</sub><br>-V <sub>LCD4</sub> )<br>-0.6 |     | 1/4<br>(V <sub>LCD0</sub><br>-V <sub>LCD4</sub> )<br>+0.6 |      |
| Oscillator frequency           | fosc              | OSC              | Rosc = 10 kΩ<br>Cosc = 470 pF                                                                                           | 210                                                       | 300 | 390                                                       | kHz  |
| Current drain                  | I <sub>DD1</sub>  | V <sub>DD</sub>  | sleep mode                                                                                                              |                                                           |     | 100                                                       | µA   |
|                                | I <sub>DD2</sub>  | V <sub>DD</sub>  | V <sub>DD</sub> = 3.6 V<br>output open<br>fosc = 300 kHz                                                                |                                                           | 500 | 1000                                                      |      |
|                                | I <sub>LCD1</sub> | V <sub>LCD</sub> | sleep mode                                                                                                              |                                                           |     | 15                                                        |      |
|                                | I <sub>LCD2</sub> | V <sub>LCD</sub> | V <sub>LCD</sub> = 10.0 V<br>output open<br>fosc = 300 kHz<br>When the display contrast adjustment circuit is used.     |                                                           | 450 | 900                                                       |      |
|                                | I <sub>LCD3</sub> | V <sub>LCD</sub> | V <sub>LCD</sub> = 10.0 V<br>output open<br>fosc = 300 kHz<br>When the display contrast adjustment circuit is not used. |                                                           | 200 | 400                                                       |      |

Note: \*2. Excluding the bias voltage generation divider resistor built into the V<sub>LCD0</sub>, V<sub>LCD1</sub>, V<sub>LCD2</sub>, V<sub>LCD3</sub>, and V<sub>LCD4</sub>. (See Figure 1.)

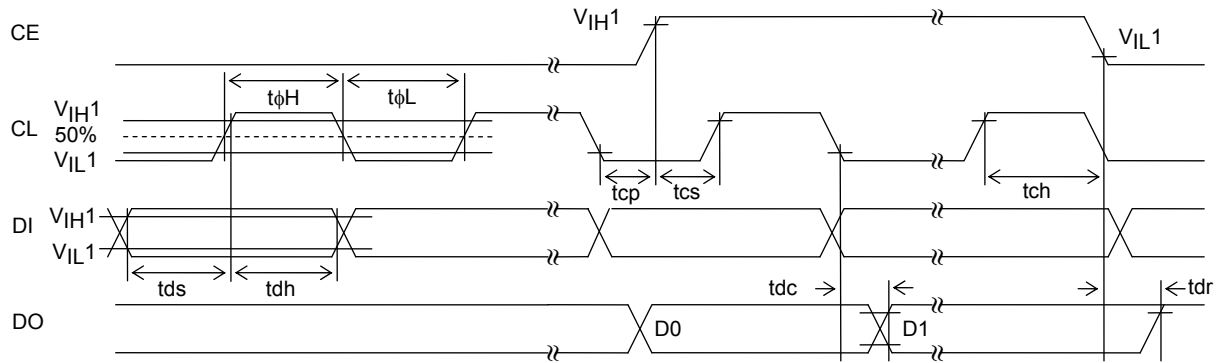


[Figure 1]

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

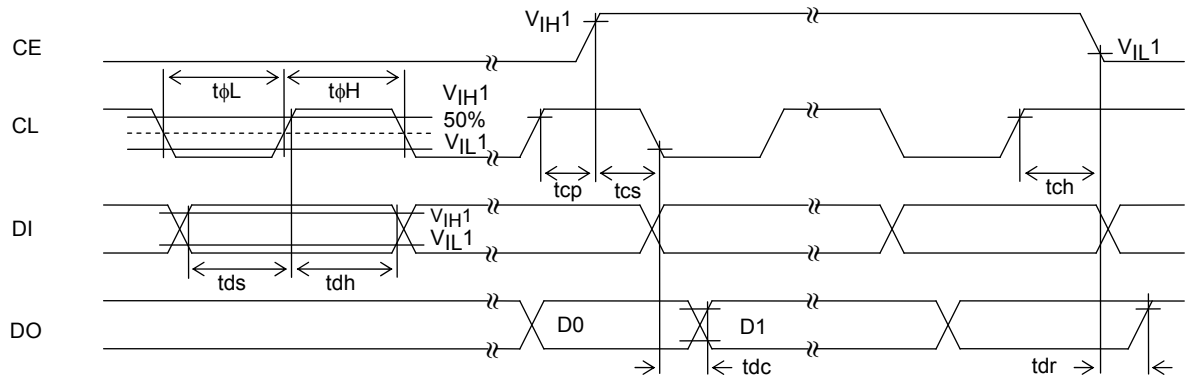
## LC75818PT

(1) When CL is stopped at the low level



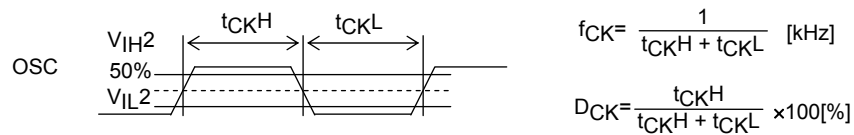
[Figure 2]

(2) When CL is stopped at the high level



[Figure 3]

(3) OSC pin clock timing in external clock operating mode



$$f_{CK} = \frac{1}{t_{CKH} + t_{CKL}} \text{ [kHz]}$$

$$D_{CK} = \frac{t_{CKH}}{t_{CKH} + t_{CKL}} \times 100\%$$

[Figure 4]

**LC75818PT**

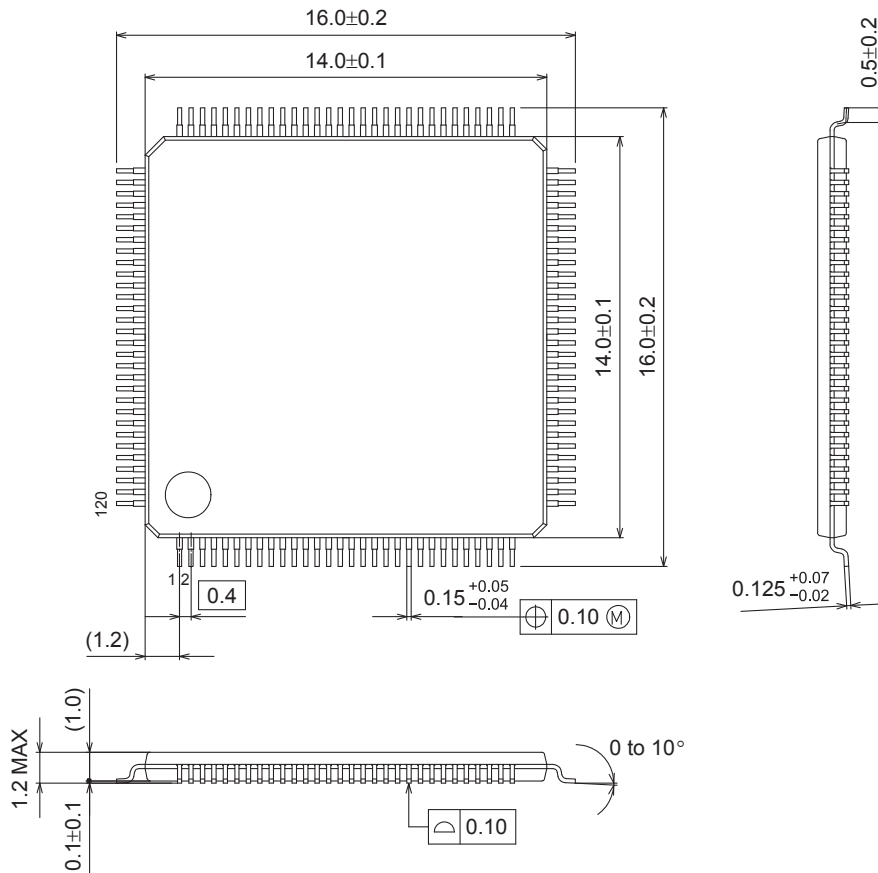
## Package Dimensions

unit : mm

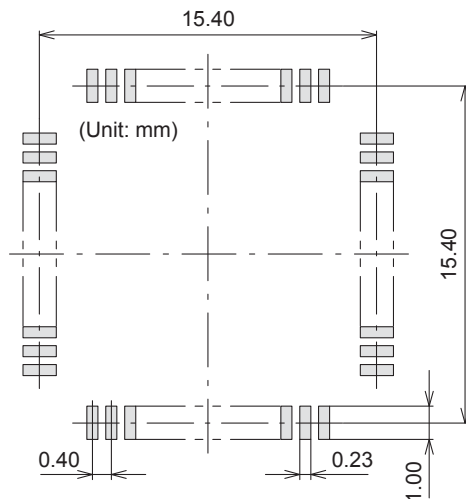
## TQFP120 14x14 / TQFP120

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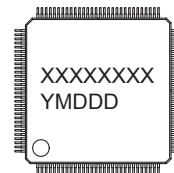
ISSUE A



### SOLDERING FOOTPRINT\*



### GENERIC MARKING DIAGRAM\*



XXXXX = Specific Device Code

Y = Year

M = Month

DDD = Additional Traceability Data

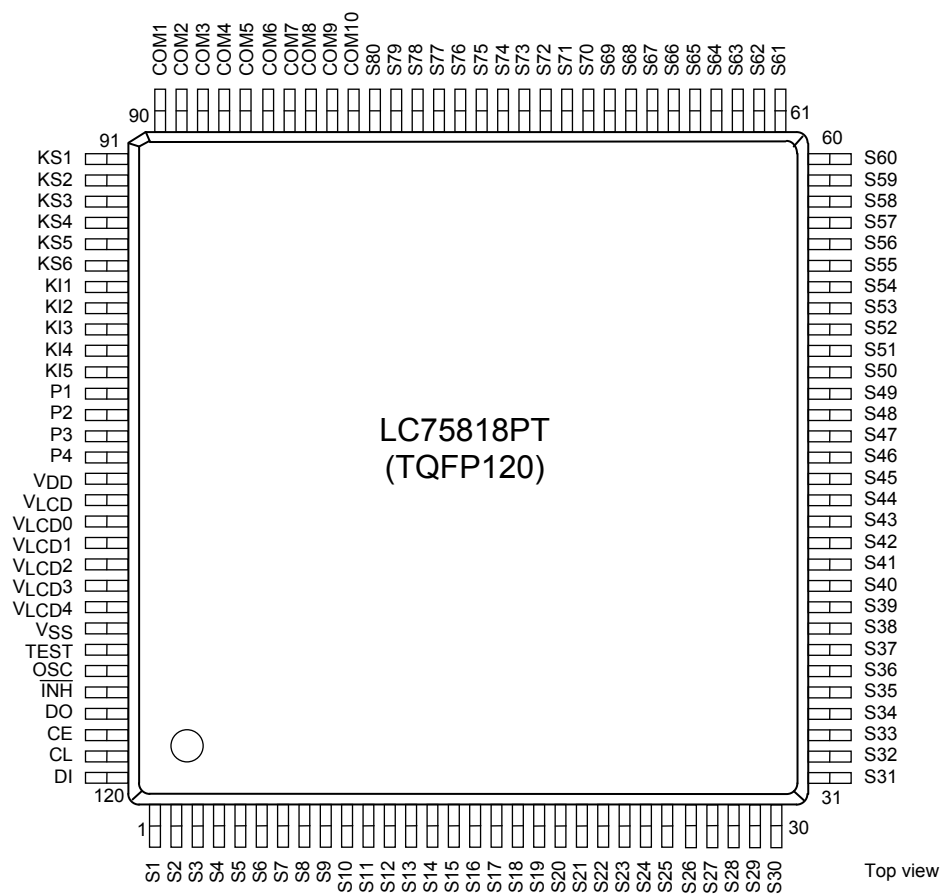
\*This information is generic. Please refer to device data sheet for actual part marking.  
Pb-Free indicator, "G" or microdot "■", may or may not be present.

NOTE: The measurements are not to guarantee but for reference only.

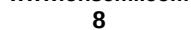
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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Pin Assignments



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## Pin Functions

| Pin                     | Pin No.    | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | Active                                                                              | I/O | Handling when unused |
|-------------------------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-----|----------------------|
| S1 to S80               | 1 to 80    | Segment driver outputs.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | -                                                                                   | O   | OPEN                 |
| COM1 to COM10           | 90 to 81   | Common driver outputs.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | -                                                                                   | O   | OPEN                 |
| KS1 to KS6              | 91 to 96   | Key scan outputs. Although normal key scan timing lines require diodes to be inserted in the timing lines to prevent shorts, since these outputs are unbalanced CMOS transistor outputs, these outputs will not be damaged by shorting when these outputs are used to form a key matrix.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | -                                                                                   | O   | OPEN                 |
| KI1 to KI5              | 97 to 101  | Key scan inputs.<br>These pins have built-in pull-down resistors.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | H                                                                                   | I   | GND                  |
| P1 to P4                | 102 to 105 | General-purpose outputs. P4 can be used as a clock output port with the "set key scan output port/general-purpose output port state" instruction.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | -                                                                                   | O   | OPEN                 |
| OSC                     | 115        | Oscillator connections. An oscillator circuit is formed by connecting an external resistor and capacitor to this pin. This pin can also be used as the external clock input pin with the "set display technique" instruction.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | -                                                                                   | I/O | V <sub>DD</sub>      |
| CE                      | 118        | Serial data interface connections to the controller. Note that DO, being an open-drain output, requires a pull-up resistor.<br>CE: Chip enable<br>CL: Synchronization clock<br>DI: Transfer data<br>DO: Output data                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | H                                                                                   | I   | GND                  |
| CL                      | 119        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |  | I   |                      |
| DI                      | 120        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | -                                                                                   | I   |                      |
| DO                      | 117        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | -                                                                                   | O   | OPEN                 |
| $\overline{\text{INH}}$ | 116        | Input that turns the display off, disables key scanning, and forces the general-purpose output ports low.<br><ul style="list-style-type: none"> <li>When <math>\overline{\text{INH}}</math> is low (V<sub>SS</sub>): <ul style="list-style-type: none"> <li>Display off<br/>S1 to S80="L" (V<sub>LCD4</sub>)<br/>COM1 to COM10="L" (V<sub>LCD4</sub>)</li> <li>General-purpose output ports P1 to P4=low (V<sub>SS</sub>)</li> <li>Key scanning disabled: KS1 to KS6=low (V<sub>SS</sub>)</li> <li>All the key data is reset to low.</li> </ul> </li> <li>When <math>\overline{\text{INH}}</math> is high (V<sub>DD</sub>): <ul style="list-style-type: none"> <li>Display on</li> <li>The state of the pins as key scan output pins or general-purpose output ports can be set with the "set key scan output port/general-purpose output port state" instruction.</li> <li>Key scanning is enabled.</li> </ul> </li> </ul> However, serial data can be transferred when the $\overline{\text{INH}}$ pin is low. | L                                                                                   | I   | V <sub>DD</sub>      |
| TEST                    | 114        | This pin must be connected to ground.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | -                                                                                   | I   | -                    |
| V <sub>LCD0</sub>       | 108        | LCD drive 4/4 bias voltage (high level) supply pin. The level on this pin can be changed by the display contrast adjustment circuit. However, (V <sub>LCD0</sub> - V <sub>LCD4</sub> ) must be greater than or equal to 4.5V. Also, external power must not be applied to this pin since the pin circuit includes the display contrast adjustment circuit.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | -                                                                                   | O   | OPEN                 |
| V <sub>LCD1</sub>       | 109        | LCD drive 3/4 bias voltage (middle level) supply pin. This pin can be used to supply the 3/4 (V <sub>LCD0</sub> - V <sub>LCD4</sub> ) voltage level externally.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | -                                                                                   | I   | OPEN                 |
| V <sub>LCD2</sub>       | 110        | LCD drive 2/4 bias voltage (middle level) supply pin. This pin can be used to supply the 2/4 (V <sub>LCD0</sub> - V <sub>LCD4</sub> ) voltage level externally.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | -                                                                                   | I   | OPEN                 |

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| Pin               | Pin No. | Function                                                                                                                                                                                                                                                                                                                          | Active | I/O | Handling when unused |
|-------------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-----|----------------------|
| V <sub>LCD3</sub> | 111     | LCD drive 1/4 bias voltage (middle level) supply pin. This pin can be used to supply the 1/4 (V <sub>LCD0</sub> - V <sub>LCD4</sub> ) voltage level externally.                                                                                                                                                                   | -      | I   | OPEN                 |
| V <sub>LCD4</sub> | 112     | LCD drive 0/4 bias voltage (low level) supply pin. Fine adjustment of the display contrast can be implemented by connecting an external variable resistor to this pin. However, (V <sub>LCD0</sub> - V <sub>LCD4</sub> ) must be greater than or equal to 4.5V, and V <sub>LCD4</sub> must be in the range 0V to 1.5V, inclusive. | -      | I   | GND                  |
| V <sub>DD</sub>   | 106     | Logic block power supply connection. Provide a voltage of between 2.7 to 3.6V.                                                                                                                                                                                                                                                    | -      | -   | -                    |
| V <sub>LCD</sub>  | 107     | LCD driver block power supply connection. Provide a voltage of between 7.0 to 10.0V when the display contrast adjustment circuit is used and provide a voltage of between 4.5 to 10.0V when the circuit is not used.                                                                                                              | -      | -   | -                    |
| V <sub>SS</sub>   | 113     | Power supply connection. Connect to ground.                                                                                                                                                                                                                                                                                       | -      | -   | -                    |

### Block Functions

- AC (address counter)

AC is a counter that provides the addresses used for DCRAM and ADRAM.

The address is automatically modified internally, and the LCD display state is retained.

- DCRAM (data control RAM)

DCRAM is RAM that is used to store display data expressed as 8-bit character codes. (These character codes are converted to 5×7, 5×8, or 5×9 dot matrix character patterns using CGROM or CGRAM.) DCRAM has a capacity of 64×8 bits, and can hold 64 characters. The table below lists the correspondence between the 6-bit DCRAM address loaded into AC and the display position on the LCD panel.

- When the DCRAM address loaded into AC is 00H.

| Display digit               | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
|-----------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| DCRAM address (hexadecimal) | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F |

However, when the display shift is performed by specifying MDATA, the DCRAM address shifts as shown below.

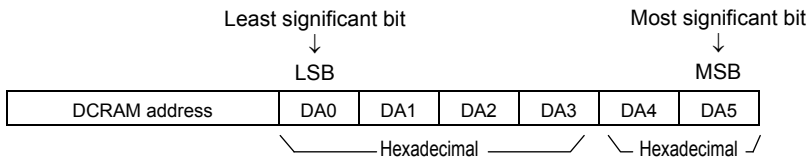
| Display digit               | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
|-----------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| DCRAM address (hexadecimal) | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F | 10 |

(shift left)

| Display digit               | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
|-----------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| DCRAM address (hexadecimal) | 3F | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E |

(shift right)

Note: \*3. The DCRAM address is expressed in hexadecimal.



Example: When the DCRAM address is 2EH.

| DA0 | DA1 | DA2 | DA3 | DA4 | DA5 |
|-----|-----|-----|-----|-----|-----|
| 0   | 1   | 1   | 1   | 0   | 1   |

## LC75818PT

- ADRAM (Additional data RAM)

ADRAM is RAM that is used to store the ADATA display data. ADRAM has a capacity of 16×5 bits, and the stored display data is displayed directly without the use of CGROM or CGRAM. The table below lists the correspondence between the 4-bit ADRAM address loaded into AC and the display position on the LCD panel.

- When the ADRAM address loaded into AC is 0H. (Number of digit displayed: 16)

|                             |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |
|-----------------------------|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|
| Display digit               | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
| ADRAM address (hexadecimal) | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9  | A  | B  | C  | D  | E  | F  |

However, when the display shift is performed by specifying ADATA, the ADRAM address shifts as shown below.

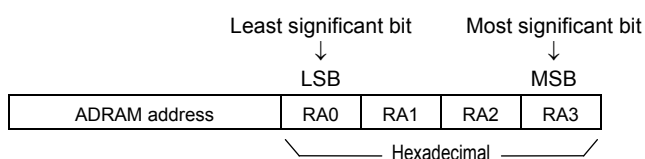
|                             |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |
|-----------------------------|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|
| Display digit               | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
| ADRAM address (hexadecimal) | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A  | B  | C  | D  | E  | F  | 0  |

(shift left)

|                             |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |
|-----------------------------|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|
| Display digit               | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
| ADRAM address (hexadecimal) | F | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8  | 9  | A  | B  | C  | D  | E  |

(shift right)

Note: \*4. The ADRAM address is expressed in hexadecimal.



Example: When the ADRAM address is AH.

|     |     |     |     |
|-----|-----|-----|-----|
| RA0 | RA1 | RA2 | RA3 |
| 0   | 1   | 0   | 1   |

- CGROM (Character generator ROM)

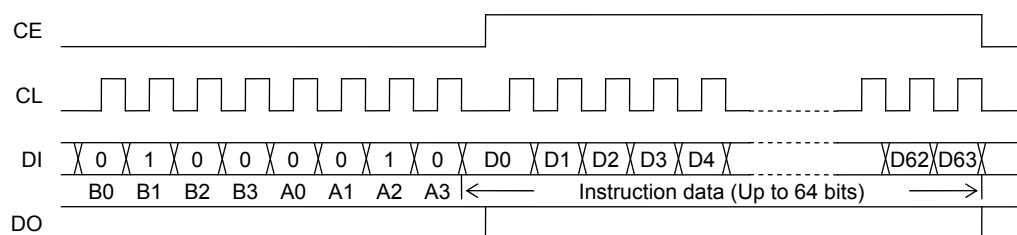
CGROM is ROM that is used to generate the 240 kinds of 5×7, 5×8, or 5×9 dot matrix character patterns from the 8-bit character codes. CGROM has a capacity of 240×45 bits. When a character code is written to DCRAM, the character pattern stored in CGROM corresponding to the character code is displayed at the position on the LCD corresponding to the DCRAM address loaded into AC.

- CGRAM (Character generator RAM)

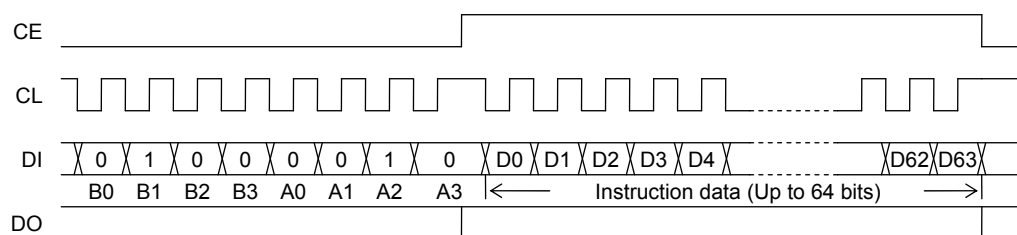
CGRAM is RAM to which user programs can freely write arbitrary character patterns. Up to 16 kinds of 5×7, 5×8, or 5×9 dot matrix character patterns can be stored. CGRAM has a capacity of 16×45 bits.

## Serial Data Input

(1) When CL is stopped at the low level



(2) When CL is stopped at the high level



- B0 to B3, A0 to A3: CCB address 42H
- D0 to D63: Instruction data

The data is acquired on the rising edge of the CL signal and latched on the falling edge of the CE signal. When transferring instruction data from the microcontroller, applications must assure that the time from the transfer of one set of instruction data until the next instruction data transfer is significantly longer than the instruction execution time.

Instruction Table

| Instruction                                                       | D0 | D1... D39 | D40 | D41 | D42 | D43 | D44 | D45 | D46 | D47 | D48 | D49 | D50 | D51 | D52 | D53 | D54 | D55 | D56 | D57 | D58 | D59 | D60 | D61 | D62 | D63 | Execution time<br>*8 |
|-------------------------------------------------------------------|----|-----------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|----------------------|
| Set display technique<br>*5                                       |    |           |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     | 0µs/108µs<br>*5      |
| Display on/off<br>control                                         |    |           |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     | 0µs/27µs<br>*9       |
| Display shift                                                     |    |           |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     | 27µs                 |
| Set AC address                                                    |    |           |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     | 27µs                 |
| DCRAM data<br>write *6                                            |    |           |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     | 27µs                 |
| ADRAM data write<br>*7                                            |    |           |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     | 27µs                 |
| CGRAM data write                                                  |    |           |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     | 27µs                 |
| Set display<br>contrast                                           |    |           |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     | 0µs                  |
| Set key scan output port/<br>general-purpose output<br>port state |    |           |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     | 0µs                  |

Notes: \*5. Be sure to execute the "set display technique" instruction first after power-on ( $V_{DET}$ -based system reset). Note that the execution time of this first instruction is 108µs ( $f_{osc}=300\text{kHz}$ ,  $f_{CK}=300\text{kHz}$ ).

\*6. The data format differs when the "DCRAM data write" instruction is executed in the increment mode ( $IM = 1$ ).

(See detailed instruction descriptions.)

\*7. The data format differs when the "ADRAM data write" instruction is executed in the increment mode ( $IM = 1$ ).

(See detailed instruction descriptions.)

\*8. The execution times listed here apply when  $f_{osc}=300\text{kHz}$ ,  $f_{CK}=300\text{kHz}$ . The execution times differ when the oscillator frequency  $f_{osc}$  or the external clock frequency  $f_{CK}$  differs.

Example: When  $f_{osc} = 210\text{kHz}$ ,  $f_{CK} = 210\text{kHz}$

$$27\mu\text{s} \times \frac{300}{210} = 39\mu\text{s}, 108\mu\text{s} \times \frac{300}{210} = 155\mu\text{s}$$

\*9. When the sleep mode ( $SP = 1$ ) is set, the execution time is 27µs (when  $f_{osc} = 300\text{kHz}$ ,  $f_{CK} = 300\text{kHz}$ ).

X: don't care

## Detailed Instruction Descriptions

- Set display technique ... <Sets the display technique>  
(Display technique)

| Code |     |     |     |     |     |     |     |
|------|-----|-----|-----|-----|-----|-----|-----|
| D56  | D57 | D58 | D59 | D60 | D61 | D62 | D63 |
| DT1  | DT2 | FC  | OC  | 0   | 0   | 0   | 1   |

Note: Be sure to execute the "set display technique" instruction first after power-on (V<sub>DET</sub>-based system reset).

X: don't care

DT1, DT2: Sets the display technique

| DT1 | DT2 | Display technique         | Output pins             |                         |
|-----|-----|---------------------------|-------------------------|-------------------------|
|     |     |                           | COM9                    | COM10                   |
| 0   | 0   | 1/8 duty, 1/4 bias drive  | V <sub>LCD4</sub> level | V <sub>LCD4</sub> level |
| 1   | 0   | 1/9 duty, 1/4 bias drive  | COM9                    | V <sub>LCD4</sub> level |
| 0   | 1   | 1/10 duty, 1/4 bias drive | COM9                    | COM10                   |

Note: \*10. COM<sub>n</sub> (n=9,10): Common output

FC: Sets the frame frequency of the common and segment output waveforms

| FC | Frame frequency                                 |                                                 |                                                   |
|----|-------------------------------------------------|-------------------------------------------------|---------------------------------------------------|
|    | 1/8 duty, 1/4 bias drive<br>f <sub>8</sub> [Hz] | 1/9 duty, 1/4 bias drive<br>f <sub>9</sub> [Hz] | 1/10 duty, 1/4 bias drive<br>f <sub>10</sub> [Hz] |
| 0  | fosc/3072, f <sub>CK</sub> /3072                | fosc/3456, f <sub>CK</sub> /3456                | fosc/3840, f <sub>CK</sub> /3840                  |
| 1  | fosc/1536, f <sub>CK</sub> /1536                | fosc/1728, f <sub>CK</sub> /1728                | fosc/1920, f <sub>CK</sub> /1920                  |

OC: Sets the RC oscillator operating mode and external clock operating mode.

| OC | OSC pin function              |
|----|-------------------------------|
| 0  | RC oscillator operating mode  |
| 1  | External clock operating mode |

Note: \*11. When selecting the RC oscillator operating mode, be sure to connect an external resistor R<sub>osc</sub> and an external capacitor C<sub>osc</sub> to the OSC pin.

- Display on/off control ... <Turns the display on or off>  
(Display ON/OFF control)

| Code |     |     |     |     |     |     |     |     |      |      |      |      |      |      |      |
|------|-----|-----|-----|-----|-----|-----|-----|-----|------|------|------|------|------|------|------|
| D40  | D41 | D42 | D43 | D44 | D45 | D46 | D47 | D48 | D49  | D50  | D51  | D52  | D53  | D54  | D55  |
| DG1  | DG2 | DG3 | DG4 | DG5 | DG6 | DG7 | DG8 | DG9 | DG10 | DG11 | DG12 | DG13 | DG14 | DG15 | DG16 |

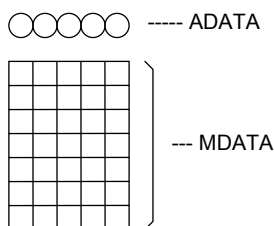
X: don't care

M, A: Specifies the data to be turned on or off

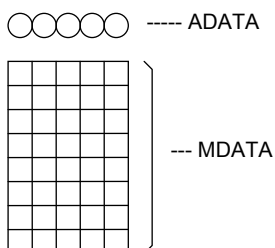
| M | A | Display operating state                                                                                                     |
|---|---|-----------------------------------------------------------------------------------------------------------------------------|
| 0 | 0 | Both MDATA and ADATA are turned off (The display is forcibly turned off regardless of the DG1 to DG16 data.)                |
| 0 | 1 | Only ADATA is turned on (The ADATA of display digits specified by the DG1 to DG16 data are turned on.)                      |
| 1 | 0 | Only MDATA is turned on (The MDATA of display digits specified by the DG1 to DG16 data are turned on.)                      |
| 1 | 1 | Both MDATA and ADATA are turned on (The MDATA and ADATA of display digits specified by the DG1 to DG16 data are turned on.) |

Note: \*12. MDATA, ADATA

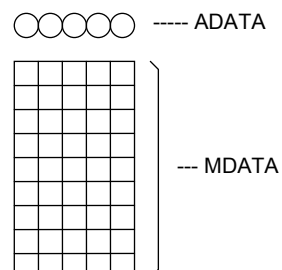
5×7 dot matrix display



5×8 dot matrix display



5×9 dot matrix display



## LC75818PT

DG1 to DG16: Specifies the display digit

| Display digit      | 1   | 2   | 3   | 4   | 5   | 6   | 7   | 8   | 9   | 10   | 11   | 12   | 13   | 14   | 15   | 16   |
|--------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|------|------|------|------|------|------|
| Display digit data | DG1 | DG2 | DG3 | DG4 | DG5 | DG6 | DG7 | DG8 | DG9 | DG10 | DG11 | DG12 | DG13 | DG14 | DG15 | DG16 |

For example, if DG1 to DG7 are 1, and DG8 to DG16 are 0, then display digits 1 to 7 will be turned on, and display digits 8 to 16 will be turned off (blanked).

SC: Controls the common and segment output pins

| SC | Common and segment output pin states             |
|----|--------------------------------------------------|
| 0  | Output of LCD drive waveforms                    |
| 1  | Fixed at the $V_{LCD4}$ level (all segments off) |

Note: \*13. When SC is 1, the S1 to S80 and COM1 to COM10 output pins are set to the  $V_{LCD4}$  level, regardless of the M, A, and DG1 to DG16 data.

SP: Controls the normal mode and sleep mode

| SP | Mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0  | Normal mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 1  | <p>Sleep mode</p> <p>(The common and segment pins go to the <math>V_{LCD4}</math> level and the oscillator on the OSC pin is stopped (although it operates during key scan operations) in RC oscillator operating mode (OC="0") and reception of the external clock is stopped (external clock is received during key scan operations) in external clock operating mode (OC="1"), to reduce current drain. Although the "display on/off control", "set display contrast" and "set key scan output port/general-purpose output port state" (disallowed to set the clock output at the P4 pin) instructions can be executed in this mode, applications must return the IC to normal mode to execute any of the other instruction setting. When the IC is in external clock operating mode, be sure to stop the external clock input after the lapse of the instruction execution time (27<math>\mu</math>s: <math>f_{CK}</math>=300kHz).</p> |

- Display shift ... <Shifts the display>  
(Display shift)

| Code |     |     |     |     |     |     |     |
|------|-----|-----|-----|-----|-----|-----|-----|
| D56  | D57 | D58 | D59 | D60 | D61 | D62 | D63 |
| M    | A   | R/L | X   | 0   | 0   | 1   | 1   |

X: don't care

M, A: Specifies the data to be shifted

| M | A | Shift operating state              |
|---|---|------------------------------------|
| 0 | 0 | Neither MDATA nor ADATA is shifted |
| 0 | 1 | Only ADATA is shifted              |
| 1 | 0 | Only MDATA is shifted              |
| 1 | 1 | Both MDATA and ADATA are shifted   |

R/L: Specifies the shift direction

| R/L | Shift direction |
|-----|-----------------|
| 0   | Shift left      |
| 1   | Shift right     |

## LC75818PT

- Set AC address... <Specifies the DCRAM and ADRAM address for AC>

(Set AC)

| Code |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| D48  | D49 | D50 | D51 | D52 | D53 | D54 | D55 | D56 | D57 | D58 | D59 | D60 | D61 | D62 | D63 |
| DA0  | DA1 | DA2 | DA3 | DA4 | DA5 | X   | X   | RA0 | RA1 | RA2 | RA3 | 0   | 1   | 0   | 0   |

X: don't care

DA0 to DA5: DCRAM address

| DA0 | DA1 | DA2 | DA3 | DA4 | DA5 |
|-----|-----|-----|-----|-----|-----|
|-----|-----|-----|-----|-----|-----|

LSB



Least significant bit

MSB



Most significant bit

RA0 to RA3: ADRAM address

| RA0 | RA1 | RA2 | RA3 |
|-----|-----|-----|-----|
|-----|-----|-----|-----|

LSB



Least significant bit

MSB



Most significant bit

This instruction loads the 6-bit DCRAM address DA0 to DA5 and the 4-bit ADRAM address RA0 to RA3 into the AC.

- DCRAM data write ... <Specifies the DCRAM address and stores data at that address>

(Write data to DCRAM)

| Code |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| D40  | D41 | D42 | D43 | D44 | D45 | D46 | D47 | D48 | D49 | D50 | D51 | D52 | D53 | D54 | D55 | D56 | D57 | D58 | D59 | D60 | D61 | D62 | D63 |
| AC0  | AC1 | AC2 | AC3 | AC4 | AC5 | AC6 | AC7 | DA0 | DA1 | DA2 | DA3 | DA4 | DA5 | X   | X   | IM  | X   | X   | X   | 0   | 1   | 0   | 1   |

X: don't care

DA0 to DA5: DCRAM address

| DA0 | DA1 | DA2 | DA3 | DA4 | DA5 |
|-----|-----|-----|-----|-----|-----|
|-----|-----|-----|-----|-----|-----|

LSB



Least significant bit

MSB



Most significant bit

AC0 to AC7: DCRAM data (character code)

| AC0 | AC1 | AC2 | AC3 | AC4 | AC5 | AC6 | AC7 |
|-----|-----|-----|-----|-----|-----|-----|-----|
|-----|-----|-----|-----|-----|-----|-----|-----|

LSB



Least significant bit

MSB



Most significant bit

This instruction writes the 8 bits of data AC0 to AC7 to DCRAM. This data is a character code, and is converted to a 5×7, 5×8, or 5×9 dot matrix display data using CGROM or CGRAM.

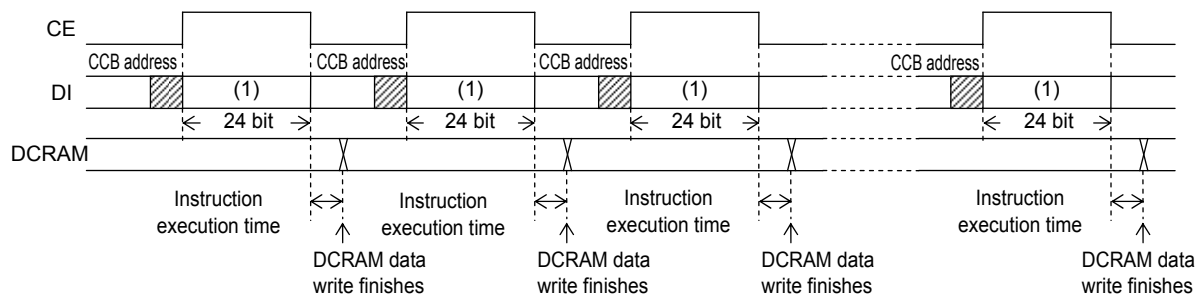
IM: Sets the method of writing data to DCRAM

| IM | DCRAM data write method                                                                                  |
|----|----------------------------------------------------------------------------------------------------------|
| 0  | Normal DCRAM data write (Specifies the DCRAM address and writes the DCRAM data.)                         |
| 1  | Increment mode DCRAM data write (Increments the DCRAM address by +1 each time data is written to DCRAM.) |

## LC75818PT

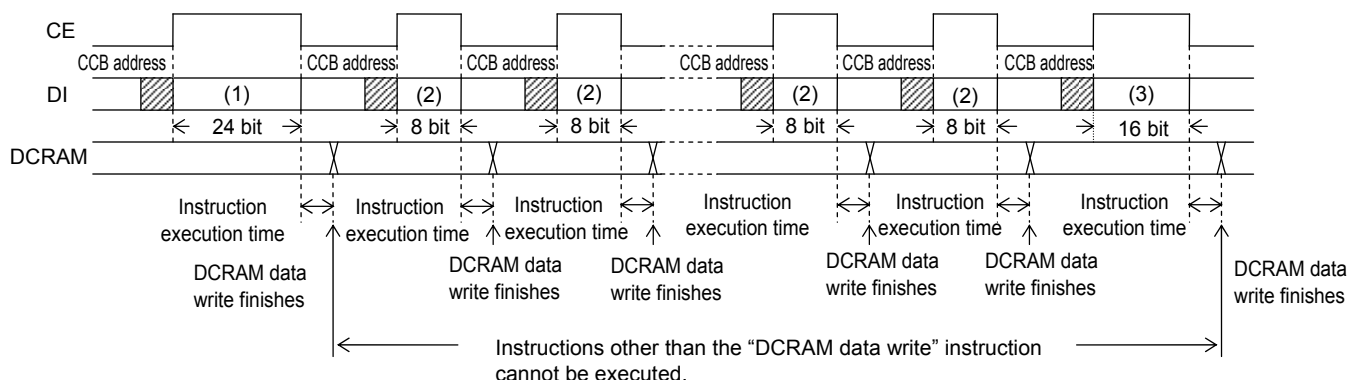
Notes: \*14.

- DCRAM data write method when IM = 0



- DCRAM data write method when IM = 1

(Instructions other than the “DCRAM data write” instruction cannot be executed.)



### Data format at (1) (24 bits)

| Code |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| D40  | D41 | D42 | D43 | D44 | D45 | D46 | D47 | D48 | D49 | D50 | D51 | D52 | D53 | D54 | D55 | D56 | D57 | D58 | D59 | D60 | D61 | D62 | D63 |
| AC0  | AC1 | AC2 | AC3 | AC4 | AC5 | AC6 | AC7 | DA0 | DA1 | DA2 | DA3 | DA4 | DA5 | X   | X   | IM  | X   | X   | X   | 0   | 1   | 0   | 1   |

X: don't care

### Data format at (2) (8 bits)

| Code |     |     |     |     |     |     |     |
|------|-----|-----|-----|-----|-----|-----|-----|
| D56  | D57 | D58 | D59 | D60 | D61 | D62 | D63 |
| AC0  | AC1 | AC2 | AC3 | AC4 | AC5 | AC6 | AC7 |

### Data format at (3) (16 bits)

| Code |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| D48  | D49 | D50 | D51 | D52 | D53 | D54 | D55 | D56 | D57 | D58 | D59 | D60 | D61 | D62 | D63 |
| AC0  | AC1 | AC2 | AC3 | AC4 | AC5 | AC6 | AC7 | 0   | X   | X   | X   | 0   | 1   | 0   | 1   |

X: don't care

- ADRAM data write ... <Specifies the ADRAM address and stores data at that address>  
(Write data to ADRAM)

| Code |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| D40  | D41 | D42 | D43 | D44 | D45 | D46 | D47 | D48 | D49 | D50 | D51 | D52 | D53 | D54 | D55 | D56 | D57 | D58 | D59 | D60 | D61 | D62 | D63 |
| AD1  | AD2 | AD3 | AD4 | AD5 | X   | X   | X   | RA0 | RA1 | RA2 | RA3 | X   | X   | X   | X   | IM  | X   | X   | X   | 0   | 1   | 1   | 0   |

X: don't care

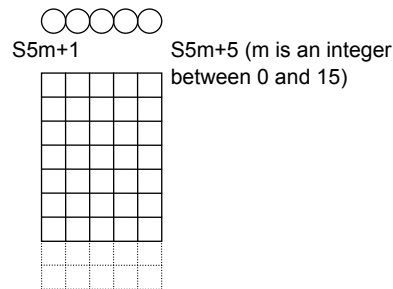
### RA0 to RA3:ADRAM address

|     |     |     |     |
|-----|-----|-----|-----|
| RA0 | RA1 | RA2 | RA3 |
|-----|-----|-----|-----|

LSB                      MSB  
↑                      ↑  
Least significant bit      Most significant bit

AD1 to AD5: ADATA display data

In addition to the 5×7, 5×8, or 5×9 dot matrix display data (MDATA), this IC supports direct display of the five accessory display segments provided in each digit as ADATA. This display function does not use CGROM or CGRAM. The figure below shows the correspondence between the data and the display. When ADn = 1 (where n is an integer between 1 and 5) the segment corresponding to that data will be turned on.



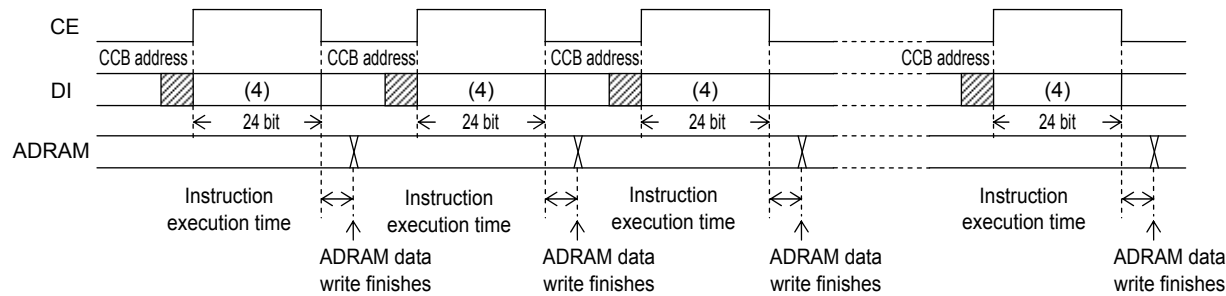
| ADATA | Corresponding output pin                 |
|-------|------------------------------------------|
| AD1   | S5m+1 (m is an integer between 0 and 15) |
| AD2   | S5m+2                                    |
| AD3   | S5m+3                                    |
| AD4   | S5m+4                                    |
| AD5   | S5m+5                                    |

IM: Sets the method of writing data to ADRAM

| IM | ADRAM data write method                                                                                  |
|----|----------------------------------------------------------------------------------------------------------|
| 0  | Normal ADRAM data write (Specifies the ADRAM address and writes the ADRAM data.)                         |
| 1  | Increment mode ADRAM data write (Increments the ADRAM address by +1 each time data is written to ADRAM.) |

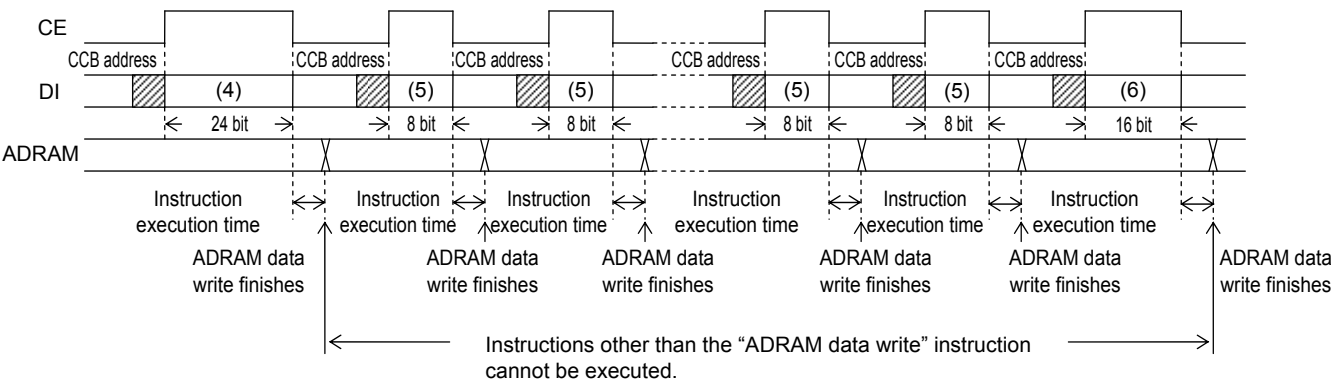
Notes: \*15.

• ADRAM data write method when IM = 0



• ADRAM data write method when IM = 1

(Instructions other than the “ADRAM data write” instruction cannot be executed.)



## LC75818PT

Data format at (4) (24 bits)

| Code |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| D40  | D41 | D42 | D43 | D44 | D45 | D46 | D47 | D48 | D49 | D50 | D51 | D52 | D53 | D54 | D55 | D56 | D57 | D58 | D59 | D60 | D61 | D62 | D63 |
| AD1  | AD2 | AD3 | AD4 | AD5 | X   | X   | X   | RA0 | RA1 | RA2 | RA3 | X   | X   | X   | X   | IM  | X   | X   | X   | 0   | 1   | 1   | 0   |

X: don't care

Data format at (5) (8 bits)

| Code |     |     |     |     |     |     |     |
|------|-----|-----|-----|-----|-----|-----|-----|
| D56  | D57 | D58 | D59 | D60 | D61 | D62 | D63 |
| AD1  | AD2 | AD3 | AD4 | AD5 | X   | X   | X   |

X: don't care

Data format at (6) (16 bits)

| Code |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| D48  | D49 | D50 | D51 | D52 | D53 | D54 | D55 | D56 | D57 | D58 | D59 | D60 | D61 | D62 | D63 |
| AD1  | AD2 | AD3 | AD4 | AD5 | X   | X   | X   | 0   | X   | X   | X   | 0   | 1   | 1   | 0   |

X: don't care

- CGRAM data write ... <Specifies the CGRAM address and stores data at that address>  
(Write data to CGRAM)

| Code |     |     |     |     |     |     |     |     |      |      |      |      |      |      |      |
|------|-----|-----|-----|-----|-----|-----|-----|-----|------|------|------|------|------|------|------|
| D0   | D1  | D2  | D3  | D4  | D5  | D6  | D7  | D8  | D9   | D10  | D11  | D12  | D13  | D14  | D15  |
| CD1  | CD2 | CD3 | CD4 | CD5 | CD6 | CD7 | CD8 | CD9 | CD10 | CD11 | CD12 | CD13 | CD14 | CD15 | CD16 |

| Code |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| D16  | D17  | D18  | D19  | D20  | D21  | D22  | D23  | D24  | D25  | D26  | D27  | D28  | D29  | D30  | D31  |
| CD17 | CD18 | CD19 | CD20 | CD21 | CD22 | CD23 | CD24 | CD25 | CD26 | CD27 | CD28 | CD29 | CD30 | CD31 | CD32 |

| Code |      |      |      |      |      |      |      |      |      |      |      |      |     |     |     |
|------|------|------|------|------|------|------|------|------|------|------|------|------|-----|-----|-----|
| D32  | D33  | D34  | D35  | D36  | D37  | D38  | D39  | D40  | D41  | D42  | D43  | D44  | D45 | D46 | D47 |
| CD33 | CD34 | CD35 | CD36 | CD37 | CD38 | CD39 | CD40 | CD41 | CD42 | CD43 | CD44 | CD45 | X   | X   | X   |

| Code |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| D48  | D49 | D50 | D51 | D52 | D53 | D54 | D55 | D56 | D57 | D58 | D59 | D60 | D61 | D62 | D63 |
| CA0  | CA1 | CA2 | CA3 | CA4 | CA5 | CA6 | CA7 | X   | X   | X   | X   | 0   | 1   | 1   | 1   |

X: don't care

CA0 to CA7: CGRAM address

|     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|
| CA0 | CA1 | CA2 | CA3 | CA4 | CA5 | CA6 | CA7 |
|-----|-----|-----|-----|-----|-----|-----|-----|

LSB



Least significant bit

MSB



Most significant bit

CD1 to CD45: CGRAM data (5×7, 5×8, or 5×9 dot matrix display data)

The bit CD<sub>n</sub> (where n is an integer between 1 and 45) corresponds to the 5×7, 5×8, or 5×9 dot matrix display data.

The figure below shows that correspondence. When CD<sub>n</sub> is 1 the dots which correspond to that data will be turned on.

|      |      |      |      |      |
|------|------|------|------|------|
| CD1  | CD2  | CD3  | CD4  | CD5  |
| CD6  | CD7  | CD8  | CD9  | CD10 |
| CD11 | CD12 | CD13 | CD14 | CD15 |
| CD16 | CD17 | CD18 | CD19 | CD20 |
| CD21 | CD22 | CD23 | CD24 | CD25 |
| CD26 | CD27 | CD28 | CD29 | CD30 |
| CD31 | CD32 | CD33 | CD34 | CD35 |
| CD36 | CD37 | CD38 | CD39 | CD40 |
| CD41 | CD42 | CD43 | CD44 | CD45 |

Note: \*16. CD1 to CD35: 5×7 dot matrix display data

CD1 to CD40: 5×8 dot matrix display data

CD1 to CD45: 5×9 dot matrix display data

## LC75818PT

- Set display contrast... <Sets the display contrast>

(Set display contrast)

| Code |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| D48  | D49 | D50 | D51 | D52 | D53 | D54 | D55 | D56 | D57 | D58 | D59 | D60 | D61 | D62 | D63 |
| CT0  | CT1 | CT2 | CT3 | X   | X   | X   | X   | CTC | X   | X   | X   | 1   | 0   | 0   | 0   |

X: don't care

CT0 to CT3: Sets the display contrast (11 steps)

| CT0 | CT1 | CT2 | CT3 | LCD drive 4/4 bias voltage supply $V_{LCD0}$ level |
|-----|-----|-----|-----|----------------------------------------------------|
| 0   | 0   | 0   | 0   | $0.94V_{LCD}=V_{LCD}-(0.03V_{LCD}\times 2)$        |
| 1   | 0   | 0   | 0   | $0.91V_{LCD}=V_{LCD}-(0.03V_{LCD}\times 3)$        |
| 0   | 1   | 0   | 0   | $0.88V_{LCD}=V_{LCD}-(0.03V_{LCD}\times 4)$        |
| 1   | 1   | 0   | 0   | $0.85V_{LCD}=V_{LCD}-(0.03V_{LCD}\times 5)$        |
| 0   | 0   | 1   | 0   | $0.82V_{LCD}=V_{LCD}-(0.03V_{LCD}\times 6)$        |
| 1   | 0   | 1   | 0   | $0.79V_{LCD}=V_{LCD}-(0.03V_{LCD}\times 7)$        |
| 0   | 1   | 1   | 0   | $0.76V_{LCD}=V_{LCD}-(0.03V_{LCD}\times 8)$        |
| 1   | 1   | 1   | 0   | $0.73V_{LCD}=V_{LCD}-(0.03V_{LCD}\times 9)$        |
| 0   | 0   | 0   | 1   | $0.70V_{LCD}=V_{LCD}-(0.03V_{LCD}\times 10)$       |
| 1   | 0   | 0   | 1   | $0.67V_{LCD}=V_{LCD}-(0.03V_{LCD}\times 11)$       |
| 0   | 1   | 0   | 1   | $0.64V_{LCD}=V_{LCD}-(0.03V_{LCD}\times 12)$       |

CTC: Sets the display contrast adjustment circuit state

| CTC | Display contrast adjustment circuit state                                                                           |
|-----|---------------------------------------------------------------------------------------------------------------------|
| 0   | The display contrast adjustment circuit is disabled, and the $V_{LCD0}$ pin level is forced to the $V_{LCD}$ level. |
| 1   | The display contrast adjustment circuit operates, and the display contrast is adjusted.                             |

Note that although the display contrast can be adjusted by operating the built-in display contrast adjustment circuit, it is also possible to apply fine adjustments to the contrast by connecting an external variable resistor to the  $V_{LCD4}$  pin and modifying the  $V_{LCD4}$  pin voltage. However, the following conditions must be met:  $V_{LCD0}-V_{LCD4}\geq 4.5V$ , and  $1.5V\geq V_{LCD4}\geq 0V$ .

- Set key scan output port/general-purpose output port state

... <Sets the key scan output port and general-purpose output port states>

(Key scan output port and General-purpose output port control)

| Code |     |     |     |     |     |      |      |     |     |     |     |     |     |     |     |
|------|-----|-----|-----|-----|-----|------|------|-----|-----|-----|-----|-----|-----|-----|-----|
| D48  | D49 | D50 | D51 | D52 | D53 | D54  | D55  | D56 | D57 | D58 | D59 | D60 | D61 | D62 | D63 |
| KC1  | KC2 | KC3 | KC4 | KC5 | KC6 | PC40 | PC41 | PC1 | PC2 | PC3 | X   | 1   | 0   | 0   | 1   |

X: don't care

KC1 to KC6: Sets the key scan output pin KS1 to KS6 state

| Output pin                         | KS1 | KS2 | KS3 | KS4 | KS5 | KS6 |
|------------------------------------|-----|-----|-----|-----|-----|-----|
| Key scan output state setting data | KC1 | KC2 | KC3 | KC4 | KC5 | KC6 |

When KC1 to KC3 are set to 1 and KC4 to KC6 are set to 0, in the key scan standby state, the KS1 to KS3 output pins will output the high level ( $V_{DD}$ ) and KS4 to KS6 will output the low level ( $V_{SS}$ ).

Note that key scan output signals are not output from output pins that are set to the low level.

PC1, PC2, PC3: Sets the general-purpose output port P1, P2, P3 state

| Output pin                                | P1  | P2  | P3  |
|-------------------------------------------|-----|-----|-----|
| General-purpose output port state setting | PC1 | PC2 | PC3 |

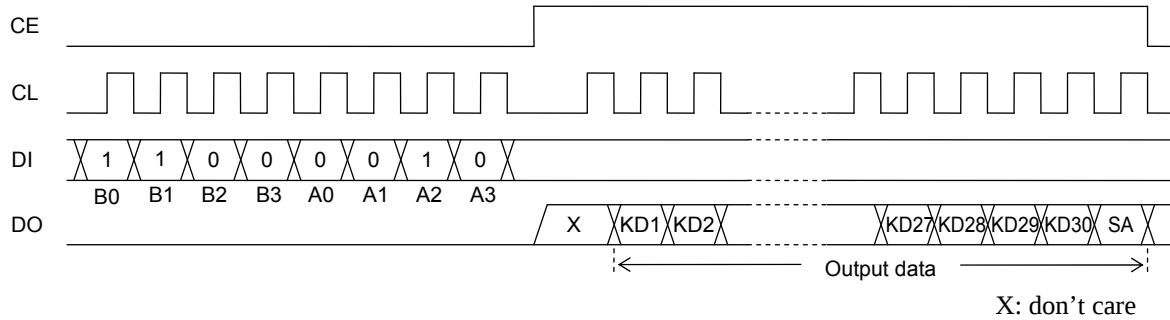
When PC1 is set to 1 and PC2 to PC3 are set to 0, P1 output pin will output the high levels ( $V_{DD}$ ) and P2 to P3 will output the low levels ( $V_{SS}$ ).

PC40, PC41: Sets the general-purpose output port P4 state

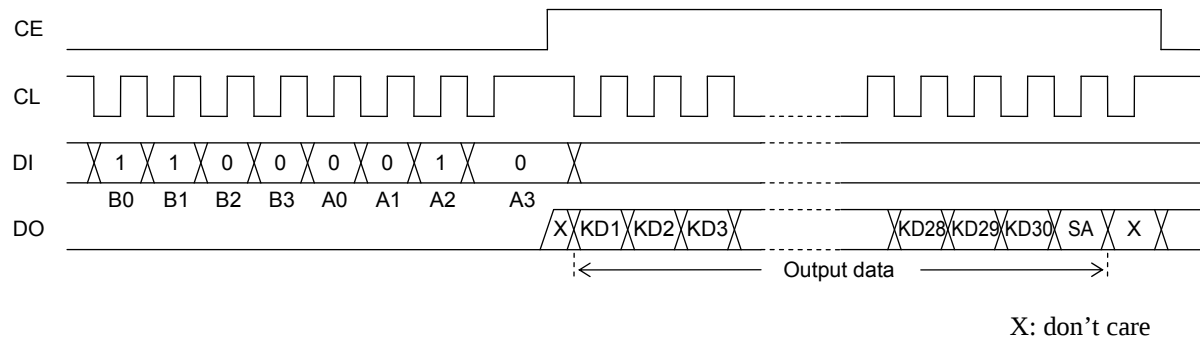
| PC40 | PC41 | Output pin (P4) state                            |
|------|------|--------------------------------------------------|
| 0    | 0    | "L"(V <sub>SS</sub> )                            |
| 1    | 0    | "H"(V <sub>DD</sub> )                            |
| 0    | 1    | Clock signal output ( $f_{osc}/2$ , $f_{CK}/2$ ) |
| 1    | 1    | Clock signal output ( $f_{osc}/8$ , $f_{CK}/8$ ) |

## Serial Data Output

(1) When CL is stopped at the low level



(2) When CL is stopped at the high level



- B0 to B3, A0 to A3: CCB address 43H
- KD1 to KD30: Key data
- SA: Sleep acknowledge data

Note: \*17. If a key data read operation is executed when DO is high, the read key data (KD1 to KD30) and sleep acknowledge data(SA) will be invalid.

## Output Data

(1) KD1 to KD30: Key data

When a key matrix of up to 30 keys is formed from the KS1 to KS6 output pins and the KI1 to KI5 input pins and one of those keys is pressed, the key output data corresponding to that key will be set to 1. The table shows the relationship between those pins and the key data bits.

|     | KI1  | KI2  | KI3  | KI4  | KI5  |
|-----|------|------|------|------|------|
| KS1 | KD1  | KD2  | KD3  | KD4  | KD5  |
| KS2 | KD6  | KD7  | KD8  | KD9  | KD10 |
| KS3 | KD11 | KD12 | KD13 | KD14 | KD15 |
| KS4 | KD16 | KD17 | KD18 | KD19 | KD20 |
| KS5 | KD21 | KD22 | KD23 | KD24 | KD25 |
| KS6 | KD26 | KD27 | KD28 | KD29 | KD30 |

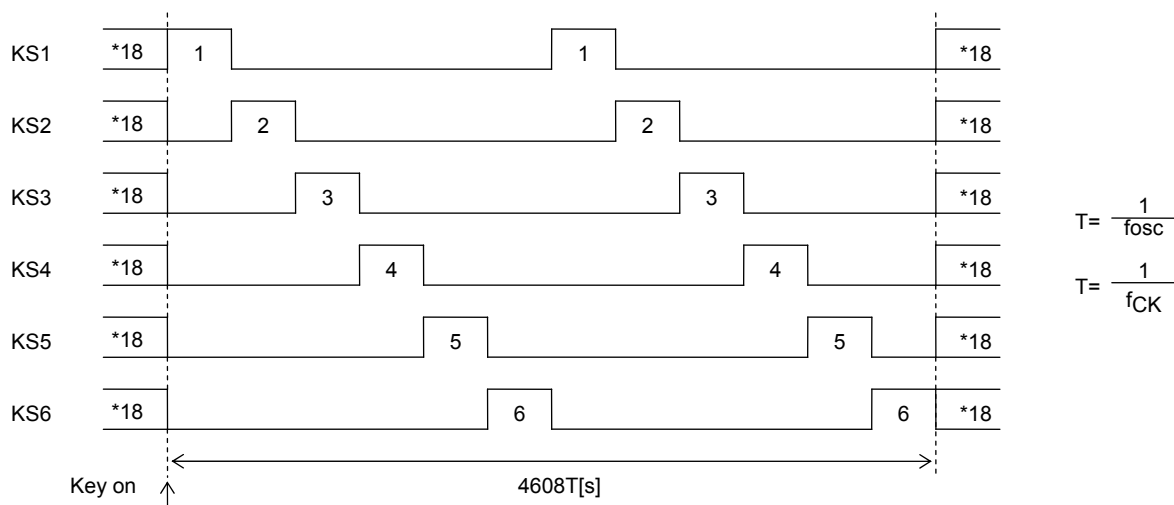
(2) SA : Sleep acknowledge data

This output data bit is set to the state when the key was pressed. Also, while DO will be low in this case, if serial data is input and the mode is set (to normal or sleep mode) during this period, that mode will be set. SA will be 1 in Sleep mode and 0 in normal mode.

## Key Scan Operation Functions

### (1) Key scan timing

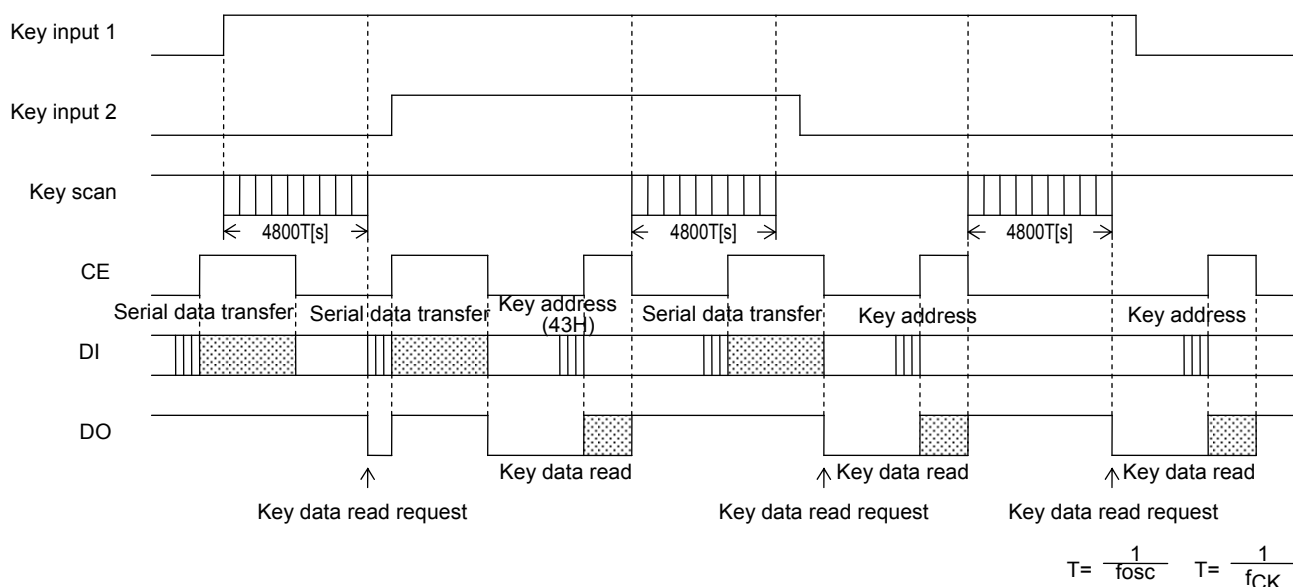
The key scan period is 2304T(s). To reliably determine the on/off state of the keys, the LC75818PT scans the keys twice and determines that a key has been pressed when the key data agrees. It outputs a key data read request (a low level on DO) 4800T(s) after starting a key scan. If the key data dose not agree and a key was pressed at that point, it scans the keys again. Thus the LC75818PT cannot detect a key press shorter than 4800T(s).



Note: \*18. Not that the high/low states of these pins are determined by the "set key scan output port/general-purpose output port state" instruction, and that key scan output signals are not output from pins that are set to low.

### (2) In normal mode

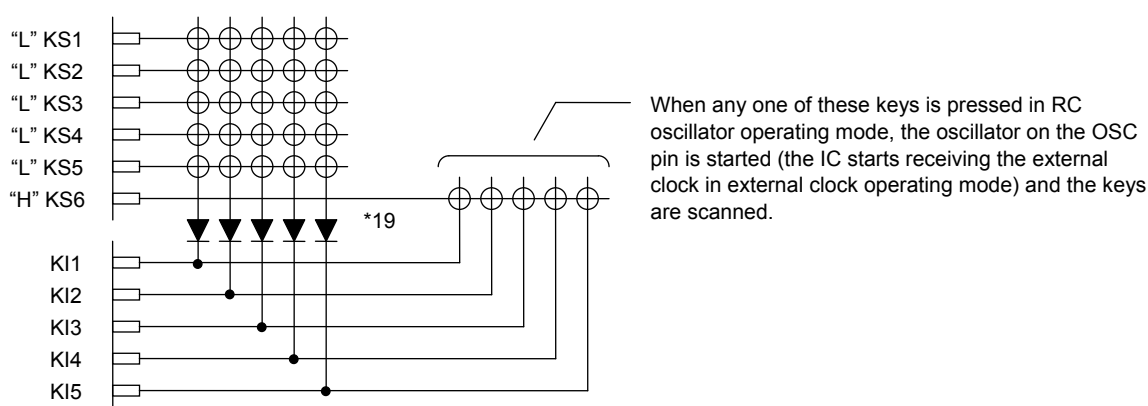
- The pins KS1 to KS6 are set to high or low with the "set key scan output port/general-purpose output port state" instruction.
- If a key on one of the lines corresponding to a KS1 to KS6 pin which is set high is pressed, a key scan is started and the keys are scanned until all keys are released. Multiple key presses are recognized by determining whether multiple key data bits are set.
- If a key is pressed for longer than 4800T(s) (Where  $T=1/f_{osc}$ ,  $T=1/f_{CK}$ ) the LC75818PT outputs a key data read request (a low level on DO) to the controller. The controller acknowledges this request and reads the key data. However, if CE is high during a serial data transfer, DO will be set high.
- After the controller reads the key data, the key data read request is cleared (DO is set high) and the LC75818PT performs another key scan. Also note that DO, being an open-drain output, requires a pull-up resistor (between 1 kΩ and 10 kΩ).



(3) In sleep mode

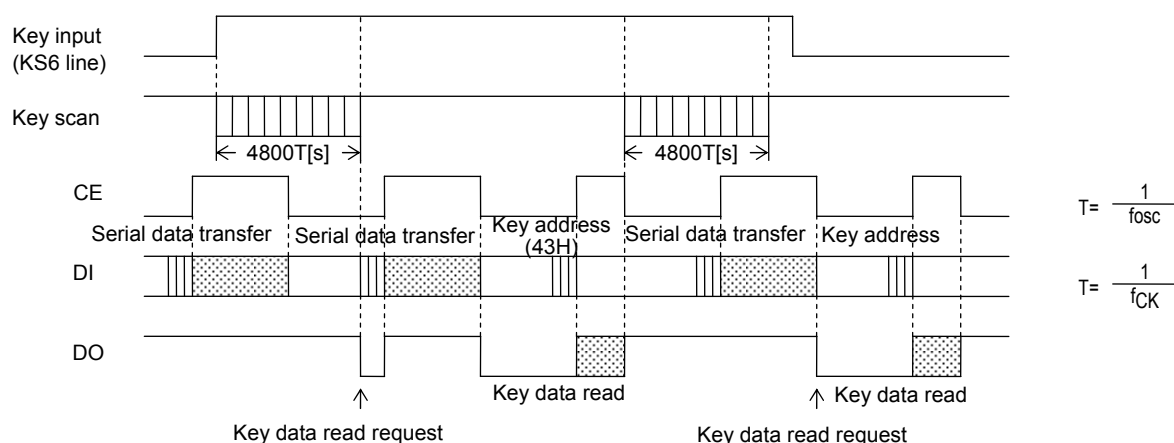
- The pins KS1 to KS6 are set to high or low with the "set key scan output port/general-purpose output port state" instruction.
- If a key on one of the lines corresponding to a KS1 to KS6 pin which is set high is pressed in the RC oscillator operating mode, the oscillator on the OSC pin is started (the IC starts receiving the external clock in external clock operating mode) and a key scan is performed. Keys are scanned until all keys released. Multiple key presses are recognized by determining whether multiple key data bits are set.
- If a key is pressed for longer than 4800T(s) (Where  $T=1/f_{osc}$ ,  $T=1/f_{CK}$ ) the LC75818PT outputs a key data read request (a low level on DO) to the controller. The controller acknowledges this request and reads the key data. However, if CE is high during a serial data transfer, DO will be set high.
- After the controller reads the key data, the key data read request is cleared (DO is set high) and the LC75818PT performs another key scan. However, this does not clear sleep mode. Also note that DO, being an open-drain output, requires a pull-up resistor (between 1 kΩ and 10 kΩ).
- Sleep mode key scan example

Example: When a "display on/off control (SP=1)" instruction and a "set key scan output port/general-purpose output port state (KC1 to KC5= 0, KC6=1)" instruction are executed. (i.e. sleep mode with only KS6 high.)



Note: \*19. These diodes are required to reliably recognize multiple key presses on the KS6 line when sleep mode state with only KS6 high, as in the above example.

That is, these diodes prevent incorrect operations due to sneak currents in the KS6 key scan output signal when keys on the KS1 to KS5 lines are pressed at the same time.



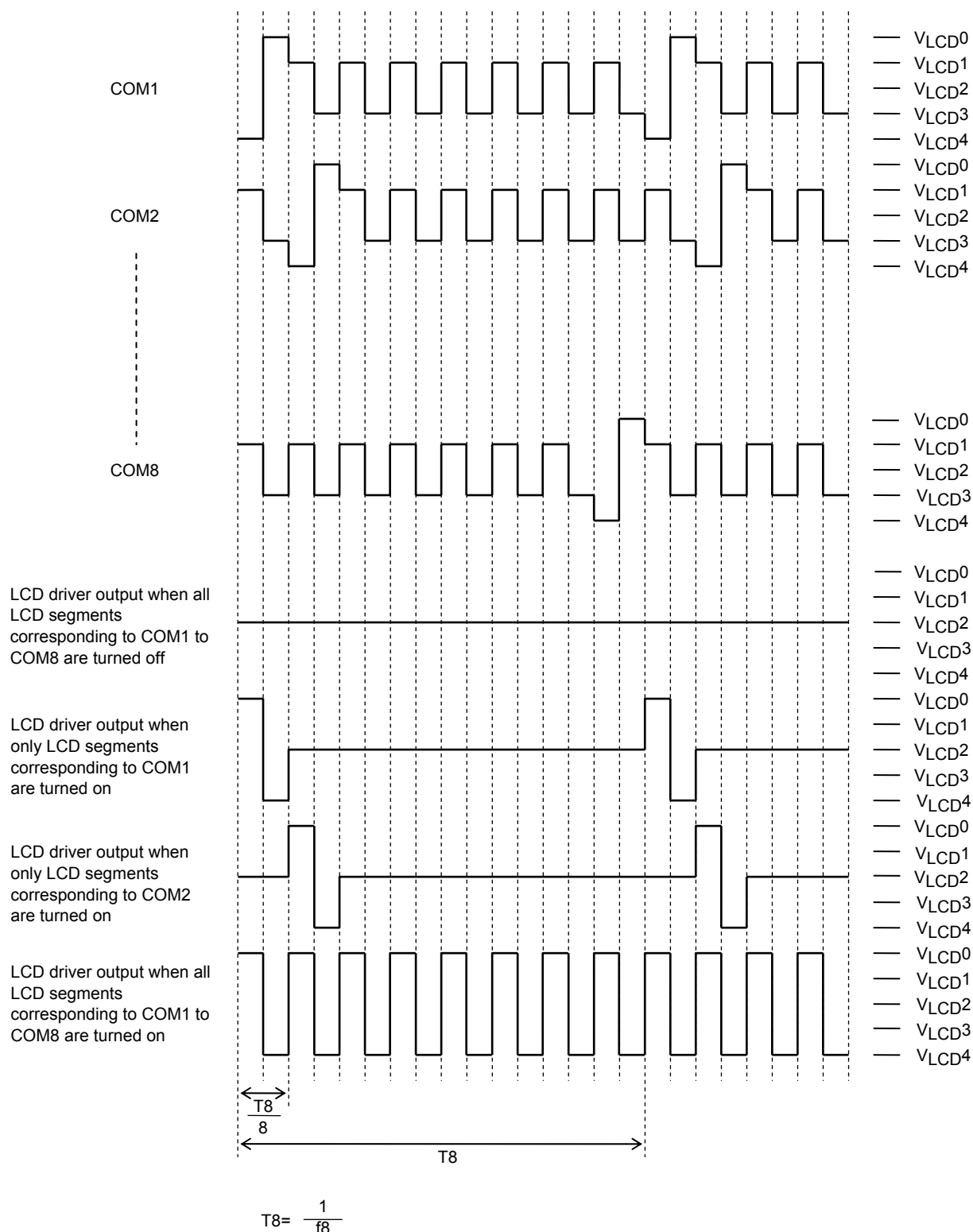
### Multiple Key Presses

Although the LC75818PT is capable of key scanning without inserting diodes for dual key presses, triple key presses on the KI1 to KI5 input pin lines, or multiple key presses on the KS1 to KS6 output pin lines, multiple presses other than these cases may result in keys that were not pressed recognized as having been pressed.

Therefore, a diode must be inserted in series with each key. Applications that do not recognize multiple key presses of three or more keys should check the key data for three or more 1 bits and ignore such data.

# LC75818PT

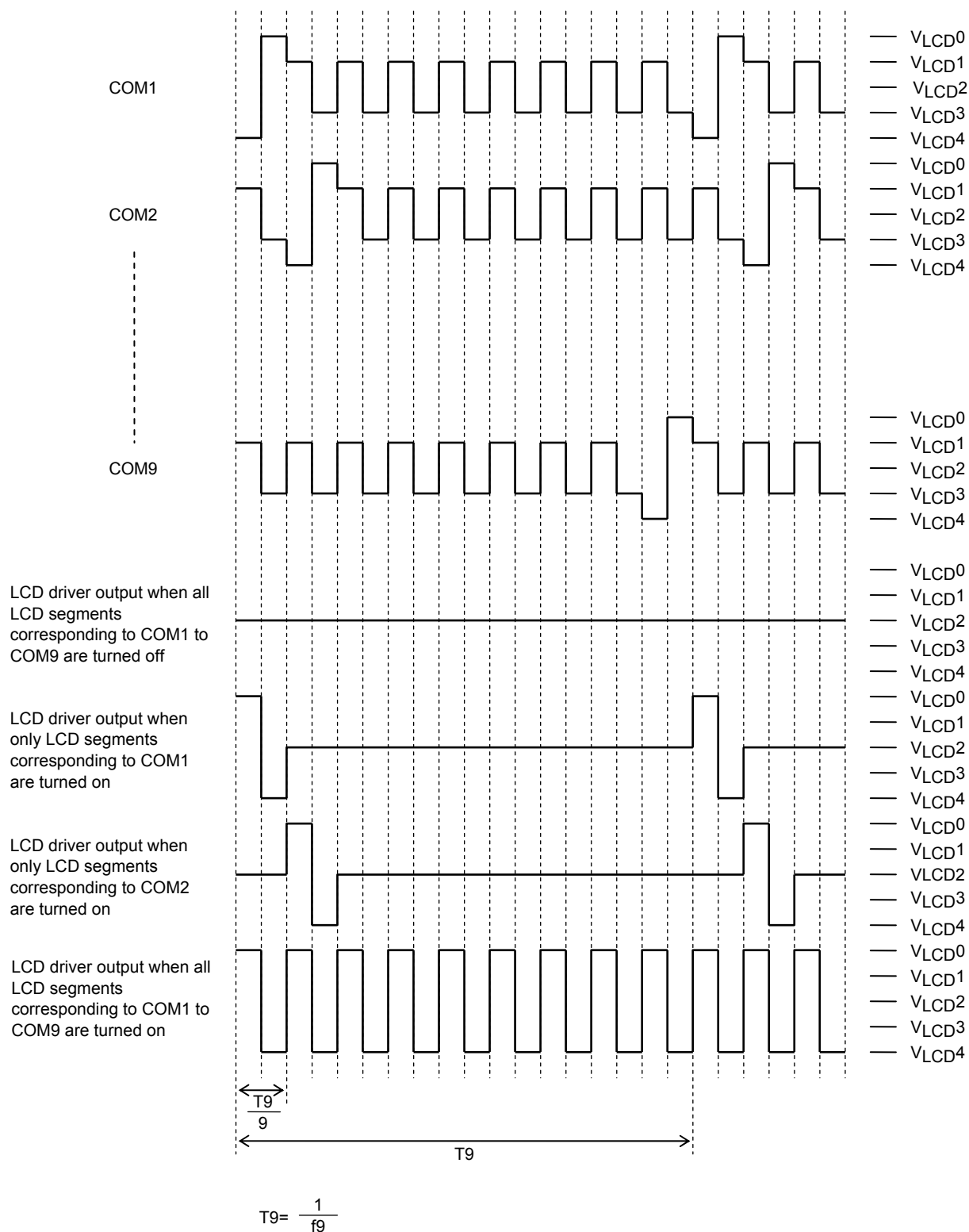
## 1/8 Duty, 1/4 Bias Drive Technique



When a "set display technique" instruction with FC = 0 is executed:  $f8 = \frac{fosc}{3072}$ ,  $f8 = \frac{fCK}{3072}$

When a "set display technique" instruction with FC = 1 is executed:  $f8 = \frac{fosc}{1536}$ ,  $f8 = \frac{fCK}{1536}$

1/9 Duty, 1/4 Bias Drive Technique

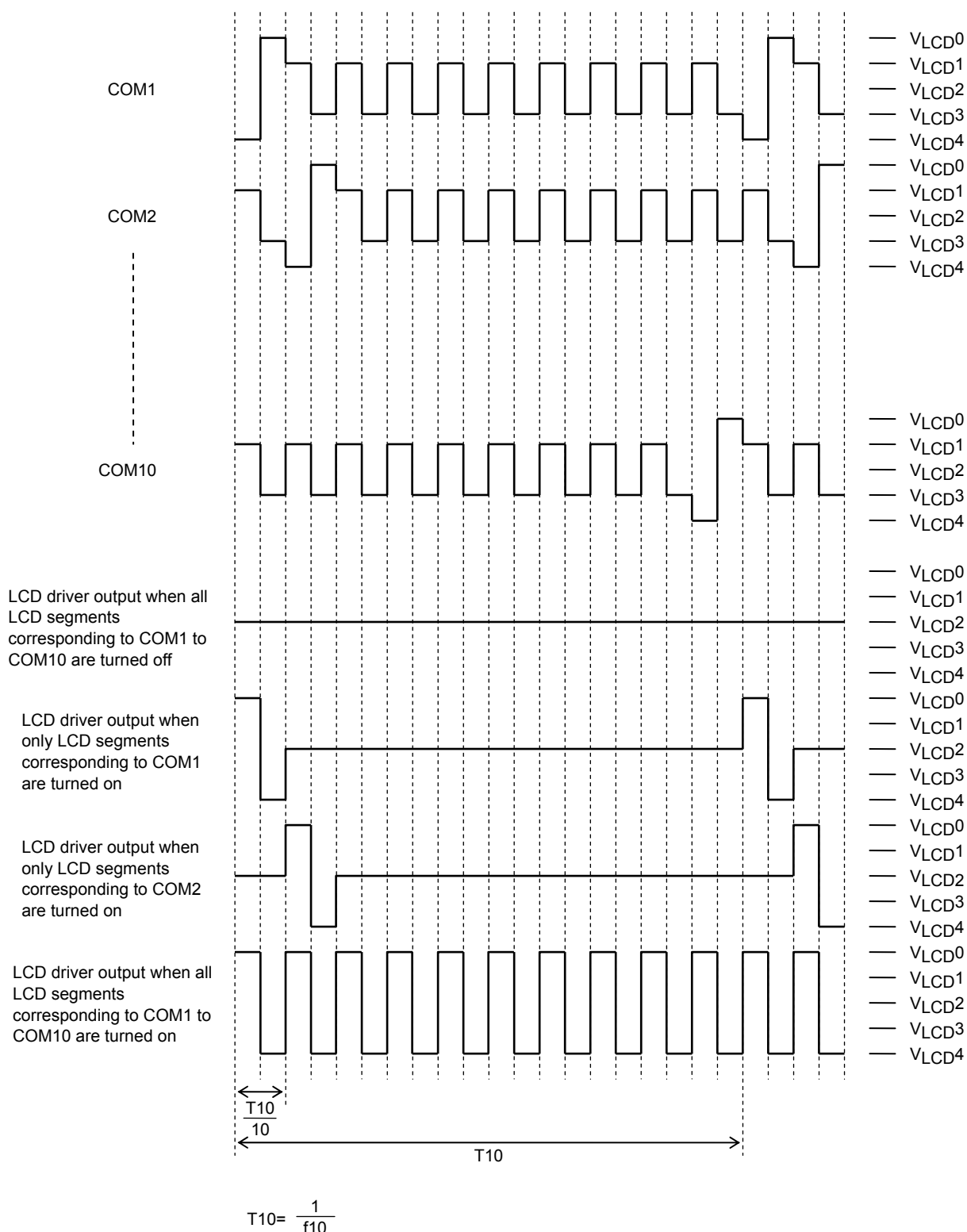


When a "set display technique" instruction with FC = 0 is executed:  $f_9 = \frac{f_{osc}}{3456}$ ,  $f_9 = \frac{f_{CK}}{3456}$

When a "set display technique" instruction with FC = 1 is executed:  $f_9 = \frac{f_{osc}}{1728}$ ,  $f_9 = \frac{f_{CK}}{1728}$

# LC75818PT

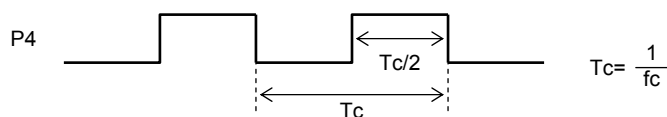
## 1/10 Duty, 1/4 Bias Drive Technique



When a "set display technique" instruction with FC = 0 is executed:  $f_{10} = \frac{f_{osc}}{3840}$ ,  $f_{10} = \frac{f_{CK}}{3840}$

When a "set display technique" instruction with FC = 1 is executed:  $f_{10} = \frac{f_{osc}}{1920}$ ,  $f_{10} = \frac{f_{CK}}{1920}$

## Clock Signal Output Waveform



| "Set Key Scan Output Port/<br>General-purpose Port State"<br>Instruction Data |      | General-purpose port P4<br>clock signal frequency<br>$f_c$ ( $1/T_c$ ) [Hz] |
|-------------------------------------------------------------------------------|------|-----------------------------------------------------------------------------|
| PC40                                                                          | PC41 |                                                                             |
| 0                                                                             | 1    | Clock signal output ( $f_{osc}/2$ , $f_{CK}/2$ )                            |
| 1                                                                             | 1    | Clock signal output ( $f_{osc}/8$ , $f_{CK}/8$ )                            |

## Voltage Detection Type Reset Circuit ( $V_{DET}$ )

This circuit generates an output signal and resets the system when logic block power is first applied and when the voltage drops, i.e., when the logic block power supply voltage is less than or equal to the power down detection voltage  $V_{DET}$ , which is 2.2 V, typical. To assure that this function operates reliably, a capacitor must be added to the logic block power supply line so that the logic block power supply voltage  $V_{DD}$  rise time when the logic block power is first applied and the logic block power supply voltage  $V_{DD}$  fall time when the voltage drops are both at least 1 ms. (See Figure 5.)

## Power Supply Sequence

The following sequences must be observed when power is turned on and off. (See Figure 5.)

- Power on: Logic block power supply ( $V_{DD}$ ) on → LCD driver block power supply ( $V_{LCD}$ ) on
- Power off: LCD driver block power supply ( $V_{LCD}$ ) off → Logic block power supply ( $V_{DD}$ ) off

When 5 V signal is applied to the CE, CL, DI, and  $\overline{INH}$  pins which are to be connected to the controller and if the logic block power supply ( $V_{DD}$ ) is off, set the input voltage at the CE, CL, DI, and  $\overline{INH}$  pins to 0V and apply the 5 V signal to these pins after turning on the logic block power supply ( $V_{DD}$ ).

## System Reset

### 1. Reset function

The LC75818PT performs a system reset with the  $V_{DET}$ . When a system reset is applied, the display is turned off, key scanning is disabled, the key data is reset, and the general-purpose output ports are set to and held at the low level ( $V_{SS}$ ).

These states that are created as a result of the system reset can be cleared by executing the instruction described below. (See Figure 5.)

#### • Clearing the display off state

Display operation can be enabled by executing a "display on/off control" instruction. However, since the contents of the DCRAM, ADRAM, and CGRAM are undefined, applications must set the contents of these memories before turning on display with the "display on/off control" instruction. That is, applications must execute the following instructions.

- Set display technique (The "set display technique" instruction must be executed first.)
- DCRAM data write
- ADRAM data write (If the ADRAM is used.)
- CGRAM data write (If the CGRAM is used.)
- Set AC address
- Set display contrast (If the display contrast adjustment circuit is used.)

After executing the above instructions, applications must turn on the display with a "display on/off control" instruction.

Note that when applications turn off in the normal mode, applications must turn off the display with a "display on/off control" instruction or the  $\overline{INH}$  pin.

## LC75818PT

- Clearing the key scan disable and key data reset states

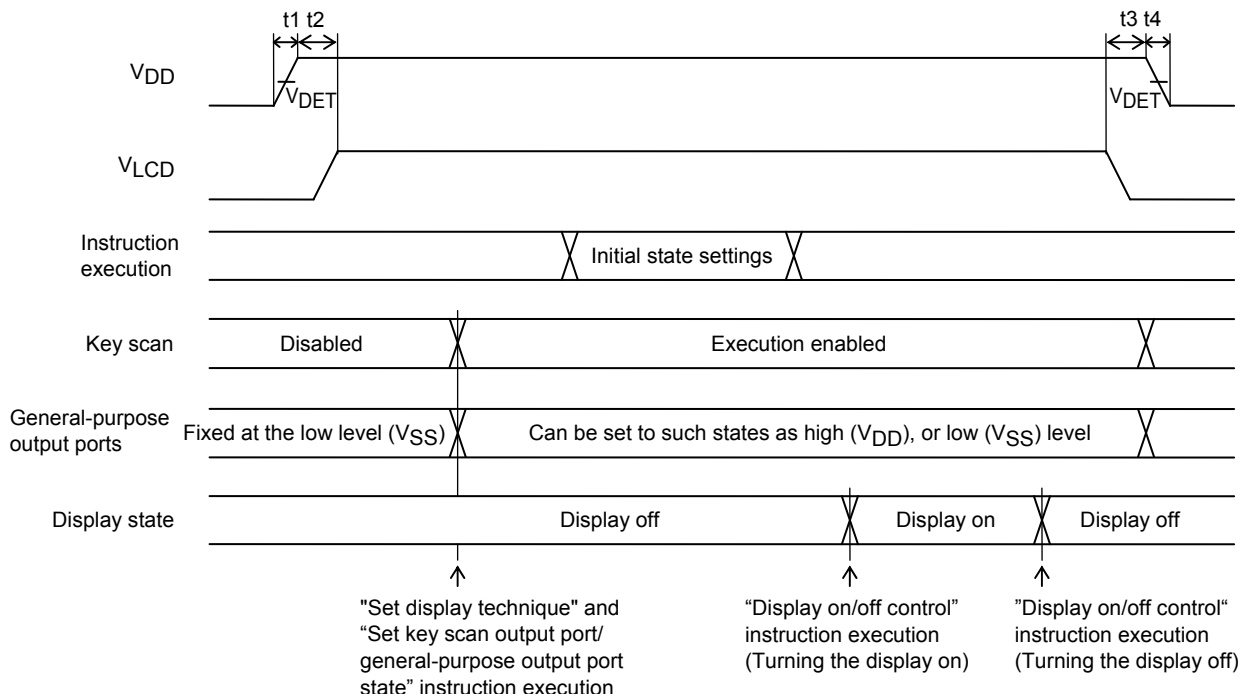
By executing the following instructions not only create a state in which key scanning can be performed, but also clear the key data reset.

- "Set display technique" (The "set display technique" instruction must be executed first.)
- "Set key scan output port / general-purpose output port state"

- Clearing the general-purpose output ports locked at the low level ( $V_{SS}$ ) state

By executing the following instructions clear the general-purpose output ports locked at the low level ( $V_{SS}$ ) state and set the states of the general-purpose output ports.

- "Set display technique" (The "set display technique" instruction must be executed first.)
- "Set key scan output port / general-purpose output port state"



- $t_1 \geq 1$  [ms] (Logic block power supply voltage  $V_{DD}$  rise time)
- $t_2 \geq 0$
- $t_3 \geq 0$
- $t_4 \geq 1$  [ms] (Logic block power supply voltage  $V_{DD}$  fall time)
- Initial state settings
  - Set display technique (The "set display technique" instruction must be executed first.)
  - DCRAM data write
  - ADRAM data write (If the ADRAM is used.)
  - CGRAM data write (If the CGRAM is used.)
  - Set AC address
  - Set display contrast (If the display contrast adjustment circuit is used.)

[Figure 5]

**2. Block states during a system reset****(1) CLOCK GENERATOR, TIMING GENERATOR**

When a reset is applied, these circuits are forcibly initialized internally. Then, when the "set display technique" instruction is executed, oscillation of the OSC pin starts in RC oscillator operating mode (the IC starts receiving the external clock in external clock operating mode), execution of the instruction is enabled.

**(2) INSTRUCTION REGISTER, INSTRUCTION DECODER**

When a reset is applied, these circuits are forcibly initialized internally. Then, when instruction execution starts, the IC operates according to those instructions.

**(3) ADDRESS REGISTER, ADDRESS COUNTER**

When a reset is applied, these circuits are forcibly initialized internally. Then, the DGRAM and the AGRAM addresses are set when "Set AC address" instruction is executed.

**(4) DGRAM, AGRAM, CGRAM**

Since the contents of the DGRAM, AGRAM, and CGRAM become undefined during a reset, applications must execute "DGRAM data write", "AGRAM data write (If the AGRAM is used.)", and "CGRAM data write (If the CGRAM is used.)" instructions before executing a "display on/off control" instruction.

**(5) CGROM**

Character patterns are stored in this ROM.

**(6) LATCH**

Although the value of the data in the latch is undefined during a reset, the AGRAM, CGROM, and CGRAM data is stored by executing a "display on/off control" instruction.

**(7) COMMON DRIVER, SEGMENT DRIVER**

These circuits are forced to the display off state when a reset is applied.

**(8) CONTRAST ADJUSTER**

Display contrast adjustment circuit operation is disabled when a reset is applied. After that, the display contrast can be set by executing a "set display contrast" instruction.

**(9) KEY SCAN, KEY BUFFER**

When a reset is applied, these circuits are forcibly initialized internally, and key scan operation is disabled. Also, the key data is all set to 0. After that, key scanning can be performed by executing a "set key scan output port/general-purpose output port state" instruction.

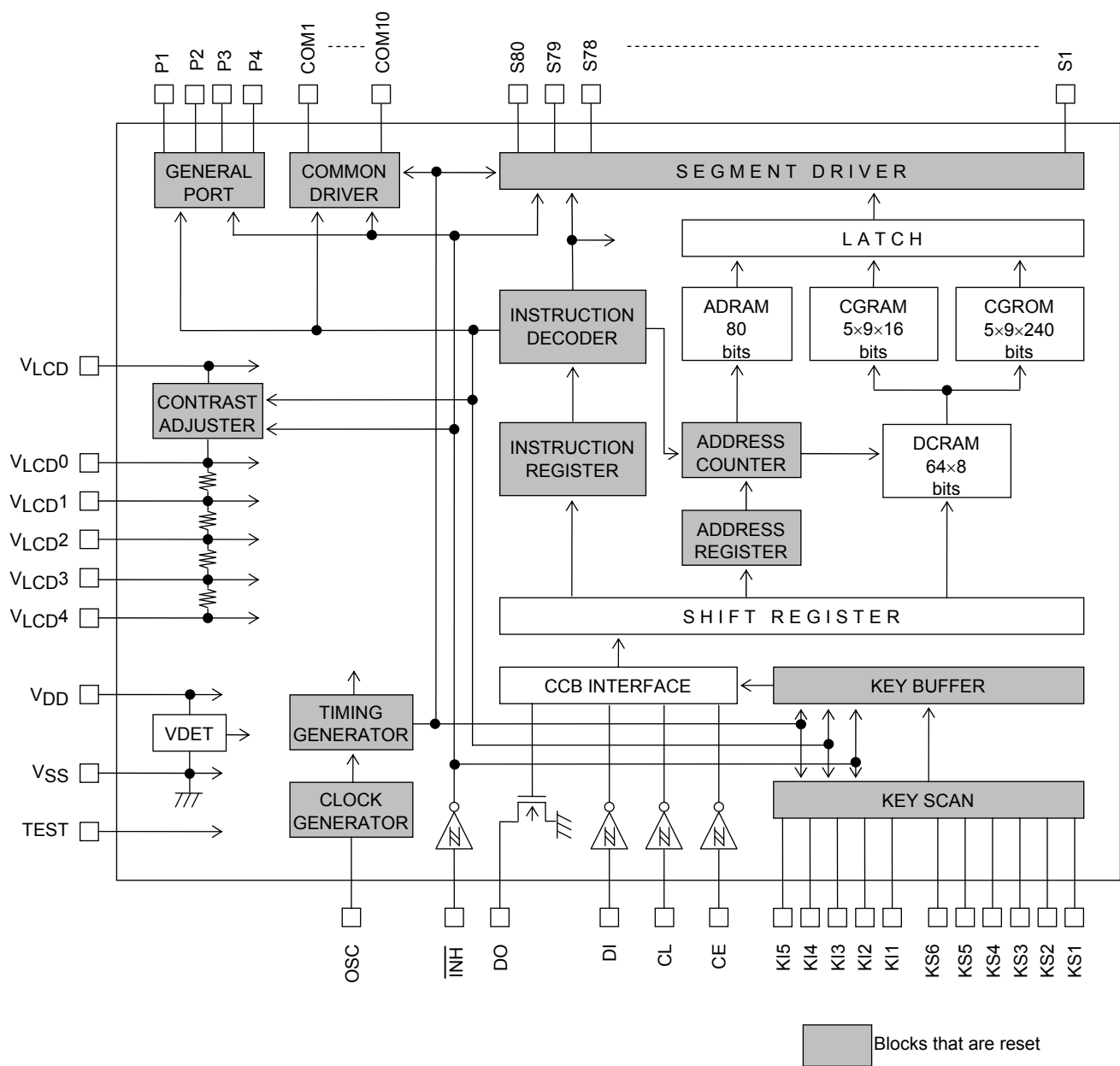
**(10) GENERAL PORT**

When a reset is applied, the general-purpose output port state is locked at the low level (VSS).

**(11) CCB INTERFACE, SHIFT REGISTER**

These circuits go to the serial data input wait state.

LC75818PT



(3) Output pin states during the reset period

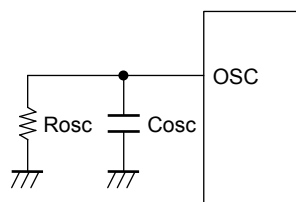
| Output pin    | State during reset     |
|---------------|------------------------|
| S1 to S80     | L (V <sub>LCD4</sub> ) |
| COM1 to COM10 | L (V <sub>LCD4</sub> ) |
| KS1 to KS6    | L (V <sub>SS</sub> )   |
| P1 to P4      | L (V <sub>SS</sub> )   |
| D0            | H *20                  |

Note: \*20. Since this output pin is an open-drain output, a pull-up resistor (between 1 kΩ and 10 kΩ) is required. This pin is held at the high level even if a key data read operation is performed before executing the "set display technique" or "set key scan output port/general-purpose output port state" instruction.

## OSC Pin Peripheral Circuit

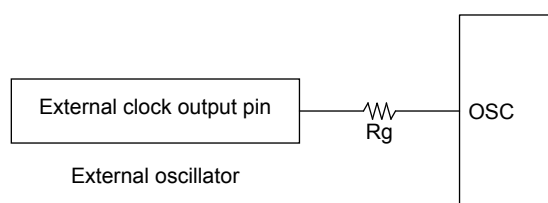
(1) RC oscillator operating mode (when the "set display technique (OC = 0)" instruction is executed)

When RC oscillator operating mode is selected, an external resistor  $R_{osc}$  and an external capacitor  $C_{osc}$  must be connected between the OSC pin and GND.



(2) External clock operating mode (when the "set display technique (OC = 1)" instruction is executed)

When selecting the external clock operating mode, connect a current protection resistor  $R_g$  (2.2 to 22 k $\Omega$ ) between the OSC pin and external clock output pin (external oscillator). Determine the value of the resistance according to the maximum allowable current value at the external clock output pin. Also make sure that the waveform of the external clock is not heavily distorted.



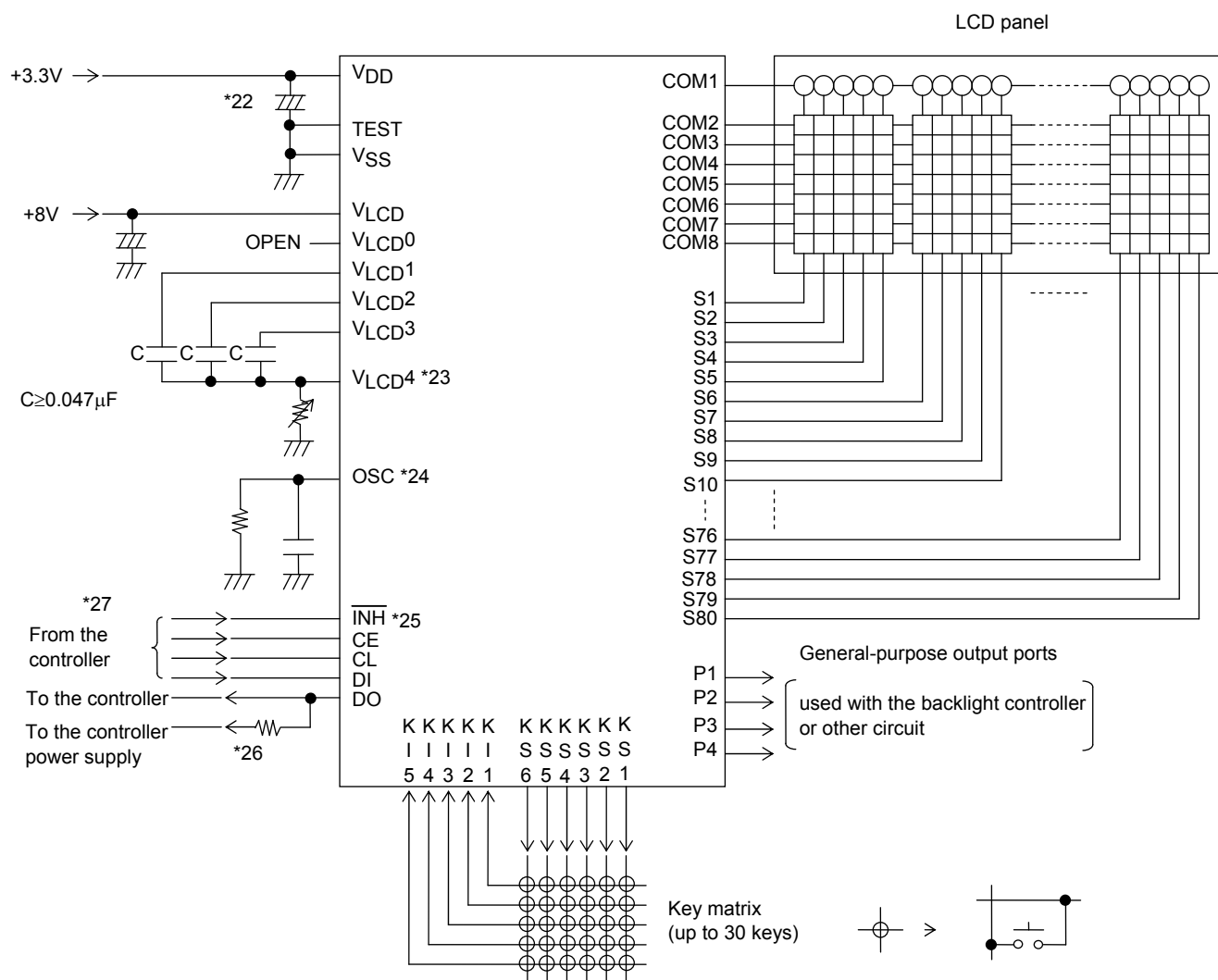
Note: \*21. Allowable current value at external clock output pin  $> \frac{V_{DD}}{R_g}$

## Note when applying a 5V signal to the CE, CL, DI, and $\overline{INH}$ pins

When applying a 5 V signal to the CE, CL, DI, and  $\overline{INH}$  pins which are to be connected to the controller, set the input voltage to the CE, CL, DI, and  $\overline{INH}$  pins to 0V if the logic block power supply ( $V_{DD}$ ) is off, and apply the 5 V signal to those pins after turning on the logic block power supply ( $V_{DD}$ ).

# Sample Application Circuit 1

1/8 duty, 1/4 bias drive technique (for use with normal panels)



Note \*22. Add a capacitor to the logic block power supply line so that the logic block power supply voltage  $V_{DD}$  rise time when power is applied and the logic block power supply voltage  $V_{DD}$  fall time when power drops are both at least 1 ms, as the LC75818PT is reset by the  $V_{DET}$ .

\*23. If a variable resistor is not used for display contrast fine adjustment, the  $V_{LCD4}$  pin must be connected to ground.

\*24. In RC oscillator operating mode, an external resistor,  $R_{osc}$ , and an external capacitor,  $C_{osc}$ , must be connected between the OSC pin and ground. When selecting the external clock operating mode, connect a current protection resistor  $R_g$  (2.2 to 22 k $\Omega$ ) between the OSC pin and the external clock output pin (external oscillator). (See the “OSC Pin Peripheral Circuit” section.)

\*25. If the function of  $\overline{INH}$  pin is not used, the  $\overline{INH}$  pin must be connected to the logic block power supply  $V_{DD}$ .

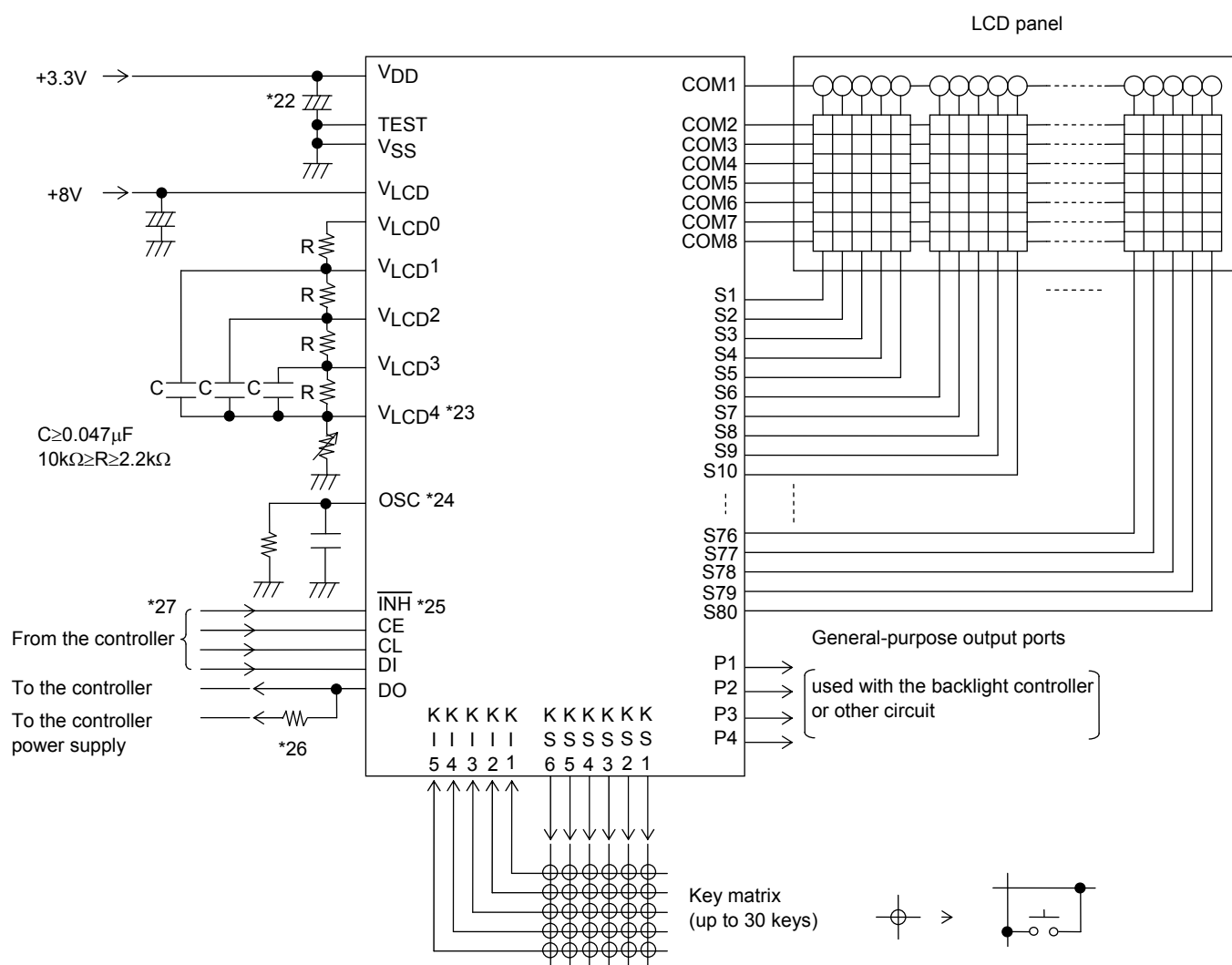
\*26. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 k $\Omega$  and 10 k $\Omega$ ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

\*27 When applying a 5 V signal to the CE, CL, DI, and INH pins, set the input voltage to 0 V if the logic block power supply ( $V_{DD}$ ) is off, and apply the 5 V signal to those pins after turning on the logic block power supply ( $V_{DD}$ ).

## LC75818PT

### Sample Application Circuit 2

1/8 duty, 1/4 bias drive technique (for use with large panels)



Note \*22. Add a capacitor to the logic block power supply line so that the logic block power supply voltage  $V_{DD}$  rise time when power is applied and the logic block power supply voltage  $V_{DD}$  fall time when power drops are both at least 1 ms, as the LC75818PT is reset by the  $V_{DET}$ .

\*23. If a variable resistor is not used for display contrast fine adjustment, the  $V_{LCD4}$  pin must be connected to ground.

\*24. In RC oscillator operating mode, an external resistor,  $R_{osc}$ , and an external capacitor,  $C_{osc}$ , must be connected between the OSC pin and ground. When selecting the external clock operating mode, connect a current protection resistor  $R_g$  (2.2 to 22 k $\Omega$ ) between the OSC pin and the external clock output pin (external oscillator). (See the “OSC Pin Peripheral Circuit” section.)

\*25. If the function of  $\overline{INH}$  pin is not used, the  $\overline{INH}$  pin must be connected to the logic block power supply  $V_{DD}$ .

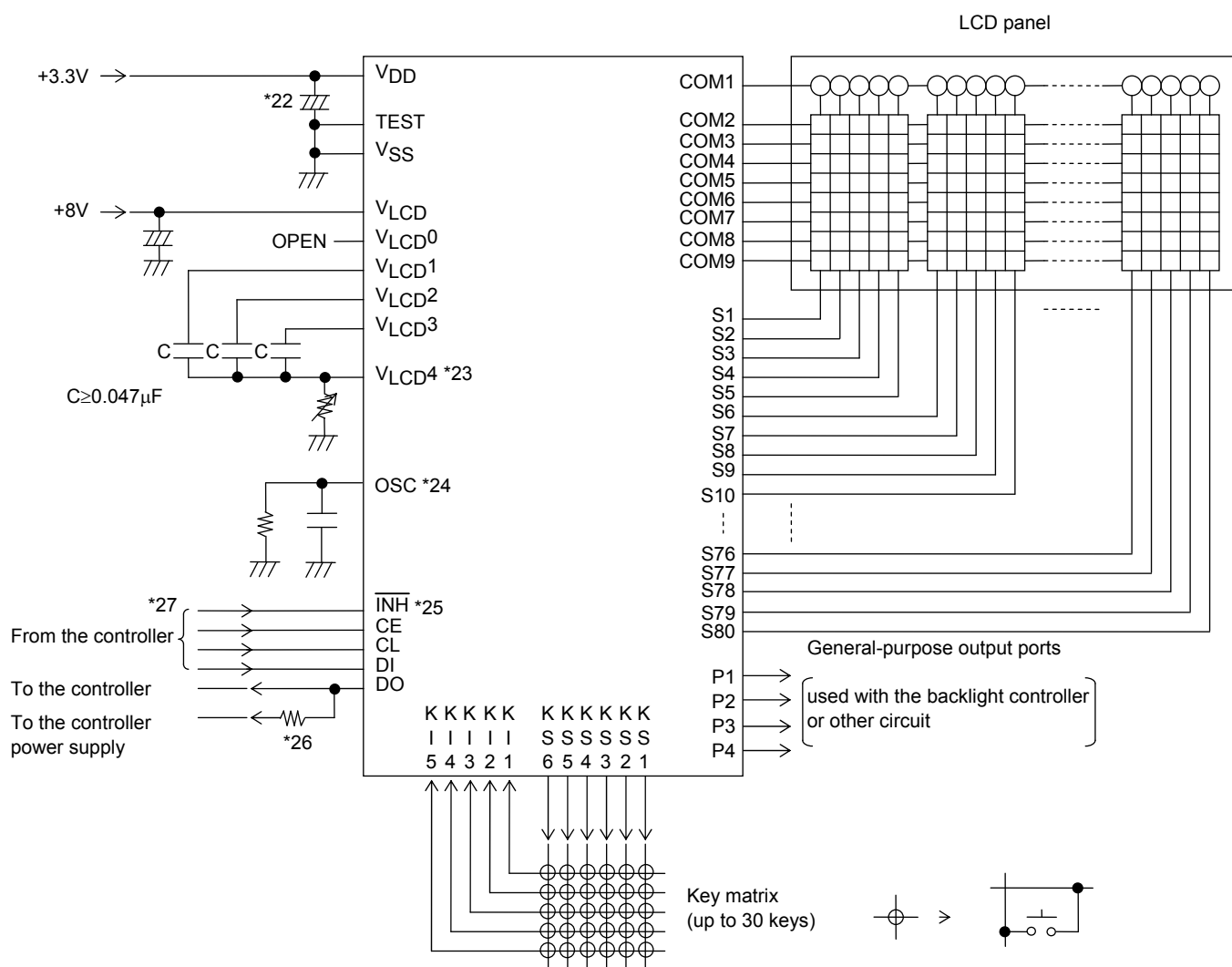
\*26. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 k $\Omega$  and 10 k $\Omega$ ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

\*27 When applying a 5 V signal to the CE, CL, DI, and  $\overline{INH}$  pins, set the input voltage to 0 V if the logic block power supply ( $V_{DD}$ ) is off, and apply the 5 V signal to those pins after turning on the logic block power supply ( $V_{DD}$ ).

# LC75818PT

## Sample Application Circuit 3

1/9 duty, 1/4 bias drive technique (for use with normal panels)



Note \*22. Add a capacitor to the logic block power supply line so that the logic block power supply voltage  $V_{DD}$  rise time when power is applied and the logic block power supply voltage  $V_{DD}$  fall time when power drops are both at least 1 ms, as the LC75818PT is reset by the  $V_{DET}$ .

\*23. If a variable resistor is not used for display contrast fine adjustment, the  $V_{LCD4}$  pin must be connected to ground.

\*24. In RC oscillator operating mode, an external resistor,  $R_{osc}$ , and an external capacitor,  $C_{osc}$ , must be connected between the OSC pin and ground. When selecting the external clock operating mode, connect a current protection resistor  $R_g$  (2.2 to 22 k $\Omega$ ) between the OSC pin and the external clock output pin (external oscillator). (See the “OSC Pin Peripheral Circuit” section.)

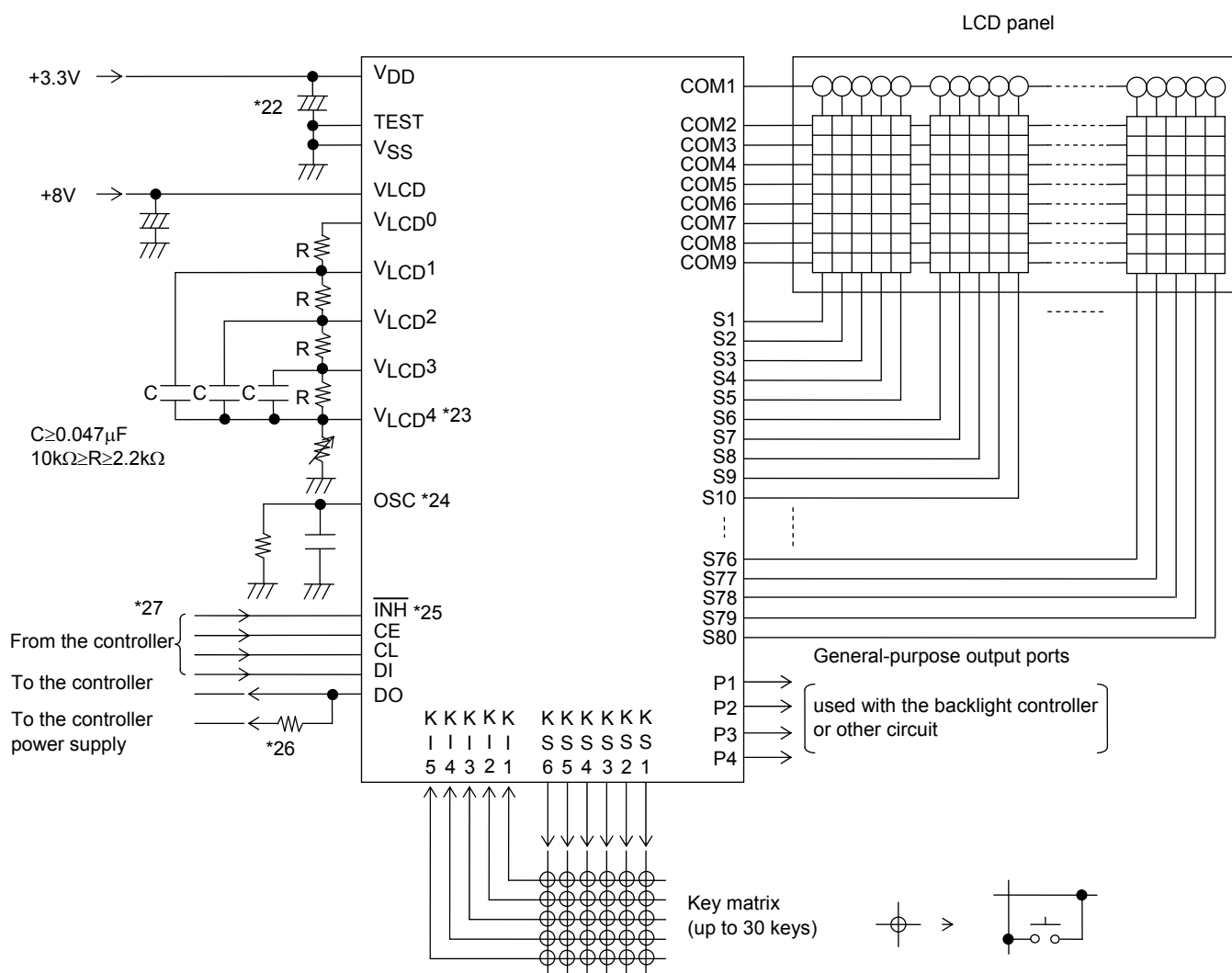
\*25. If the function of  $\overline{INH}$  pin is not used, the  $\overline{INH}$  pin must be connected to the logic block power supply  $V_{DD}$ .

\*26. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 k $\Omega$  and 10 k $\Omega$ ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

\*27 When applying a 5 V signal to the CE, CL, DI, and  $\overline{INH}$  pins, set the input voltage to 0 V if the logic block power supply ( $V_{DD}$ ) is off, and apply the 5 V signal to those pins after turning on the logic block power supply ( $V_{DD}$ ).

# Sample Application Circuit 4

1/9 duty, 1/4 bias drive technique (for use with large panels)



Note \*22. Add a capacitor to the logic block power supply line so that the logic block power supply voltage  $V_{DD}$  rise time when power is applied and the logic block power supply voltage  $V_{DD}$  fall time when power drops are both at least 1 ms, as the LC75818PT is reset by the  $V_{DET}$ .

\*23. If a variable resistor is not used for display contrast fine adjustment, the  $V_{LCD4}$  pin must be connected to ground.

\*24. In RC oscillator operating mode, an external resistor,  $R_{osc}$ , and an external capacitor,  $C_{osc}$ , must be connected between the OSC pin and ground. When selecting the external clock operating mode, connect a current protection resistor  $R_g$  (2.2 to 22 k $\Omega$ ) between the OSC pin and the external clock output pin (external oscillator). (See the “OSC Pin Peripheral Circuit” section.)

\*25. If the function of  $\overline{INH}$  pin is not used, the  $\overline{INH}$  pin must be connected to the logic block power supply  $V_{DD}$ .

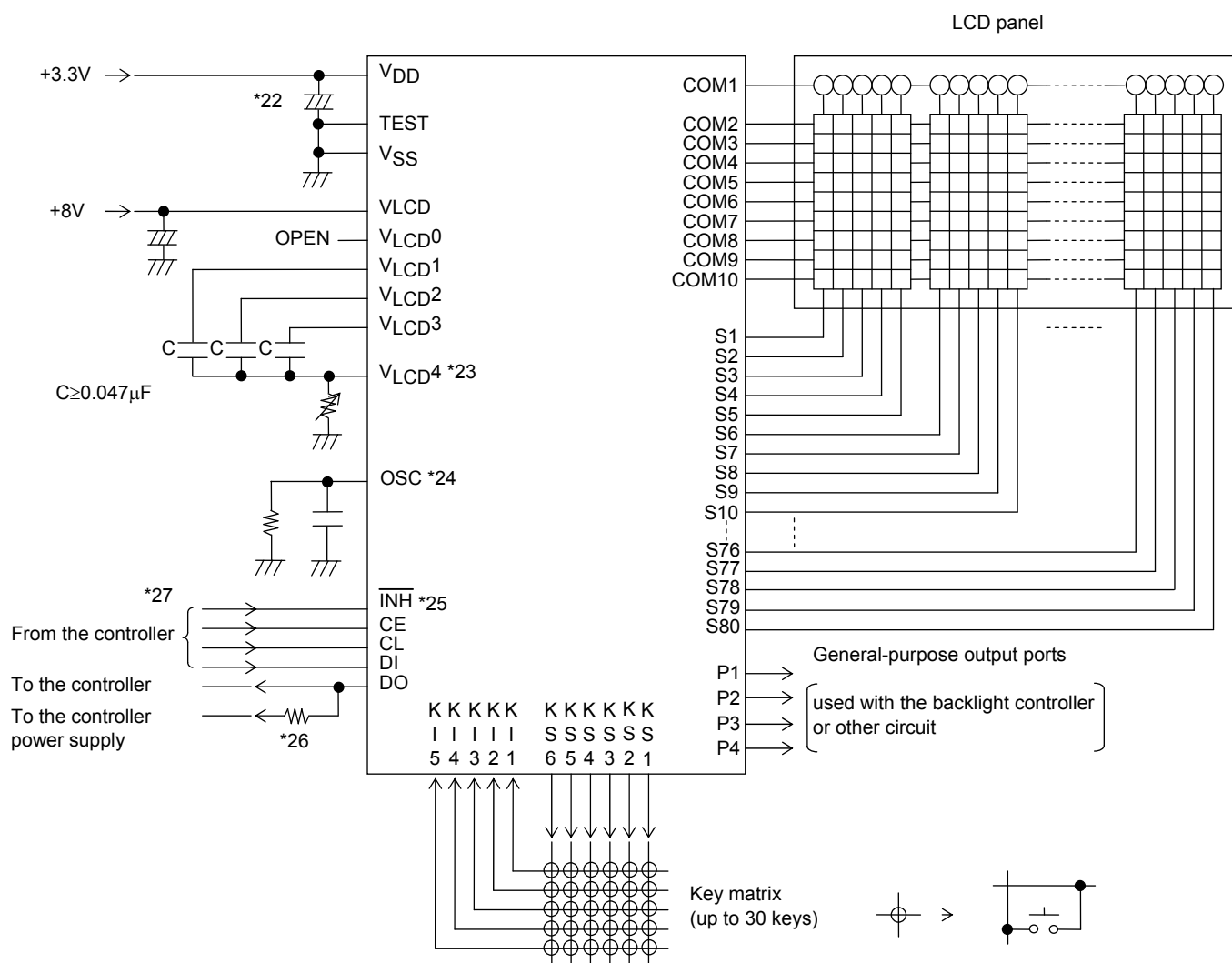
\*26. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 k $\Omega$  and 10 k $\Omega$ ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

\*27 When applying a 5 V signal to the CE, CL, DI, and  $\overline{INH}$  pins, set the input voltage to 0 V if the logic block power supply ( $V_{DD}$ ) is off, and apply the 5 V signal to those pins after turning on the logic block power supply ( $V_{DD}$ ).

# LC75818PT

## Sample Application Circuit 5

1/10 duty, 1/4 bias drive technique (for use with normal panels)



Note \*22. Add a capacitor to the logic block power supply line so that the logic block power supply voltage  $V_{DD}$  rise time when power is applied and the logic block power supply voltage  $V_{DD}$  fall time when power drops are both at least 1 ms, as the LC75818PT is reset by the  $V_{DET}$ .

\*23. If a variable resistor is not used for display contrast fine adjustment, the  $V_{LCD4}$  pin must be connected to ground.

\*24. In RC oscillator operating mode, an external resistor,  $R_{osc}$ , and an external capacitor,  $C_{osc}$ , must be connected between the OSC pin and ground. When selecting the external clock operating mode, connect a current protection resistor  $R_g$  (2.2 to 22 k $\Omega$ ) between the OSC pin and the external clock output pin (external oscillator). (See the “OSC Pin Peripheral Circuit” section.)

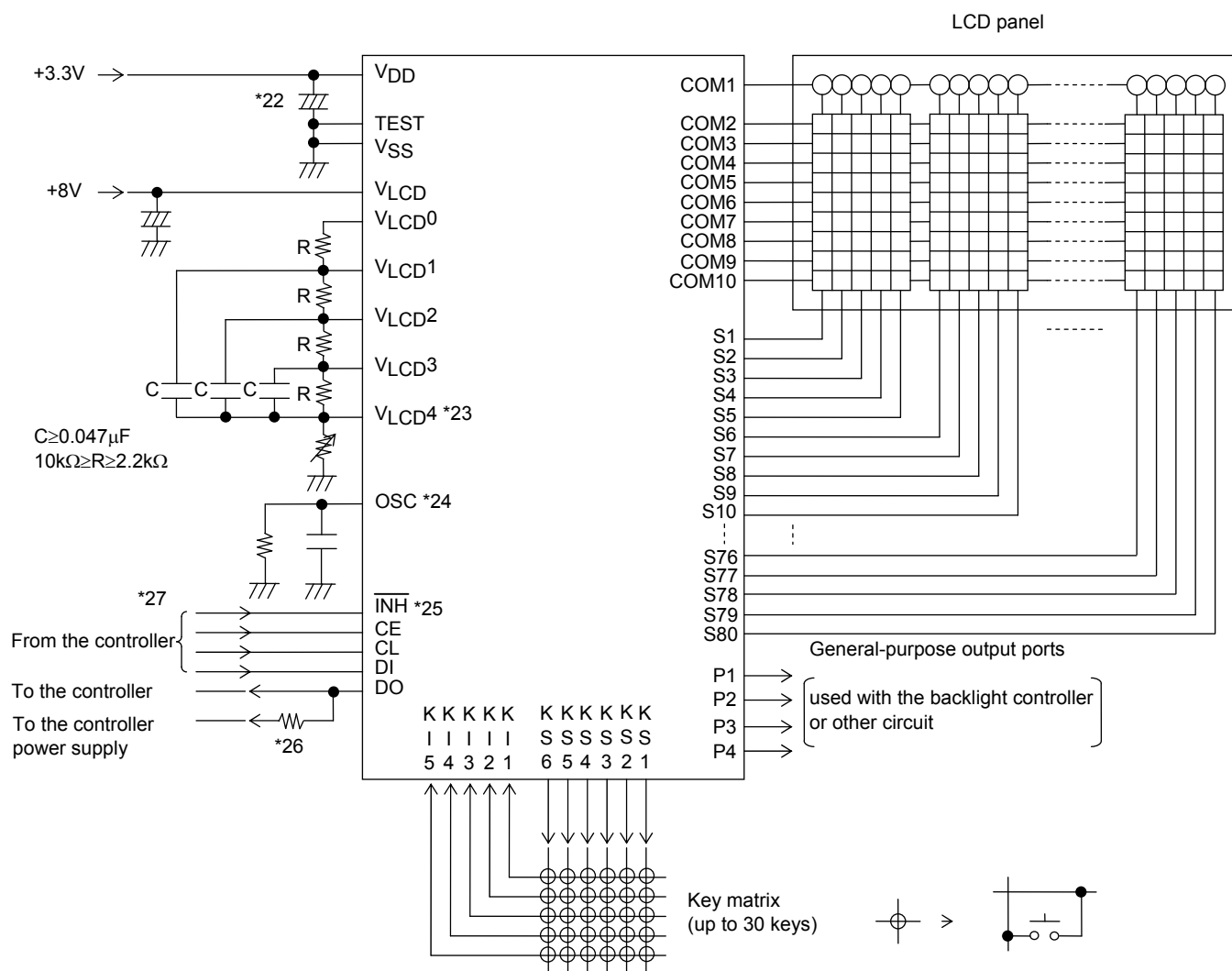
\*25. If the function of  $\overline{INH}$  pin is not used, the  $\overline{INH}$  pin must be connected to the logic block power supply  $V_{DD}$ .

\*26. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 k $\Omega$  and 10 k $\Omega$ ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

\*27 When applying a 5 V signal to the CE, CL, DI, and  $\overline{INH}$  pins, set the input voltage to 0 V if the logic block power supply ( $V_{DD}$ ) is off, and apply the 5 V signal to those pins after turning on the logic block power supply ( $V_{DD}$ ).

# Sample Application Circuit 6

1/10 duty, 1/4 bias drive technique (for use with large panels)



Note \*22. Add a capacitor to the logic block power supply line so that the logic block power supply voltage  $V_{DD}$  rise time when power is applied and the logic block power supply voltage  $V_{DD}$  fall time when power drops are both at least 1 ms, as the LC75818PT is reset by the  $V_{DET}$ .

\*23. If a variable resistor is not used for display contrast fine adjustment, the  $V_{LCD4}$  pin must be connected to ground.

\*24. In RC oscillator operating mode, an external resistor,  $R_{osc}$ , and an external capacitor,  $C_{osc}$ , must be connected between the OSC pin and ground. When selecting the external clock operating mode, connect a current protection resistor  $R_g$  (2.2 to 22 k $\Omega$ ) between the OSC pin and the external clock output pin (external oscillator). (See the “OSC Pin Peripheral Circuit” section.)

\*25. If the function of INH pin is not used, the INH pin must be connected to the logic block power supply  $V_{DD}$ .

\*26. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 k $\Omega$  and 10 k $\Omega$ ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

\*27 When applying a 5 V signal to the CE, CL, DI, and INH pins, set the input voltage to 0 V if the logic block power supply ( $V_{DD}$ ) is off, and apply the 5 V signal to those pins after turning on the logic block power supply ( $V_{DD}$ ).

# LC75818PT

## Sample Correspondence between Instructions and the Display (When the LC75818PT-8560 is used)

| No. | Instruction (hexadecimal)                                        |               |               |               |               |                      | Display | Operation                                               |
|-----|------------------------------------------------------------------|---------------|---------------|---------------|---------------|----------------------|---------|---------------------------------------------------------|
|     | LSB<br>D40 to<br>D43                                             | D44 to<br>D47 | D48 to<br>D51 | D52 to<br>D55 | D56 to<br>D59 | MSB<br>D60 to<br>D63 |         |                                                         |
| 1   | Power application<br>(Initialization with the V <sub>DET</sub> ) |               |               |               |               |                      |         | Initializes the IC.<br>The display is in the off state. |
| 2   | Set display technique                                            |               |               |               |               |                      |         | Sets to 1/8 duty 1/4 bias display drive technique       |
| 3   | DCRAM data write (increment mode)                                |               |               |               |               |                      |         | Writes the display data " " to DCRAM address 00H        |
|     | 0                                                                | 2             | 0             | 0             | 1             | A                    |         |                                                         |
| 4   | DCRAM data write (increment mode)                                |               |               |               |               |                      |         | Writes the display data "S" to DCRAM address 01H        |
| 5   | DCRAM data write (increment mode)                                |               |               |               |               |                      |         | Writes the display data "A" to DCRAM address 02H        |
|     |                                                                  |               |               |               |               |                      |         |                                                         |
| 6   | DCRAM data write (increment mode)                                |               |               |               |               |                      |         | Writes the display data "N" to DCRAM address 03H        |
| 7   | DCRAM data write (increment mode)                                |               |               |               |               |                      |         | Writes the display data "Y" to DCRAM address 04H        |
|     |                                                                  |               |               |               |               |                      |         |                                                         |
| 8   | DCRAM data write (increment mode)                                |               |               |               |               |                      |         | Writes the display data "O" to DCRAM address 05H        |
| 9   | DCRAM data write (increment mode)                                |               |               |               |               |                      |         | Writes the display data " " to DCRAM address 06H        |
|     |                                                                  |               |               |               |               |                      |         |                                                         |
| 10  | DCRAM data write (increment mode)                                |               |               |               |               |                      |         | Writes the display data "L" to DCRAM address 07H        |
| 11  | DCRAM data write (increment mode)                                |               |               |               |               |                      |         | Writes the display data "S" to DCRAM address 08H        |
|     |                                                                  |               |               |               |               |                      |         |                                                         |
| 12  | DCRAM data write (increment mode)                                |               |               |               |               |                      |         | Writes the display data "I" to DCRAM address 09H        |
| 13  | DCRAM data write (increment mode)                                |               |               |               |               |                      |         | Writes the display data " " to DCRAM address 0AH        |
|     |                                                                  |               |               |               |               |                      |         |                                                         |
| 14  | DCRAM data write (increment mode)                                |               |               |               |               |                      |         | Writes the display data "L" to DCRAM address 0BH        |
| 15  | DCRAM data write (increment mode)                                |               |               |               |               |                      |         | Writes the display data "C" to DCRAM address 0CH        |
|     |                                                                  |               |               |               |               |                      |         |                                                         |
| 16  | DCRAM data write (increment mode)                                |               |               |               |               |                      |         | Writes the display data "7" to DCRAM address 0DH        |
| 17  | DCRAM data write (increment mode)                                |               |               |               |               |                      |         | Writes the display data "5" to DCRAM address 0EH        |
|     |                                                                  |               |               |               |               |                      |         |                                                         |
| 18  | DCRAM data write (increment mode)                                |               |               |               |               |                      |         | Writes the display data "8" to DCRAM address 0FH        |
| 19  | DCRAM data write (increment mode)                                |               |               |               |               |                      |         | Writes the display data "1" to DCRAM address 10H        |
|     |                                                                  |               |               |               |               |                      |         |                                                         |
| 20  | DCRAM data write (increment mode)                                |               |               |               |               |                      |         | Writes the display data "8" to DCRAM address 11H        |
| 21  | DCRAM data write (increment mode)                                |               |               |               |               |                      |         | Writes the display data " " to DCRAM address 12H        |
|     |                                                                  | 0             | 2             | 0             |               | A                    |         |                                                         |

Continued on next page.

## LC75818PT

Continued from preceding page.

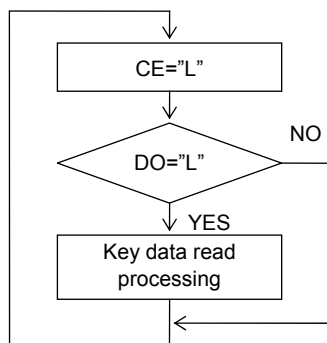
| No. | Instruction (hexadecimal) |               |               |               |               |                      | Display          | Operation                                                    |
|-----|---------------------------|---------------|---------------|---------------|---------------|----------------------|------------------|--------------------------------------------------------------|
|     | LSB<br>D40 to<br>D43      | D44 to<br>D47 | D48 to<br>D51 | D52 to<br>D55 | D56 to<br>D59 | MSB<br>D60 to<br>D63 |                  |                                                              |
| 22  | Set AC address            |               |               |               |               |                      |                  | Loads the DCRAM address 00H and the ADRAM address 0H into AC |
|     |                           |               | 0             | 0             | 0             | 2                    |                  |                                                              |
| 23  | Display on/off control    |               |               |               |               |                      | SANYO LSI LC758  | Turns on the LCD for all digits (16 digits) in MDATA         |
|     | F                         | F             | F             | F             | 1             | 4                    |                  |                                                              |
| 24  | Display shift             |               |               |               |               |                      | SANYO LSI LC7581 | Shifts the display (MDATA only) to the left                  |
|     |                           |               |               |               | 1             | C                    |                  |                                                              |
| 25  | Display shift             |               |               |               |               |                      | ANYO LSI LC75818 | Shifts the display (MDATA only) to the left                  |
|     |                           |               |               |               | 1             | C                    |                  |                                                              |
| 26  | Display shift             |               |               |               |               |                      | NYO LSI LC75818  | Shifts the display (MDATA only) to the left                  |
|     |                           |               |               |               | 1             | C                    |                  |                                                              |
| 27  | Display shift             |               |               |               |               |                      | YO LSI LC75818   | Shifts the display (MDATA only) to the left                  |
|     |                           |               |               |               | 1             | C                    |                  |                                                              |
| 28  | Display shift             |               |               |               |               |                      | O LSI LC75818    | Shifts the display (MDATA only) to the left                  |
|     |                           |               |               |               | 1             | C                    |                  |                                                              |
| 29  | Display shift             |               |               |               |               |                      | LSI LC75818      | Shifts the display (MDATA only) to the left                  |
|     |                           |               |               |               | 1             | C                    |                  |                                                              |
| 30  | Display on/off control    |               |               |               |               |                      |                  | Set to sleep mode, turns off the LCD for all digits          |
|     | 0                         | 0             | 0             | 0             | 8             | 4                    |                  |                                                              |
| 31  | Display on/off control    |               |               |               |               |                      | LSI LC75818      | Turns on the LCD for all digits (16 digits) in MDATA         |
|     | F                         | F             | F             | F             | 1             | 4                    |                  |                                                              |
| 32  | Set AC address            |               |               |               |               |                      | SANYO LSI LC758  | Loads the DCRAM address 00H and the ADRAM address 0H into AC |
|     |                           |               | 0             | 0             | 0             | 2                    |                  |                                                              |

Note: \*28. This sample above assumes the use of 16 digits 5×7 dot matrix LCD. CGRAM and ADRAM are not used.

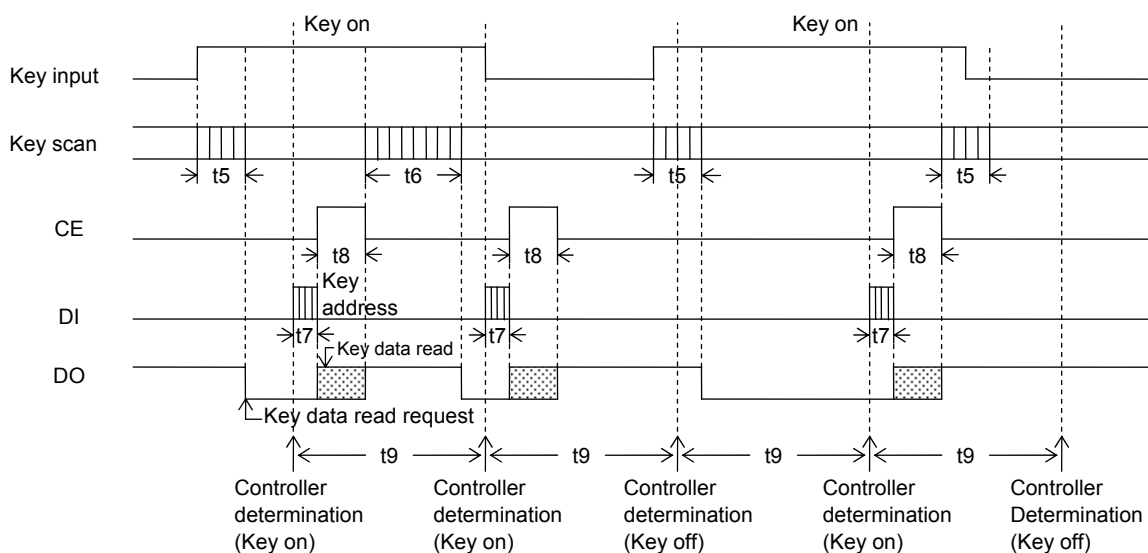
## Notes on the controller key data read techniques

### 1. Timer based key data acquisition

#### • Flowchart



#### • Timing chart



t5: Key scan execution time when the key data agreed for two key scans. (4800T(s))

t6: Key scan execution time when the key data did not agree for two key scans and the key scan was executed again. (9600T(s))

t7: Key address (43H) transfer time

t8: Key data read time

$$T = \frac{1}{f_{osc}} \quad T = \frac{1}{f_{CK}}$$

#### • Explanation

In this technique, the controller uses a timer to determine key on/off states and read the key data. The controller must check the DO state when CE is low every t9 period without fail. If DO is low, the controller recognizes that a key has been pressed and executes the key data read operation.

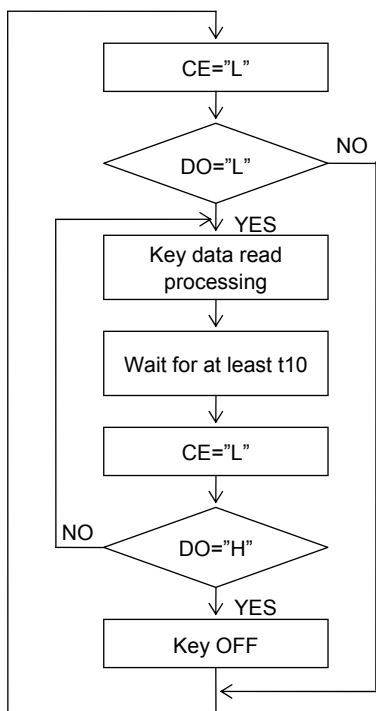
The period t9 in this technique must satisfy the following condition.

$$t9 > t6 + t7 + t8$$

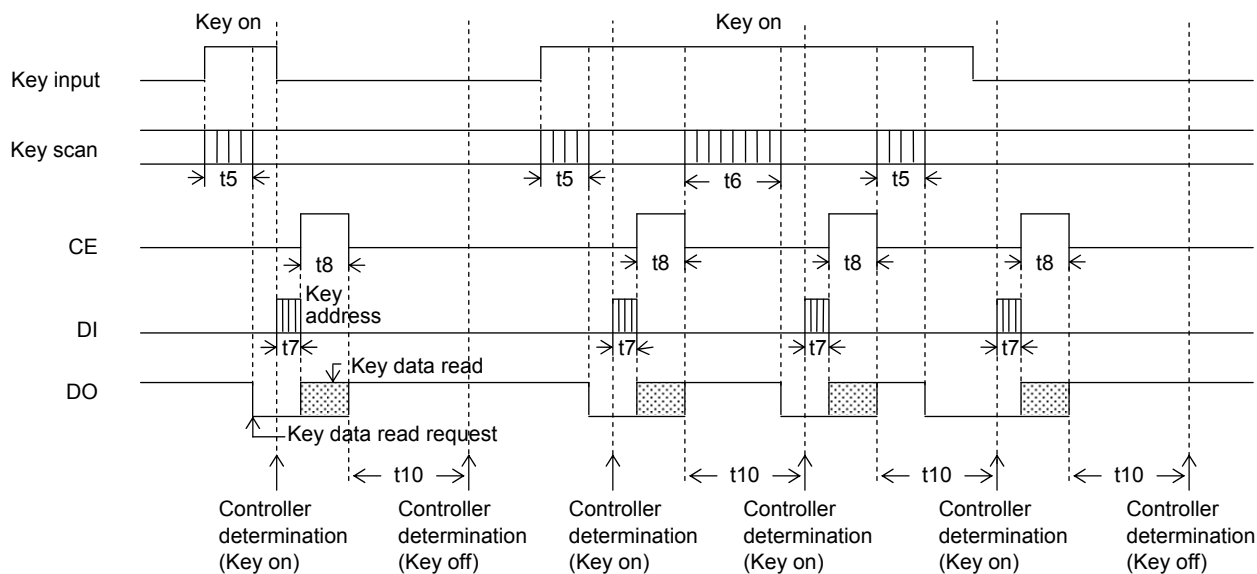
If a key data read operation is executed when DO is high, the read key data (KD1 to KD30) and sleep acknowledge data (SA) will be invalid.

## 2. Interrupt based key data acquisition

### • Flowchart



### • Timing chart



t5: Key scan execution time when the key data agreed for two key scans. (4800T(s))

t6: Key scan execution time when the key data did not agree for two key scans and the key scan was executed again. (9600T(s))

t7: Key address (43H) transfer time

t8: Key data read time

$$T = \frac{1}{f_{osc}} \quad T = \frac{1}{f_{CK}}$$

- Explanation

In this technique, the controller uses interrupts to determine key on/off states and read the key data. The controller must check the DO state when CE is low. If DO is low, the controller recognizes that a key has been pressed and executes the key data read operation. After that the next key on/off determination is performed after the time  $t_{10}$  has elapsed by checking the DO state when CE is low and reading the key data. The period  $t_{10}$  in this technique must satisfy the following condition.

$$t_{10} > t_6$$

If a key data read operation is executed when DO is high, the read key data (KD1 to KD30) and sleep acknowledge data (SA) will be invalid.

LC75818PT-8560 Character Font (Standard)

| Upper<br>4BIT |              | Lower<br>4BIT |  | MSB<br>0000 | 0001 | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |  |  |  |
|---------------|--------------|---------------|--|-------------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|--|--|--|
| 0000<br>LSB   | CG<br>RAM(1) | $\alpha$      |  |             |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |  |  |  |
|               |              |               |  |             |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |  |  |  |
|               |              |               |  |             |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |  |  |  |
|               |              |               |  |             |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |  |  |  |
| 0001          | (2)          | $\beta$       |  |             |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |  |  |  |
|               |              |               |  |             |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |  |  |  |
|               |              |               |  |             |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |  |  |  |
|               |              |               |  |             |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |  |  |  |
| 0010          | (3)          | $\pm$         |  |             |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |  |  |  |
|               |              |               |  |             |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |  |  |  |
|               |              |               |  |             |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |  |  |  |
|               |              |               |  |             |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |  |  |  |
| 0011          | (4)          | $\div$        |  |             |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |  |  |  |
|               |              |               |  |             |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |  |  |  |
|               |              |               |  |             |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |  |  |  |
|               |              |               |  |             |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |  |  |  |
| 0100          | (5)          | $\pi$         |  |             |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |  |  |  |
|               |              |               |  |             |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |  |  |  |
|               |              |               |  |             |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |  |  |  |
|               |              |               |  |             |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |  |  |  |
| 0101          | (6)          | $\acute{c}$   |  |             |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |  |  |  |
|               |              |               |  |             |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |  |  |  |
|               |              |               |  |             |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |  |  |  |
|               |              |               |  |             |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |  |  |  |
| 0110          | (7)          | $\Phi$        |  |             |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |  |  |  |
|               |              |               |  |             |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |  |  |  |
|               |              |               |  |             |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |  |  |  |
|               |              |               |  |             |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |  |  |  |
| 0111          | (8)          | $\phi$        |  |             |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |  |  |  |
|               |              |               |  |             |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |  |  |  |
|               |              |               |  |             |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |  |  |  |

## LC75818PT

### ORDERING INFORMATION

| Device           | Package                                             | Shipping (Qty / Packing) |
|------------------|-----------------------------------------------------|--------------------------|
| LC75818PT-8560-H | TQFP120 14x14 / TQFP120<br>(Pb-Free / Halogen Free) | 450 / Tray JEDEC         |

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