

FDMA2002NZ

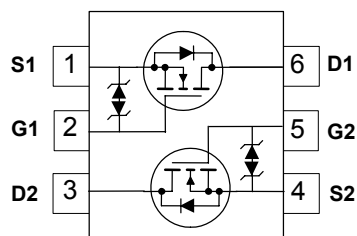
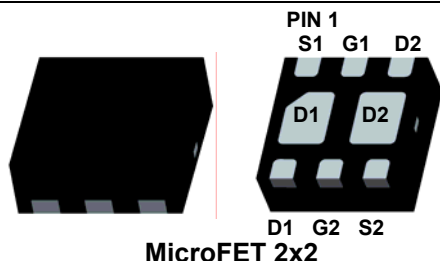
Dual N-Channel PowerTrench® MOSFET

General Description

This device is designed specifically as a single package solution for dual switching requirements in cellular handset and other ultra-portable applications. It features two independent N-Channel MOSFETs with low on-state resistance for minimum conduction losses. The MicroFET 2x2 offers exceptional thermal performance for its physical size and is well suited to linear mode applications.

Features

- 2.9 A, 30 V $R_{DS(ON)} = 123 \text{ m}\Omega @ V_{GS} = 4.5 \text{ V}$
 $R_{DS(ON)} = 140 \text{ m}\Omega @ V_{GS} = 3.0 \text{ V}$
 $R_{DS(ON)} = 163 \text{ m}\Omega @ V_{GS} = 2.5 \text{ V}$
- Low profile – 0.8 mm maximum – in the new package MicroFET 2x2 mm
- HBM ESD protection level = 1.8kV (Note 3)
- RoHS Compliant



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	± 12	V
I_D	Drain Current – Continuous ($T_C = 25^\circ\text{C}$, $V_{GS} = 4.5\text{V}$)	2.9	A
	– Continuous ($T_C = 25^\circ\text{C}$, $V_{GS} = 2.5\text{V}$)	2.7	
	– Pulsed	10	
P_D	Power Dissipation for Single Operation (Note 1a)	1.5	W
	Power Dissipation for Single Operation (Note 1b)	0.65	
T_J, T_{STG}	Operating and Storage Temperature	-55 to $+150$	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	83 (Single Operation)	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1b)	193 (Single Operation)	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1c)	68 (Dual Operation)	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1d)	145 (Dual Operation)	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
002	FDMA2002NZ	7"	8mm	3000 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C		25		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate–Body Leakage Current	$V_{GS} = \pm 12\text{ V}, V_{DS} = 0\text{ V}$			± 10	μA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	0.4	1.0	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C		–3		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 4.5\text{ V}, I_D = 2.9\text{ A}$		75	123	m Ω
		$V_{GS} = 3.0\text{ V}, I_D = 2.7\text{ A}$		84	140	
		$V_{GS} = 2.5\text{ V}, I_D = 2.5\text{ A}$		92	163	
		$V_{GS} = 4.5\text{ V}, I_D = 2.9\text{ A}, T_C = 85^\circ\text{C}$		95	166	
		$V_{GS} = 3.0\text{ V}, I_D = 2.7\text{ A}, T_C = 150^\circ\text{C}$		138	203	
		$V_{GS} = 2.5\text{ V}, I_D = 2.5\text{ A}, T_C = 150^\circ\text{C}$		150	268	

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		190	220	pF
C_{oss}	Output Capacitance			30	40	pF
C_{rss}	Reverse Transfer Capacitance			20	30	pF

Switching Characteristics (Note 2)

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 15\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 4.5\text{ V}, R_{GEN} = 6\text{ }\Omega$		6	12	ns
t_r	Turn–On Rise Time			8	16	ns
$t_{d(off)}$	Turn–Off Delay Time			12	21	ns
t_f	Turn–Off Fall Time			2	10	ns
Q_g	Total Gate Charge	$V_{DS} = 15\text{ V}, I_D = 2.9\text{ A},$ $V_{GS} = 4.5\text{ V}$		2.4	3.0	nC
Q_{gs}	Gate–Source Charge			0.35		nC
Q_{gd}	Gate–Drain Charge			0.75		nC

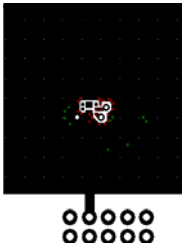

Drain–Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain–Source Diode Forward Current			2.9	A
V_{SD}	Drain–Source Diode Forward Voltage	$I_S = 2.0\text{ A}$		0.9	1.2
		$I_S = 1.1\text{ A}$		0.8	1.2
t_{rr}	Diode Reverse Recovery Time	$I_F = 2.9\text{ A},$		10	ns
Q_{rr}	Diode Reverse Recovery Charge	$di_F/dt = 100\text{ A}/\mu\text{s}$		2	nC

Electrical Characteristics

T_A = 25°C unless otherwise noted

- Notes:**
1. R_{θJA} is determined with the device mounted on a 1 in² oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{θJC} is guaranteed by design while R_{θJA} is determined by the user's board design.
- (a) R_{θJA} = 83°C/W when mounted on a 1 in² pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB
- (b) R_{θJA} = 193°C/W when mounted on a minimum pad of 2 oz copper
- (c) R_{θJA} = 68°C/W when mounted on a 1 in² pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB
- (d) R_{θJA} = 145°C/W when mounted on a minimum pad of 2 oz copper

	a) 83°C/W when mounted on a 1 in ² pad of 2 oz copper		b) 193°C/W when mounted on a minimum pad of 2 oz copper
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Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%
3. The diode connected between the gate and source serves only protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics

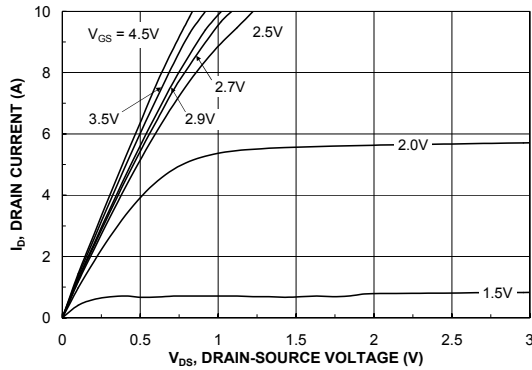


Figure 1. On-Region Characteristics.

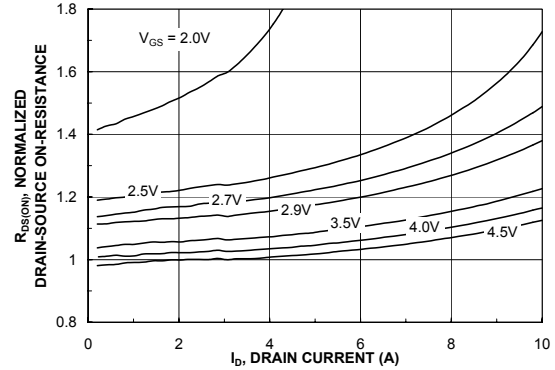


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

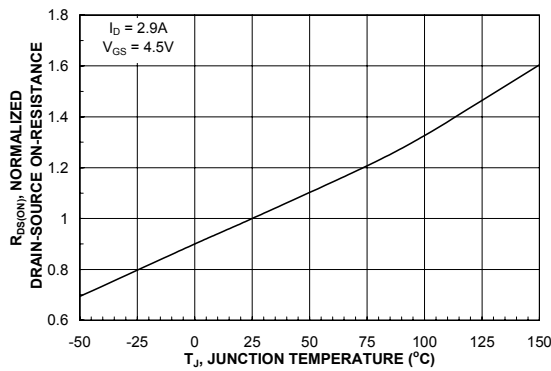


Figure 3. On-Resistance Variation with Temperature.

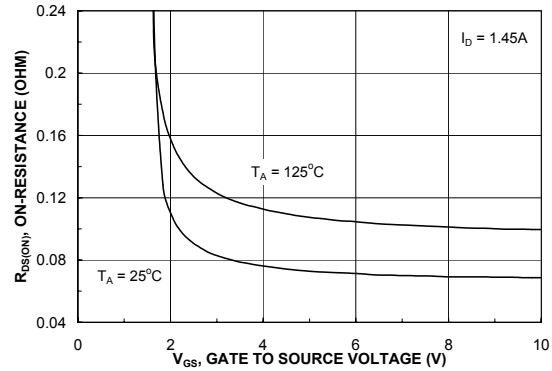


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

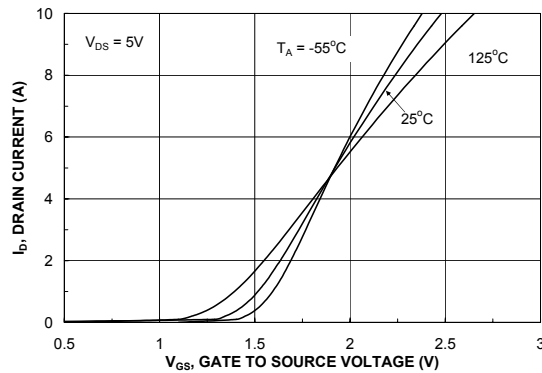


Figure 5. Transfer Characteristics.

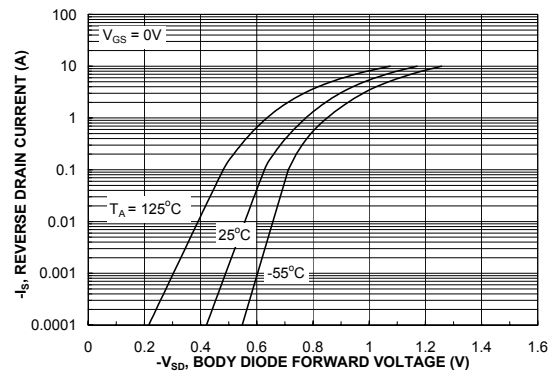
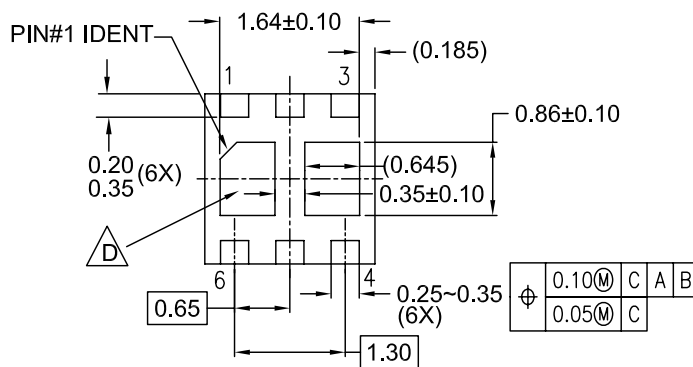
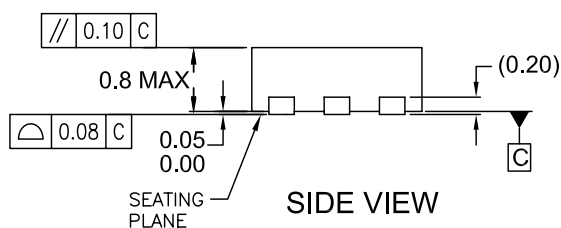
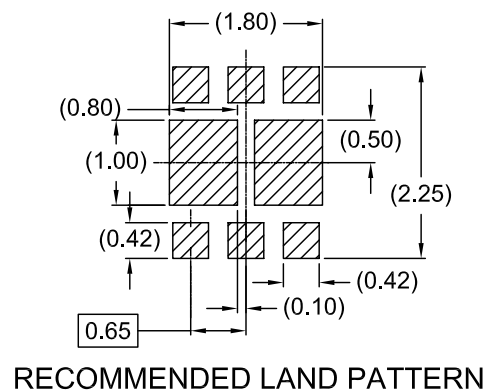
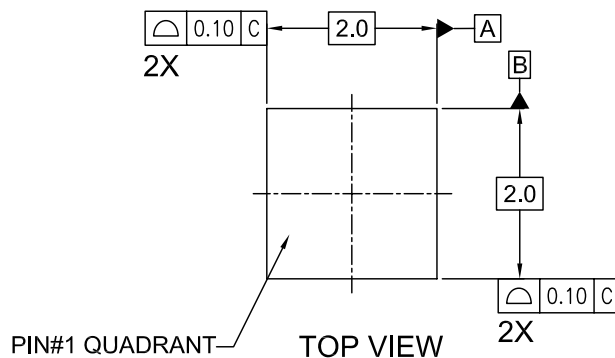


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Dimensional Outline and Pad Layout








NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-229, VARIATION VCCC EXCEPT AS NOTED.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- D. NON-JEDEC DUAL DAP
- E. DRAWING FILE NAME : MLP06Jrev3



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