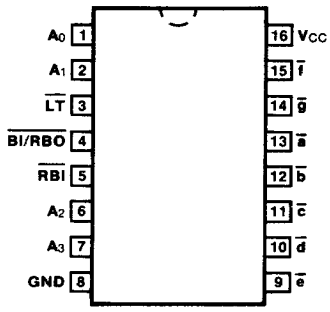
54/7446A • 54/7447A
54LS/74LS47

BCD TO 7-SEGMENT DECODER/DRIVER

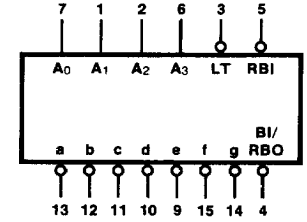
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '46A, '47A and 'LS47 accept four lines of BCD (8421) input data, generate their complements internally and decode the data with seven AND/OR gates having open-collector outputs to drive indicator segments directly. Each segment output is guaranteed to sink 40 mA (24 mA for the 'LS47) in the ON (LOW) state and withstand 15 V (30 V for the '46A) in the OFF (HIGH) state with a maximum leakage current of 250 μA. Auxiliary inputs provide blanking, lamp test and cascadable zero-suppression fuctions. Also see the 'LS247 data sheet.

- **OPEN-COLLECTOR OUTPUTS**
- **DRIVE INDICATOR SEGMENTS DIRECTLY**
- **CASCADABLE ZERO-SUPPRESSION CAPABILITY**
- **LAMP TEST INPUT**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7446APC, 7447APC 74LS47PC		9B
Ceramic DIP)D)	A	7446ADC, 7447ADC 74LS47DC	5446ADM, 5447ADM 54LS47DM	7B
Flatpak (F)	A	7446AFC, 7447AFC 74LS47FC	5446AFM, 5447AFM 54LS47FM	4L

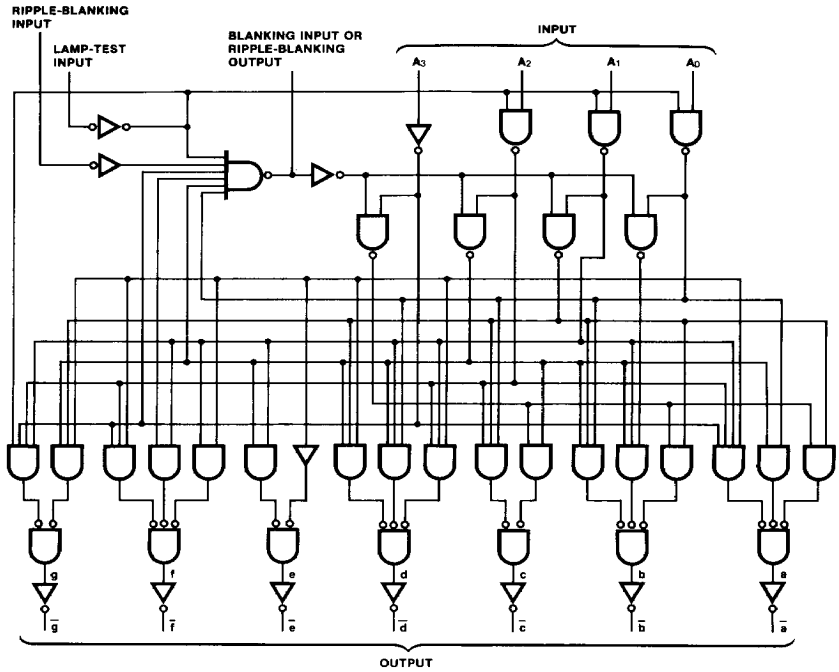
INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$\overline{A_0} - A_3$	BCD Inputs	1.0/1.0	0.5/0.25
$\overline{RBI}$	Ripple Blanking Input (Active LOW)	1.0/1.0	0.5/0.25
$\overline{LT}$	Lamp Test Input (Active LOW)	1.0/1.0	0.5/0.25
$\overline{BI/RBO}$	Blanking Input (Active LOW) or Ripple Blanking Output (Active LOW)	-/2.5 5.0/5.0	-/0.75 1.25/2.0 (1.0)
$\overline{a} - \overline{g}$	Segment Outputs (Active LOW)	OC*/25	OC*/15 (7.5)

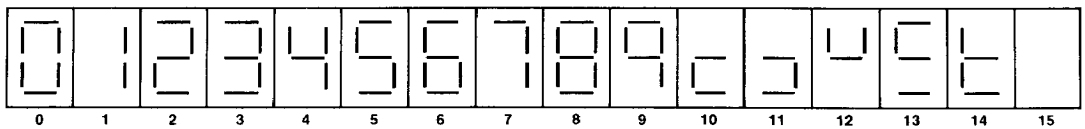
*OC — Open Collector

FUNCTIONAL DESCRIPTION — The '46A, '47A and 'LS47 decode the input data in the pattern indicated in the Truth Table and the segment identification illustration. If the input data is decimal zero, a LOW signal applied to the $\overline{RBI}$ blanks the display and causes a multidigit display. For example, by grounding the $\overline{RBI}$ of the highest order decoder and connecting its $\overline{BI/RBO}$ to $\overline{RBI}$ of the next lowest order decoder, etc., leading zeros will be suppressed. Similarly, by grounding $\overline{RBI}$ of the lowest order decoder and connecting its $\overline{BI/RBO}$ to $\overline{RBI}$ of the next highest order decoder, etc., trailing zeros will be suppressed. Leading and trailing zeros can be suppressed simultaneously by using external gates, ie: by driving $\overline{RBI}$ of an intermediate decoder from an OR gate whose inputs are $\overline{BI/RBO}$ of the next highest and lowest order decoders. BI/RBO also serves as an unconditional blanking input. The internal NAND gate that generates the $\overline{RBO}$ signal has a resistive pull-up, as opposed to a totem pole, and thus $\overline{BI/RBO}$ can be forced LOW by enternal means, using wired-collector logic. A LOW signal thus applied to $\overline{BI/RBO}$ turns off all segment outputs. This blanking feature can be used to control display intensity by varying the duty cycle of the blanking signal. A LOW signal applied to $\overline{LT}$ turns on all segment outputs, provided that $\overline{BI/RBO}$ is not forced LOW.

LOGIC DIAGRAM



NUMERICAL DESIGNATIONS — RESULTANT DISPLAYS



TRUTH TABLE

DECIMAL OR FUNCTION	INPUTS							OUTPUTS							NOTE
	$\overline{LT}$	$\overline{RBI}$	A_3	A_2	A_1	A_0	$\overline{BI/RBO}$	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	1
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	1
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
$\overline{BI}$	X	X	X	X	X	X	L	H	H	H	H	H	H	H	2
$\overline{RBI}$	H	L	L	L	L	L	L	H	H	H	H	H	H	H	3
$\overline{LT}$	L	X	X	X	X	X	H	L	L	L	L	L	L	L	4

NOTES:

(1) $\overline{BI/RBO}$ is wire-AND logic serving as blanking input ($\overline{BI}$) and/or ripple-blanking output ($\overline{RBO}$). The blanking out ($\overline{BI}$) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ($\overline{RBI}$) must be open or at a HIGH level if blanking or a decimal 0 is not desired. X = input may be HIGH or LOW.

(2) When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a HIGH level regardless of the state of any other input condition.

(3) When ripple-blanking input ($\overline{RBI}$) and inputs A_0, A_1, A_2 and A_3 are LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output ($\overline{RBO}$) goes to a LOW level (response condition).

(4) When the blanking input/ripple-blanking output ($\overline{BI/RBO}$) is open or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a LOW level.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
I_{OH}	Output HIGH Current	'46		250			μA	V_{OH} = 30 V	V_{CC} = Max
	OFF State at $\overline{a}$—$\overline{g}$	'47		250		250		V_{OH} = 15 V	
I_{OS}	Output Short Circuit Current at $\overline{BI/RBO}$			-4.0	-0.3	-2.0	mA	V_{CC} = Max	
I_{CC}	Power Supply Current	XM		85		13	mA	V_{CC} = Max	
		XC		103		13			

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 120 Ω Min	54/74 C_L = 15 pF, R_L = 120 Ω Max	54/74LS C_L = 15 pF, R_L = 665 Ω Min	54/74LS C_L = 15 pF, R_L = 665 Ω Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay A_n to $\overline{a}$—$\overline{g}$		100 100		100 100	ns	Figs. 3-2, 3-20
t_{PLH} t_{PHL}	Propagation Delay $\overline{RBI}$ to $\overline{a}$—$\overline{f}$		100 100		100 100	ns	Figs. 3-2, 3-4 $\overline{LT}$ = HIGH, A_0 - A_3 = LOW