

SN74F112

DUAL NEGATIVE-EDGE-TRIGGERED J-K FLIP-FLOP WITH CLEAR AND PRESET

SDFS048A – D2932, MARCH 1987 – REVISED OCTOBER 1993

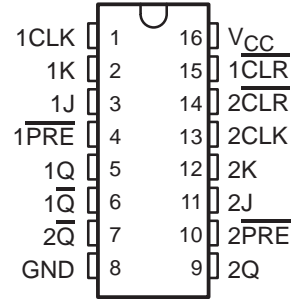
- Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs

description

The SN74F112 contains two independent J-K negative-edge-triggered flip-flops. A low level at the preset ($\overline{\text{PRE}}$) or clear ($\overline{\text{CLR}}$) inputs sets or resets the outputs regardless of the levels of the other inputs. When $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are inactive (high), data at the J and K inputs meeting the setup time requirements is transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. The SN74F112 can perform as a toggle flip-flop by tying J and K high.

The SN74F112 is characterized for operation from 0°C to 70°C.

D OR N PACKAGE (TOP VIEW)



FUNCTION TABLE

| INPUTS | | | | | OUTPUTS | |
|-------------------------|-------------------------|-----|---|---|----------------|-------------------------|
| $\overline{\text{PRE}}$ | $\overline{\text{CLR}}$ | CLK | J | K | Q | $\overline{\text{Q}}$ |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H [†] | H [†] |
| H | H | ↓ | L | L | Q ₀ | $\overline{\text{Q}}_0$ |
| H | H | ↓ | H | L | H | L |
| H | H | ↓ | L | H | L | H |
| H | H | ↓ | H | H | Toggle | |
| H | H | H | X | X | Q ₀ | $\overline{\text{Q}}_0$ |

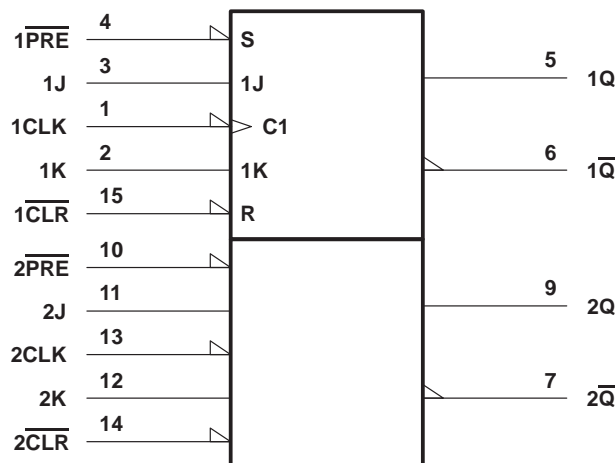
[†] The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH}. Furthermore, this configuration is nonstable; that is, it will not persist when either $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ returns to its inactive (high) level.

SN74F112

DUAL NEGATIVE-EDGE-TRIGGERED J-K FLIP-FLOP WITH CLEAR AND PRESET

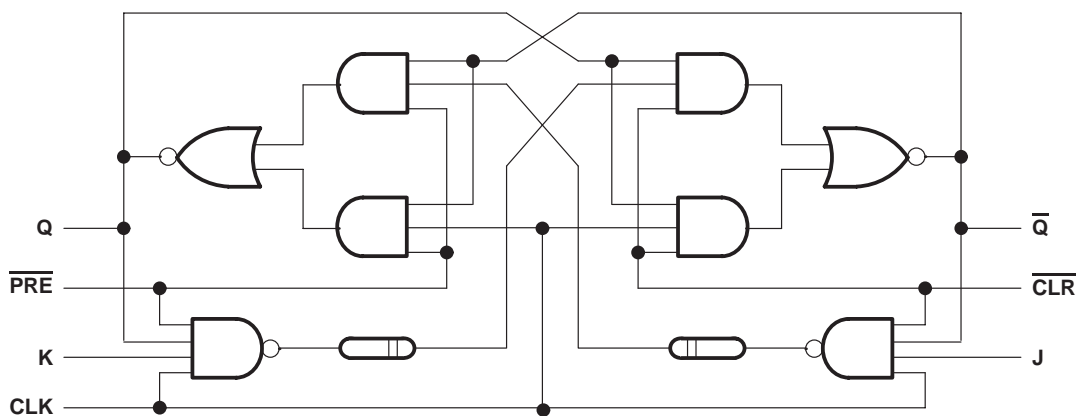
SDFS048A – D2932, MARCH 1987 – REVISED OCTOBER 1993

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each flip-flop (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

| | |
|---|--------------------|
| Supply voltage range, V_{CC} | –0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | –1.2 V to 7 V |
| Input current range | –30 mA to 5 mA |
| Voltage range applied to any output in the high state | –0.5 V to V_{CC} |
| Current into any output in the low state | 40 mA |
| Operating free-air temperature range | 0°C to 70°C |
| Storage temperature range | –65°C to 150°C |

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

SN74F112

DUAL NEGATIVE-EDGE-TRIGGERED J-K FLIP-FLOP WITH CLEAR AND PRESET

SDFS048A – D2932, MARCH 1987 – REVISED OCTOBER 1993

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|----------|--------------------------------|-----|-----|-----|------|
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | | V |
| V_{IL} | Low-level input voltage | | | 0.8 | V |
| I_{IK} | Input clamp current | | | –18 | mA |
| I_{OH} | High-level output current | | | –1 | mA |
| I_{OL} | Low-level output current | | | 20 | mA |
| T_A | Operating free-air temperature | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|-------------------|--|----------------------------|-------------------------|-----|------|------|------|
| V_{IK} | | $V_{CC} = 4.5\text{ V}$, | $I_I = -18\text{ mA}$ | | | –1.2 | V |
| V_{OH} | | $V_{CC} = 4.5\text{ V}$, | $I_{OH} = -1\text{ mA}$ | 2.5 | 3.4 | | V |
| | | $V_{CC} = 4.75\text{ V}$, | $I_{OH} = -1\text{ mA}$ | 2.7 | | | |
| V_{OL} | | $V_{CC} = 4.5\text{ V}$, | $I_{OL} = 20\text{ mA}$ | | 0.3 | 0.5 | V |
| I_I | | $V_{CC} = 5.5\text{ V}$, | $V_I = 7\text{ V}$ | | 0.1 | | mA |
| I_{IH} | | $V_{CC} = 5.5\text{ V}$, | $V_I = 2.7\text{ V}$ | | 20 | | µA |
| I_{IL} | J or K | $V_{CC} = 5.5\text{ V}$, | $V_I = 0.5\text{ V}$ | | | –0.6 | mA |
| | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ | | | | | –3 | |
| | CLK | | | | | –2.4 | |
| I_{OS}^\ddagger | | $V_{CC} = 5.5\text{ V}$, | $V_O = 0$ | –60 | | –150 | mA |
| I_{CC} | | $V_{CC} = 5.5\text{ V}$, | See Note 2 | | 12 | 19 | mA |

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: I_{CC} is measured with all outputs open, the Q and \overline{Q} outputs alternately high and the clock input grounded at the time of measurement.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | | | $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ | | MIN | MAX | UNIT |
|--------------------|---|---|---|-----|-----|-----|------|
| | | | MIN | MAX | | | |
| f_{clock} | Clock frequency | | 0 | 110 | 0 | 100 | MHz |
| t_w | Pulse duration | CLK high or low | 4.5 | | 5 | | ns |
| | | $\overline{\text{CLR}}$ or $\overline{\text{PRE}}$ low | 4.5 | | 5 | | |
| t_{su} | Setup time, data before CLK↓ | High | 4 | | 5 | | ns |
| | | Low | 3 | | 3.5 | | |
| t_h | Hold time, data after CLK↓ | High | 0 | | 0 | | ns |
| | | Low | 0 | | 0 | | |
| t_{su} | Setup time, inactive state, data before CLK↓§ | $\overline{\text{CLR}}$ or $\overline{\text{PRE}}$ high | 4 | | 5 | | ns |

§ Inactive-state setup time is also referred to as recovery time.

SN74F112

DUAL NEGATIVE-EDGE-TRIGGERED J-K FLIP-FLOP WITH CLEAR AND PRESET

SDFS048A – D2932, MARCH 1987 – REVISED OCTOBER 1993

switching characteristics (see Note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 5 V, C _L = 50 pF, R _L = 500 Ω, T _A = 25°C | | | V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX† | | UNIT |
|------------------|--|----------------|---|-----|-----|---|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | |
| f _{max} | | | 110 | 130 | | 100 | | MHz |
| t _{PLH} | CLK | Q or \bar{Q} | 1.2 | 4.6 | 6.5 | 1.2 | 7.5 | ns |
| t _{PHL} | | | 1.2 | 4.6 | 6.5 | 1.2 | 7.5 | |
| t _{PLH} | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ | Q or \bar{Q} | 1.2 | 4.1 | 6.5 | 1.2 | 7.5 | ns |
| t _{PHL} | | | 1.2 | 4.1 | 6.5 | 1.2 | 7.5 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 3: Load circuits and waveforms are shown in Section 1.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| SN74F112D | Obsolete | Production | SOIC (D) 16 | - | - | Call TI | Call TI | 0 to 70 | F112 |
| SN74F112DR | Active | Production | SOIC (D) 16 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | F112 |
| SN74F112DR.A | Active | Production | SOIC (D) 16 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | F112 |
| SN74F112N | Active | Production | PDIP (N) 16 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74F112N |
| SN74F112N.A | Active | Production | PDIP (N) 16 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74F112N |
| SN74F112NE4 | Active | Production | PDIP (N) 16 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74F112N |
| SN74F112NSR | Active | Production | SOP (NS) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74F112 |
| SN74F112NSR.A | Active | Production | SOP (NS) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74F112 |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74F112DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74F112NSR | SOP | NS | 16 | 2000 | 330.0 | 16.4 | 8.1 | 10.4 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74F112DR | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |
| SN74F112NSR | SOP | NS | 16 | 2000 | 353.0 | 353.0 | 32.0 |

TUBE



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74F112N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74F112N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74F112N.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74F112N.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74F112NE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74F112NE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |

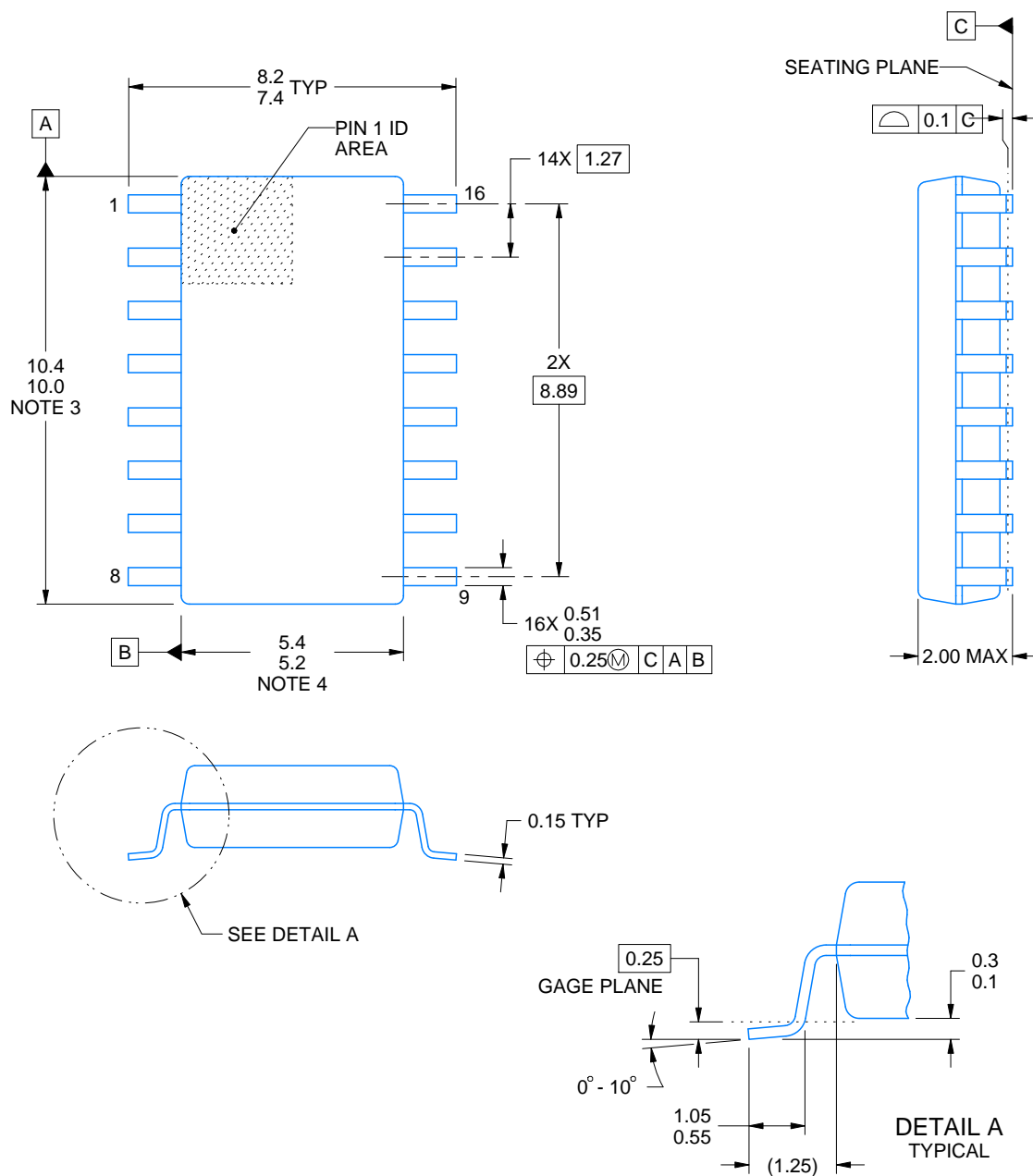


NS0016A

PACKAGE OUTLINE

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 E. Reference JEDEC MS-012 variation AC.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



| PINS ** DIM | 14 | 16 | 18 | 20 |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS-001 VARIATION | AA | BB | AC | AD |



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated