SN54AS195, SN74AS195
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

D2661, DECEMBER 1983 – REVISED MAY 1986

- Parallel-to-Serial, Serial-to-Parallel Conversions
- Parallel Synchronous Loading
- J and $\overline{K}$ Inputs to First Stage
- Right-Shift Only with Complementary Outputs on Last Stage
- Direct Overriding Clear
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 4-bit registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation:

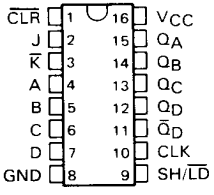
Parallel (broadside) load
Shift (in the direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading serial data flow is inhibited.

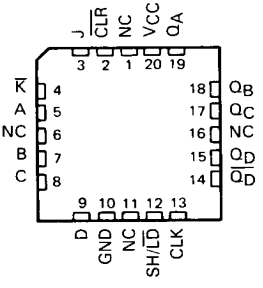
Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D-, or T-type flip-flop as shown in the function table.

The SN54AS195 is characterized for operation over the full military range of −55°C to 125°C. The SN74AS195 is characterized for operation from 0°C to 70°C.

SN54AS195 . . . J PACKAGE
SN74AS195 . . . D OR N PACKAGE
(TOP VIEW)



SN54AS195 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

2 ALS and AS Circuits

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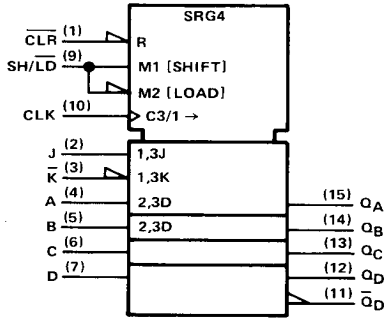
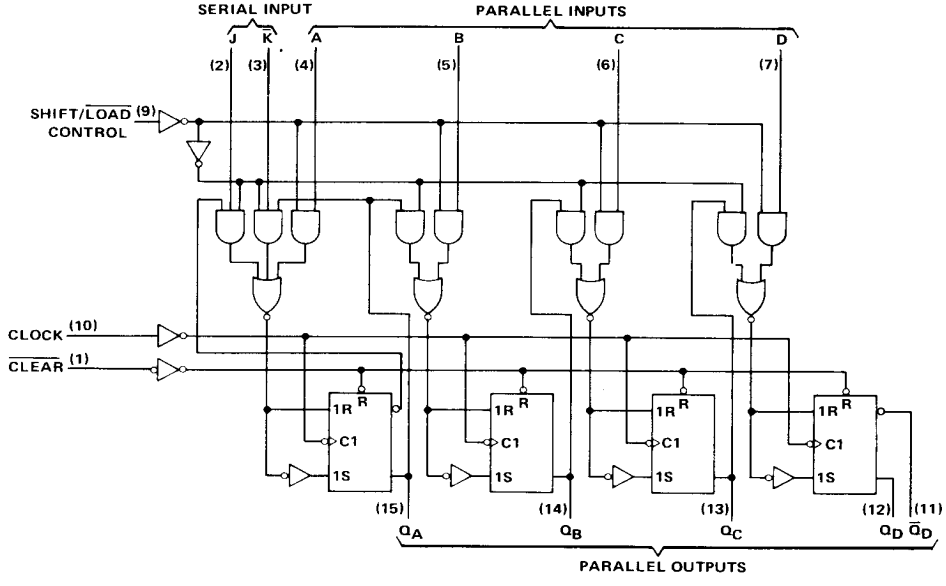
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



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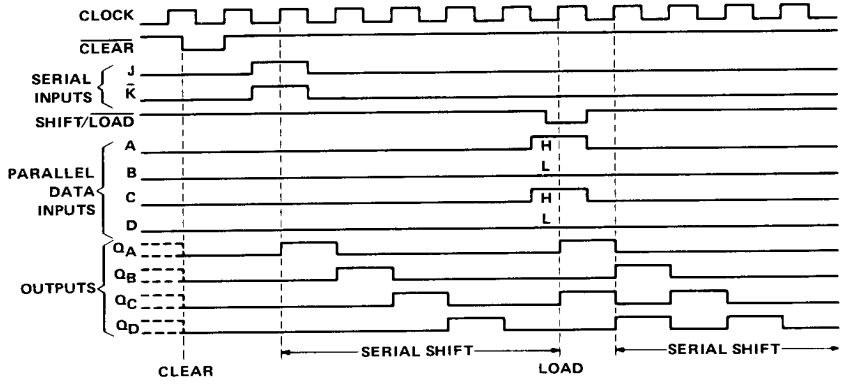
FUNCTION TABLE

INPUTS									OUTPUTS				
$\overline{CLEAR}$	SHIFT/$\overline{LOAD}$	CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

typical clear, shift, and load sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS195 . . . . . −55°C to 125°C
SN74AS195 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS195			SN74AS195			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0		60	0		70	MHz
t_w	Pulse duration	CLK high	4			4			ns
		$\overline{CLR}$ low	4			4			
t_{su}	Setup time	Data before CLK↑	4			3.5			ns
		SH/$\overline{LD}$ before CLK↑	9			8			
		$\overline{CLR}$ high before CLK↑	6.5			6			
t_h	Hold time	Data after CLK↑	1			0.5			ns
		SH/$\overline{LD}$ after CLK↑	0			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS195			SN74AS195			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	SH/$\overline{LD}$	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	All others					0.1			0.1	
I_{IH}	SH/$\overline{LD}$	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	All others					20			20	
I_{IL}	SH/$\overline{LD}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	All others					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}		V_{CC} = 5.5 V			32	51		32	51	mA
I_{CCL}		V_{CC} = 5.5 V			36	57		36	57	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS195		SN74AS195		
			MIN	MAX	MIN	MAX	
f_{max}			60		70		MHz
t_{PLH}	CLK	Any Q	3	10	3	8.5	ns
t_{PHL}			2.5	11.5	2.5	10.5	
t_{PLH}	$\overline{CLR}$	$\overline{Q}_D$	4	9.5	4	8	ns
t_{PHL}		Q_A thru Q_D	5	13	5	11.5	

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.