

ISOFACE™

ISO1H801G

Coreless Transformer Isolated
Digital Output 8 Channel 0.625A
High-Side Switch

Power Management & Drives



Never stop thinking.

ISO1H801G**Revision History:****2009-09-16****Version 2.3**

Previous Version: V2.2

V2.0 | Final Datasheet

V2.1 | Final Datasheet

V2.2 | Page 15 creepage, clearance distance and V_{ISO} adapted,

V2.3 | Diagnostic output discontinued

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Coreless Transformer Isolated Digital Output 8 Channel 0.625A High-Side Switch

Product Highlights

- Coreless transformer isolated data interface
- Galvanic isolation
- 8 High-side output switches 0.625A
- µC compatible 8-bit parallel peripheral



Features

- Interface 5V CMOS operation compatible
- Parallel interface
- Direct control mode
- High common mode transient immunity
- Short circuit protection
- Maximum current internally limited
- Overload protection
- Overtoltage protection (including load dump)
- Undervoltage shutdown with autorestart and hysteresis
- Switching inductive loads
- Common output disable pin
- Thermal shutdown with restart
- Thermal independence of separate channels
- ESD protection
- Loss of GND_{bb} and loss of V_{bb} protection
- Reverse Output Voltage protection

- Isolated switch for industrial applications (PLC)
- All types of resistive, inductive and capacitive loads
- µC compatible power switch for 24V DC applications
- Driver for solenoid, relays and resistive loads

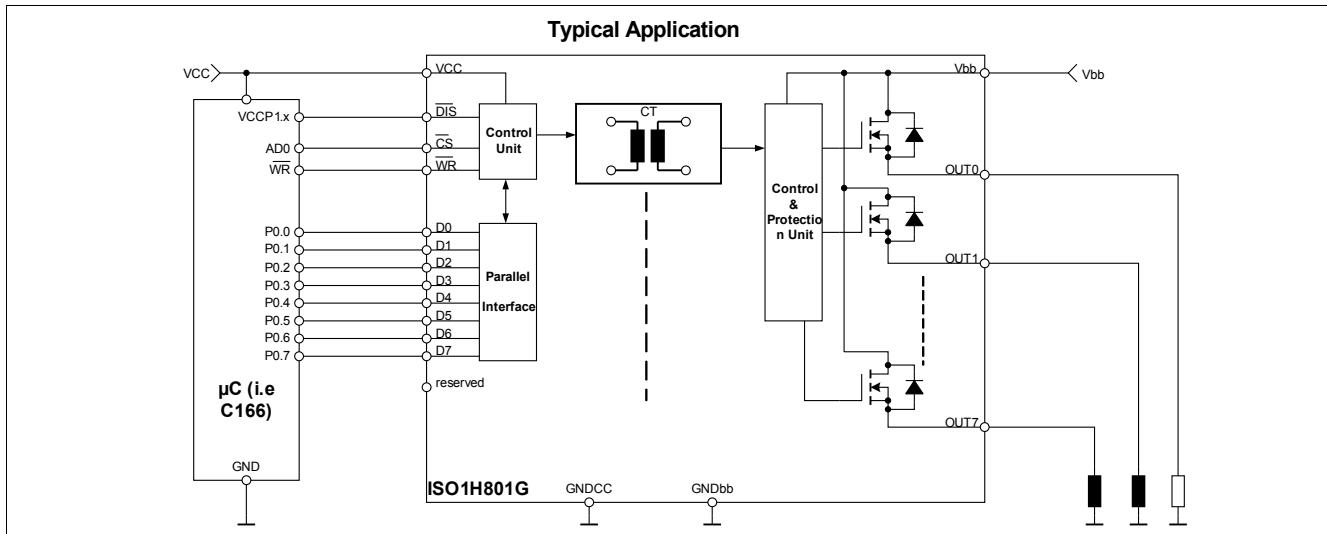
Description

The ISO1H801G is a galvanically isolated 8 bit data interface in PG-DSO-36 package that provides 8 fully protected high-side power switches that are able to handle currents up to 625 mA.

An 8 bit parallel µC compatible interface allows to connect the IC directly to a µC system. The input interface supports also a direct control mode and is designed to operate with 5V CMOS compatible levels.

The data transfer from input to output side is realized by the integrated Coreless Transformer Technology.

Typical Application



| Type | | On-state Resistance | Package |
|-----------|--|---------------------|-----------|
| ISO1H801G | | 200mΩ | PG-DSO-36 |

1 Pin Configuration and Functionality

1.1 Pin Configuration

| Pin | Symbol | Function |
|-----|------------|--------------------------------------|
| 1 | N.C. | Not connected |
| 2 | VCC | Positive 5V logic supply |
| 3 | <u>DIS</u> | Output disable |
| 4 | <u>CS</u> | Chip select |
| 5 | <u>WR</u> | Parallel write |
| 6 | D0 | Data input bit0 |
| 7 | D1 | Data input bit1 |
| 8 | D2 | Data input bit2 |
| 9 | D3 | Data input bit3 |
| 10 | D4 | Data input bit4 |
| 11 | D5 | Data input bit5 |
| 12 | D6 | Data input bit6 |
| 13 | D7 | Data input bit7 |
| 14 | reserved | - |
| 15 | GNDCC | Input logic ground |
| 16 | N.C. | Not connected |
| 17 | N.C. | Not connected |
| 18 | N.C. | Not connected |
| 19 | GNDbb | Output driver ground |
| 20 | N.C. | Not connected |
| 21 | OUT7 | High-side output of channel 7 |
| 22 | OUT7 | High-side output of channel 7 |
| 23 | OUT6 | High-side output of channel 6 |
| 24 | OUT6 | High-side output of channel 6 |
| 25 | OUT5 | High-side output of channel 5 |
| 26 | OUT5 | High-side output of channel 5 |
| 27 | OUT4 | High-side output of channel 4 |
| 28 | OUT4 | High-side output of channel 4 |
| 29 | OUT3 | High-side output of channel 3 |
| 30 | OUT3 | High-side output of channel 3 |
| 31 | OUT2 | High-side output of channel 2 |
| 32 | OUT2 | High-side output of channel 2 |
| 33 | OUT1 | High-side output of channel 1 |
| 34 | OUT1 | High-side output of channel 1 |
| 35 | OUT0 | High-side output of channel 0 |
| 36 | OUT0 | High-side output of channel 0 |
| TAB | Vbb | Positive driver power supply voltage |

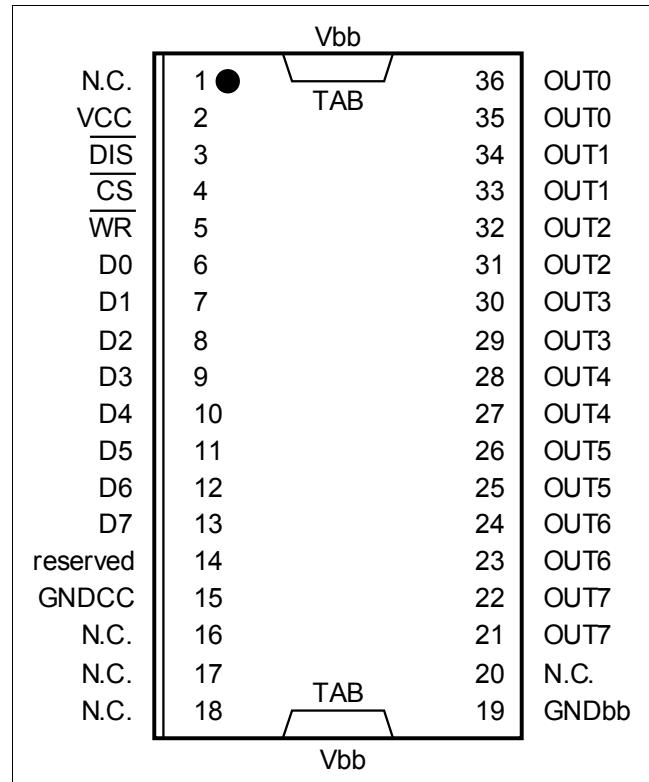


Figure 1 Power SO-36 (430mil)

1.2 Pin Functionality

VCC (Positive 5V logic supply)

The VCC supplies the input interface that is galvanically isolated from the output driver stage. The input interface can be supplied with 5V.

DIS (Output disable)

The high-side outputs OUT0...OUT7 can be immediately switched off by means of the low active pin DIS that is an asynchronous signal. The input registers are also reset by the DIS signal. The Output remains switched off after low-high transition of DIS signal, till new information is written into the input register. Current Sink to GNDCC.

CS (Chip select)

The system microcontroller selects the ISO1H801G by means of the low active pin CS to activate the parallel interface. By connecting the CS pin and WR pin to ground the parallel direct control is activated. Current Source to VCC.

WR (Parallel write)

In parallel mode data at the input pins (D0 ... D7) are latched by means of the rising edge of the low active signal WR (write). Current Source to VCC.

D0 ... D7 (Data input bit0 ... bit7)

The present data can be latched on the rising edge of the write signal WR. D0 ... D7 control the corresponding output channels OUT0 ...OUT7. By connecting CS and WR to ground, the signals at D0 ... D7 directly control the outputs. Current Sink to GNDCC.

GNDCC (Ground for VCC domain)

This pin acts as the ground reference for the input interface that is supplied by VCC.

GNDbb (Output driver ground domain)

This pin acts as the ground reference for the output driver that is supplied by Vbb.

OUT0 ... OUT7 (High side output channel 0 ... 7)

The output high side channels are internally connected to Vbb and controlled by the corresponding data input pins D0 ... D7 in parallel mode.

TAB (Vbb, Positive supply for output driver)

The heatslug is connected to the positive supply port of the output interface.

2

Blockdiagram

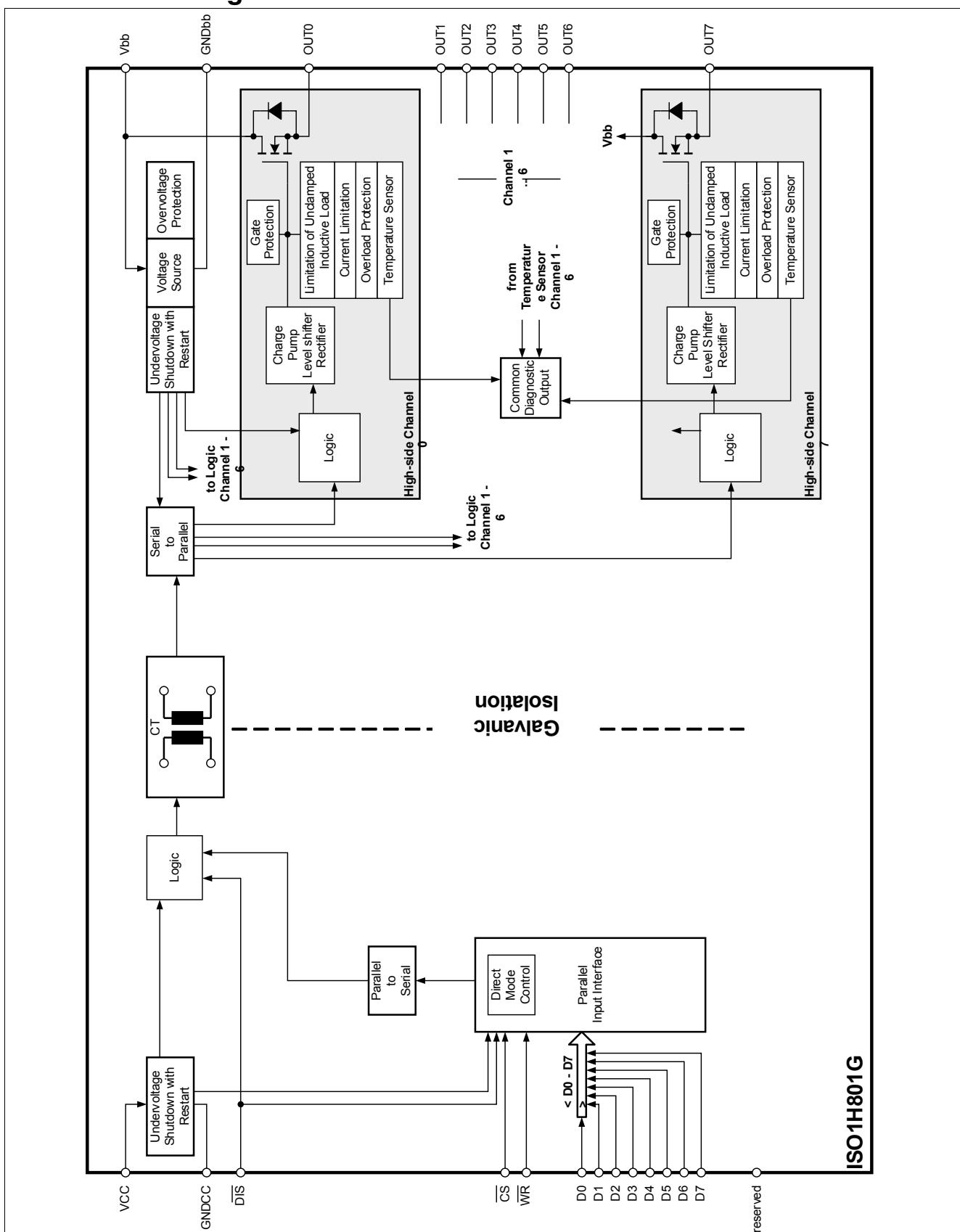


Figure 2 Blockdiagram

3 Functional Description

3.1 Introduction

The ISOFACE ISO1H801G includes 8 high-side power switches that are controlled by means of the integrated parallel interface. The interface is 8bit µC compatible. Furthermore a direct control mode can be selected that allows the direct control of the outputs OUT0...OUT7 by means of the inputs D0...D7 without any additional logic signal. The IC can replace 8 optocouplers and the 8 high-side switches in conventional I/O-Applications as a galvanic isolation is implemented by means of the integrated coreless transformer technology. The µC compatible interfaces allow a direct connection to the ports of a microcontroller without the need for other components. Each of the 8 high-side power switches is protected against short to V_{bb}, overload, overtemperature and against overvoltage by an active zener clamp.

The diagnostic logic on the power chip recognizes the overtemperature information of each power transistor.

3.2 Power Supply

The IC contains 2 galvanic isolated voltage domains that are independent from each other. The input interface is supplied at V_{CC} and the output stage is supplied at V_{bb}. The different voltage domains can be switched on at different time. The output stage is only enabled once the input stage enters a stable state.

3.3 Output Stage

Each channel contains a high-side vertical power FET that is protected by embedded protection functions.

The continuous current for each channel is 625mA (all channels ON).

3.3.1 Output Stage Control

Each output is independently controlled by an output latch and a common reset line via the pin DIS that disables all eight outputs and reset the latches. The parallel input data is transferred to the input latches with a high-to-low transition of the signal WR (write) while the CS is logic low. A low-to-high transition of CS transfers then the data of the input latches to the output buffer.

3.3.2 Power Transistor Overvoltage Protection

Each of the eight output stages has its own zener clamp that causes a voltage limitation at the power transistor

when solenoid loads are switched off. V_{ON} is then clamped to 47V (min.).

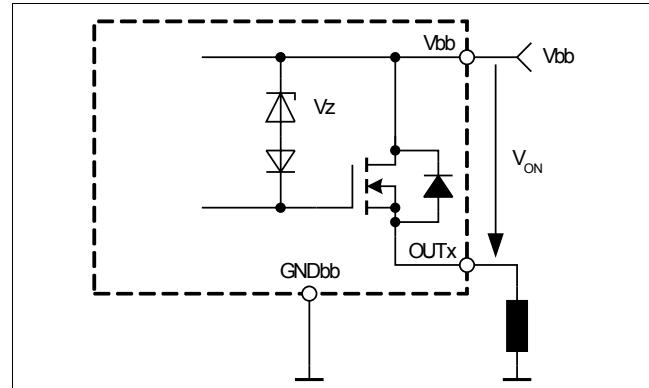


Figure 3 Inductive and overvoltage output clamp (each channel)

Energy is stored in the load inductance during an inductive load switch-off.

$$E_L = 1/2 \times L \times I_L^2$$

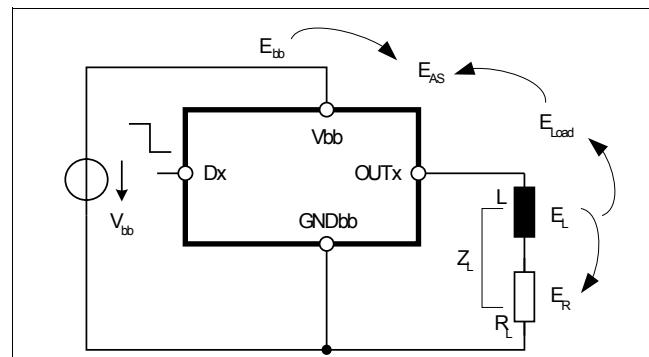


Figure 4 Inductive load switch-off energy dissipation (each channel)

While demagnetizing the load inductance, the energy dissipation in the DMOS is

$$E_{AS} = E_{bb} + E_L - E_R = V_{ON(CL)} \times i_L(t)dt$$

with an approximate solution for $R_L > 0\Omega$:

$$E_{AS} = \frac{I_L \times L}{2 \times R_L} \times (V_{bb} + |V_{ON(CL)}|) \times \ln\left(1 + \frac{I_L \times R_L}{|V_{ON(CL)}|}\right)$$

3.3.3 Power Transistor Overcurrent Protection

The outputs are provided with a current limitation that enters a repetitive switched mode after an initial peak current has been exceeded. The initial peak short circuit current limit is set to $I_{L(SCp)}$. During the repetitive mode short circuit current the limit is set to $I_{L(SCr)}$. If this operation leads to an overtemperature condition, a second protection level ($T_j > 135^\circ\text{C}$) will change the

output into a low duty cycle PWM (selective thermal shutdown with restart) to prevent critical chip temperatures.

3.4

Reserved

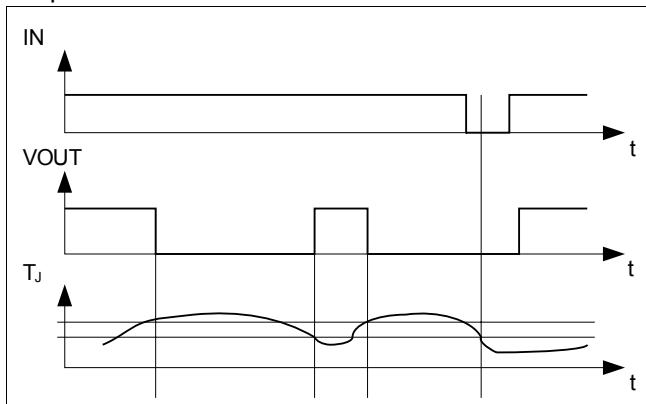


Figure 5 Overtemperature detection

The following figures show the timing for a turn on into short circuit and a short circuit in on-state. Heating up of the chip may require several milliseconds, depending on external conditions.

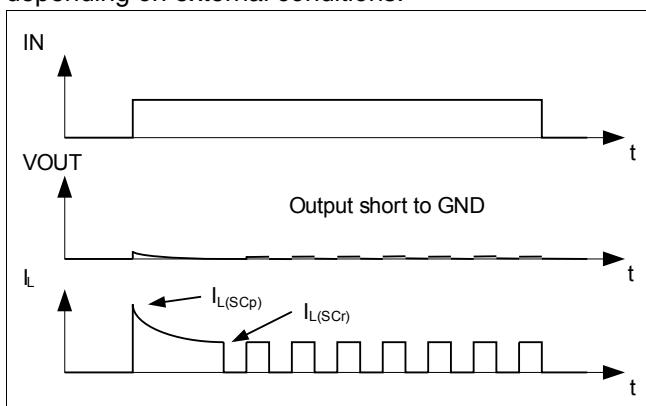


Figure 6 Turn on into short circuit, shut down by overtemperature, restart by cooling

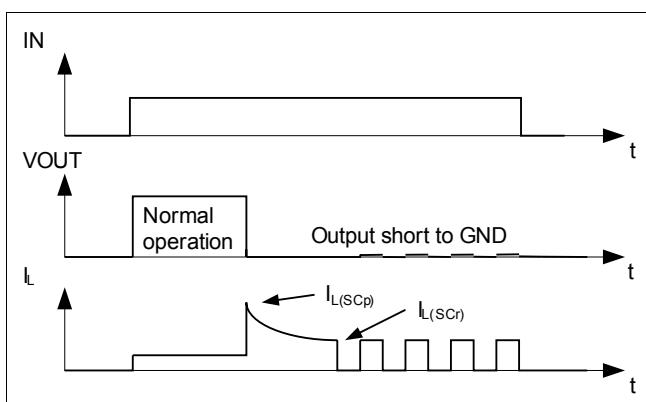


Figure 7 Short circuit in on-state, shut down by overtemperature, restart by cooling

3.5 Parallel Interface

The ISO1H801G contains a parallel interface that can be directly controlled by the microcontroller output ports. The parallel interface can also be switched over to a direct control that allows direct changes of the outputs OUT0 ... OUT7 by means of the corresponding inputs D0 ... D7 without additional logic signals. To activate the parallel direct control mode pin **CS** and pin **WR** have to be connected both to GNDCC.

3.5.1 Parallel Interface Signal Description

CS - Chip select. The system microcontroller selects the ISO1H801G by means of the **CS** pin. Whenever the pin is in a logic low state, data can be transferred from the µC.

CS High to low transition:

- Parallel input data can be written in from then on

CS Low to high transition:

- The data in the input latches is transferred to the output buffer

WR - Write. The system controller enables the write procedure in the ISO1H801G by means of the signal **WR**. A logic low state signal at pin **WR** writes the input data into the input latches when the **CS** pin is in a logic low state.

WR Logic low level:

- Parallel input data at the pins D0 - D7 is written into the input latches

WR Logic high level:

- The parallel input data is latched in the input latches. Any changes at the pins D0 - D7 after the low-to-high transition of **WR** do not affect the input latches.

D0 ... D7 - Parallel input. Parallel data bits are fed into the pins D0 ... D7. The data is written into the input latches when **WR** is logic low.

3.5.2 uC Control Mode

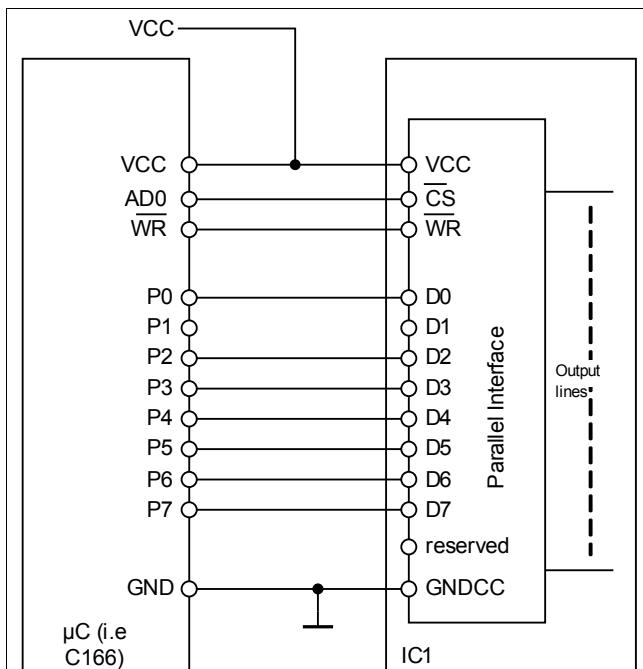


Figure 8 Parallel bus configuration

3.5.3 Direct Control Mode

Beside the use of the parallel µC compatible interface a parallel direct control mode can be chosen. In this mode the output OUT0...OUT7 can be directly controlled via the inputs D0...D7 without the need for additional logic signals. To activate this mode pin **CS** and **WR** need to be connected to GNDCC.

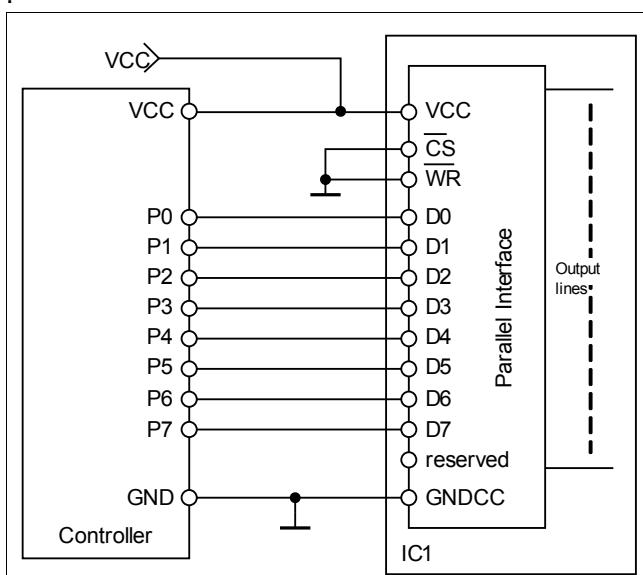


Figure 9 Parallel Direct Control

3.6 Parallel Interface Timing

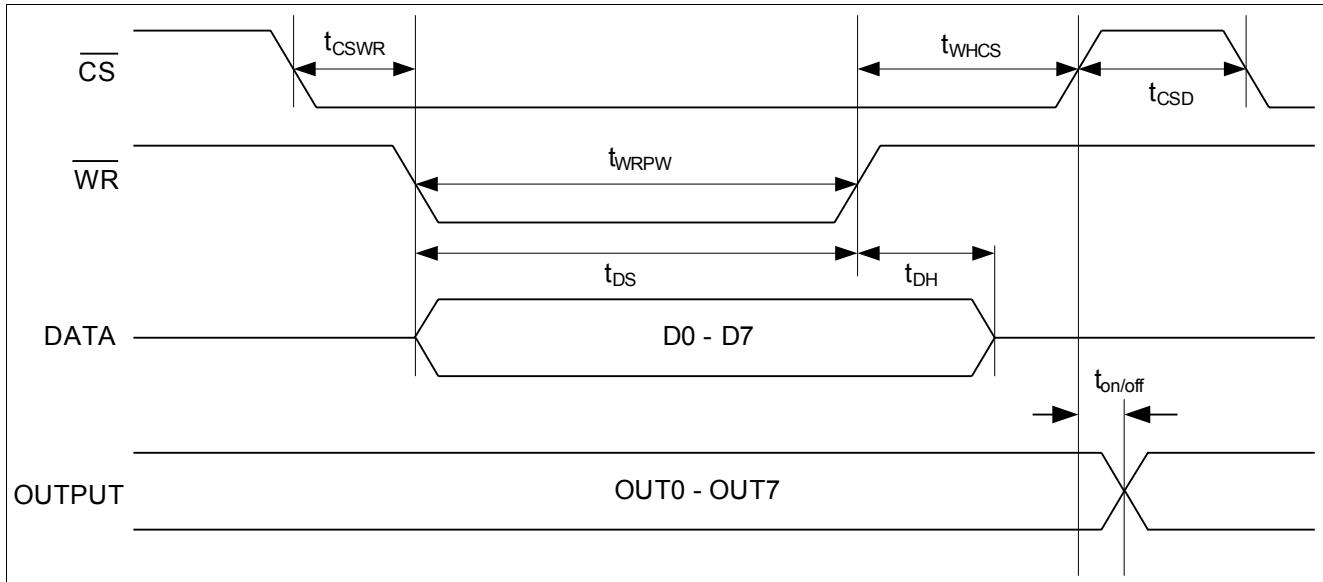


Figure 10 Parallel input - output timing diagram

3.7 Transmission Failure Detection

There is a failure detection unit integrated to ensure also a stable functionality during the integrated coreless transformer transmission. This unit decides whether the transmitted data is valid or not. If four times serial data coming in from the internal registers is not accepted, the output stages are switched off until the next valid data is received.

4 Electrical Characteristics

Note: All voltages at pins 2 to 14 are measured with respect to ground GNDCC (pin 15). All voltages at pin 20 to pin 36 and TAB are measured with respect to ground GNDbb (pin 19). The voltage levels are valid if other ratings are not violated. The two voltage domains V_{CC} and V_{bb} are internally galvanic isolated.

4.1 Absolute Maximum Ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. For the same reason make sure, that any capacitor that will be connected to pin 2 (VCC) and TAB (Vbb) is discharged before assembling the application circuit. Supply voltages higher than $V_{bb(AZ)}$ require an external current limit for the GNDbb pin, e.g. with a 15Ω resistor in GNDbb connection. Operating at absolute maximum ratings can lead to a reduced lifetime.

| Parameter | Symbol | Limit Values | | Unit |
|--|----------------|------------------|------------------|------------------|
| | | min. | max. | |
| at $T_j = -40 \dots 135^\circ\text{C}$, unless otherwise specified | | | | |
| Supply voltage input interface (VCC) | V_{CC} | -0.5 | 6.5 | |
| Supply voltage output interface (Vbb) | V_{bb} | -1 ¹⁾ | 45 | |
| Continuous voltage at data inputs (D0 ... D7) | V_{DX} | -0.5 | 6.5 | |
| Continuous voltage at pin CS | V_{CS} | -0.5 | 6.5 | |
| Continuous voltage at pin WR | V_{WR} | -0.5 | 6.5 | |
| Continuous voltage at pin DIS | V_{DIS} | -0.5 | 6.5 | |
| Continuous voltage at reserved pin | $V_{Reserved}$ | -0.5 | 6.5 | |
| Load current (short-circuit current) | I_L | — | self limited | A |
| Reverse current through GNDbb ¹⁾ | I_{GNDbb} | -1.6 | — | |
| Operating Temperature | T_j | -25 | internal limited | $^\circ\text{C}$ |
| Storage Temperature | T_{stg} | -50 | 150 | |
| Power Dissipation ²⁾ | P_{tot} | — | 3.3 | W |
| Inductive load switch-off energy dissipation ³⁾ single pulse, $T_j = 125^\circ\text{C}$, $I_L = 0.625\text{A}$ one channel active all channel simultaneously active (each channel) | E_{AS} | — | 10 1 | J |
| Load dump protection ³⁾ $V_{loadDump}^{4)} = V_A + V_S$ V_{IN} = low or high $t_d = 400\text{ms}$, $R_I = 2\Omega$, $R_L = 27\Omega$, $V_A = 13.5\text{V}$ $t_d = 350\text{ms}$, $R_I = 2\Omega$, $R_L = 57\Omega$, $V_A = 27\text{V}$ | $V_{Loaddump}$ | 90 117 | V | |
| Electrostatic discharge voltage (Human Body Model) according to JESD22-A114-B | V_{ESD} | 2 | | kV |
| Electrostatic discharge voltage (Charge Device Model) according to ESD STM5.3.1 - 1999 | V_{ESD} | 1 | | kV |
| Continuous reverse drain current ¹⁾³⁾ , each channel | I_S | — | 4 | A |

1) defined by P_{tot}

2) Device on 50mm*50mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical without blown air.

3) not subject to production test, specified by design

4) $V_{Loaddump}$ is setup without the DUT connected to the generator per ISO7637-1 and DIN40839

4.2 Thermal Characteristics

| Parameter at $T_j = -25 \dots 125^\circ\text{C}$, $V_{bb}=15\dots30\text{V}$, $V_{CC}=4.5\dots5.5\text{V}$, unless otherwise specified | Symbol | Limit Values | | | Unit | Test Condition |
|---|---------------|---------------------|-------------|-------------|-------------|-----------------------|
| | | min. | typ. | max. | | |
| Thermal resistance junction - case | R_{thJC} | — | — | 1.5 | K/W | |
| Thermal resistance @ min. footprint | $R_{th(JA)}$ | — | — | 50 | | |
| Thermal resistance @ 6cm ² cooling area ¹⁾ | $R_{th(JA)}$ | — | — | 38 | | |

1) Device on 50mm*50mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical without blown air.

4.3 Load Switching Capabilities and Characteristics

| Parameter at $T_j = -25 \dots 125^\circ\text{C}$, $V_{bb}=15\dots30\text{V}$, $V_{CC}=4.5\dots5.5\text{V}$, unless otherwise specified | Symbol | Limit Values | | | Unit | Test Condition |
|---|----------------|---------------------|-------------|-------------|------------------------|-----------------------|
| | | min. | typ. | max. | | |
| On-state resistance, $I_L = 0.5\text{A}$ $T_j = 25^\circ\text{C}$ $T_j = 125^\circ\text{C}$ | R_{ON} | — — | 150 270 | 200 320 | $\text{m}\Omega$ | |
| Turn-on time to 90% $V_{OUT}^{1)}$ $R_L = 47\Omega$, $V_{Dx} = 0$ to 5V | t_{on} | — | 64 | 120 | μs | |
| Turn-off time to 10% $V_{OUT}^{1)}$ $R_L = 47\Omega$, $V_{Dx} = 5$ to 0V | t_{off} | — | 89 | 170 | | |
| Slew rate on 10 to 30% V_{OUT} $R_L = 47\Omega$, $V_{bb} = 15\text{V}$ | dV/dt_{on} | — | 1 | 2 | $\text{V}/\mu\text{s}$ | |
| Slew rate off 70 to 40% V_{OUT} $R_L = 47\Omega$, $V_{bb} = 15\text{V}$ | $-dV/dt_{off}$ | — | 1 | 2 | | |

1) The turn-on and turn-off time includes the switching time of the high-side switch and the transmission time via the coreless transformer in normal operating mode. During a failure on the coreless transformer transmission turn-on or turn-off time can increase by up to 50 μs .

4.4 Operating Parameters

| Parameter at $T_j = -25 \dots 125^\circ\text{C}$, $V_{bb}=15\dots30\text{V}$, $V_{CC}=4.5\dots5.5\text{V}$, unless otherwise specified | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|-------------------------------|-------------|-------------|-------------------------|--------------------------------|
| | | min. | typ. | max. | | |
| Common mode transient immunity ¹⁾ | $\Delta V_{ISO}/dt$ | -25 | - | 25 | $\text{kV}/\mu\text{s}$ | $\Delta V_{ISO} = 200\text{V}$ |
| Magnetic field immunity ¹⁾ | H_{IM} | 100 | | | A/m | IEC61000-4-8 |
| V_{bb} (Output interface) | Undervoltage shutdown | $V_{bb(\text{under})}$ | 7 | — | 10.5 | V |
| | Undervoltage restart | $V_{bb(u_rst)}$ | — | — | 11 | |
| | Undervoltage hysteresis | $\Delta V_{bb(\text{under})}$ | — | 0.5 | — | |
| | Undervoltage current | $I_{bb(uvlo)}$ | — | 1 | 2.5 | mA |
| | Operating current | I_{GNDL} | — | 10 | 14 | mA |
| | Leakage output current (included in $I_{bb(\text{off})}$) $V_{Dx} = \text{low}$, each channel | $I_{L(\text{off})}$ | — | 5 | 30 | μA |

Electrical Characteristics

| | | | | | | | |
|--|-------------------------|-------------------------------|-----|-----|-----|----|-----------------|
| Voltage domain V_{CC} (Input interface) | Operating voltage | V_{CC} | 4.5 | — | 5.5 | V | $V_{CC} < 2.5V$ |
| | Undervoltage shutdown | $V_{CC(\text{under})}$ | 2.5 | — | 2.9 | | |
| | Undervoltage restart | $V_{CC(u_rst)}$ | — | — | 3 | | |
| | Undervoltage hysteresis | $\Delta V_{CC(\text{under})}$ | — | 0.1 | — | | |
| | Undervoltage current | $I_{CC(\text{uvlo})}$ | — | 1 | 2 | mA | |
| | Operating current | $I_{CC(\text{on})}$ | — | 4.5 | 6 | mA | |

1) not subject to production test

4.5 Output Protection Functions

| Parameter ¹⁾ at $T_j = -25 \dots 125^\circ\text{C}$, $V_{bb} = 15 \dots 30V$, $V_{CC} = 4.5 \dots 5.5V$, unless otherwise specified | Symbol | Limit Values | | | Unit | Test Condition |
|--|---------------------|--------------|------|------|------------------|----------------|
| | | min. | typ. | max. | | |
| Initial peak short circuit current limit, $V_{bb} = 30V$, $t_m = 700\mu\text{s}$ $T_j = -25^\circ\text{C}$ $T_j = 25^\circ\text{C}$ $T_j = 125^\circ\text{C}$ | $I_{L(\text{SCP})}$ | — | — | 1.9 | A | |
| | | — | 1.4 | — | | |
| | | 0.7 | — | — | | |
| Repetitive short circuit current limit ³⁾ $T_j = T_{jt}$ (see timing diagrams) | $I_{L(\text{SCR})}$ | — | 1.1 | — | | |
| Output clamp (inductive load switch off) at $V_{OUT} = V_{bb} - V_{ON(CL)}$ | $V_{ON(CL)}$ | 47 | 53 | 60 | V | |
| Overvoltage protection | $V_{bb(\text{AZ})}$ | 47 | — | — | | |
| Thermal overload trip temperature ²⁾³⁾ | T_{jt} | 135 | — | — | $^\circ\text{C}$ | |
| Thermal hysteresis ³⁾ | ΔT_{jt} | — | 10 | — | K | |

- 1) Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.
- 2) Higher operating temperature at normal function for each channel available
- 3) not subject to production test, specified by design

4.6 Reserved

4.7 Input Interface

| Parameter at $T_j = -25 \dots 125^\circ\text{C}$, $V_{bb}=15\dots30\text{V}$, $V_{CC}=4.5\dots5.5\text{V}$, unless otherwise specified | Symbol | Limit Values | | | Unit | Test Condition |
|--|---------------|---------------------|-------------|---------------------|---------------|-----------------------|
| | | min. | typ. | max. | | |
| Input low state voltage (D0 ... D7, $\overline{\text{DIS}}$, $\overline{\text{CS}}$, $\overline{\text{WR}}$) | V_{IL} | -0.3 | — | $0.3 \times V_{CC}$ | V | |
| Input high state voltage (D0 ... D7, $\overline{\text{DIS}}$, $\overline{\text{CS}}$, $\overline{\text{WR}}$) | V_{IH} | $0.7 \times V_{CC}$ | — | $V_{CC} + 0.3$ | | |
| Input voltage hysteresis (D0 ... D7, $\overline{\text{DIS}}$, $\overline{\text{CS}}$, $\overline{\text{WR}}$) | V_{IHys} | | 100 | | mV | |
| Input pull down current (D0 ... D7, $\overline{\text{DIS}}$) | I_{Idown} | | 100 | | μA | |
| Input pull up current ($\overline{\text{CS}}$, $\overline{\text{WR}}$) | $-I_{Iup}$ | | 100 | | | |
| Output disable time (transition $\overline{\text{DIS}}$ to logic low) ¹⁾²⁾ Normal operation Turn-off time to 10% V_{OUT} $R_L = 47\Omega$ | t_{DIS} | --- | 85 | 170 | μs | |
| Output disable time (transition $\overline{\text{DIS}}$ to logic low) ¹⁾²⁾³⁾ Disturbed operation Turn-off time to 10% V_{OUT} $R_L = 47\Omega$ | t_{DIS} | --- | --- | 230 | | |

- 1) The time includes the turn-on/off time of the high-side switch and the transmission time via the coreless transformer.
- 2) If Pin $\overline{\text{DIS}}$ is set to low the outputs are set to low; after $\overline{\text{DIS}}$ set to high a new write cycle is necessary to set the output again.
- 3) The parameter is not subject to production test - verified by design/characterization

4.8 Parallel Interface Input Timing

| Parameter at $T_j = -25 \dots 125^\circ\text{C}$, $V_{bb}=15\dots30\text{V}$, $V_{CC}=4.5\dots5.5\text{V}$, unless otherwise specified | Symbol | Limit Values | | | Unit | Test Condition |
|---|---------------|---------------------|-------------|-------------|-------------|-----------------------|
| | | min. | typ. | max. | | |
| WR pulse width | t_{WRPW} | 20 | — | — | ns | |
| Data setup time before $\overline{\text{WR}}$ | t_{DS} | 20 | — | — | | |
| Data hold time after $\overline{\text{WR}}$ | t_{DH} | 10 | — | — | | |
| Chip select valid to $\overline{\text{WR}}$ | t_{CSWR} | 0 | — | — | | |
| WR logic high to $\overline{\text{CS}}$ logic high | t_{WHCS} | 10 | — | — | | |
| Delay to next $\overline{\text{CS}}$ cycle | t_{CSD} | 10 | — | — | | |

4.9 Reverse Voltage

| Parameter at $T_j = -25 \dots 125^\circ\text{C}$, $V_{bb}=15\dots30\text{V}$, $V_{CC}=4.5\dots5.5\text{V}$, unless otherwise specified | Symbol | Limit Values | | | Unit | Test Condition |
|---|---------------|---------------------|-------------|-------------|-------------|-----------------------|
| | | min. | typ. | max. | | |
| Reverse voltage ¹⁾²⁾ $R_{GND} = 0 \Omega$ $R_{GND} = 150 \Omega$ | $-V_{bb}$ | — | — | 1 45 | V | |
| Diode forward on voltage $IF = 1.25\text{A}$, $V_{Dx} = \text{low}$, each channel | $-V_{ON}$ | — | — | 1.2 | | |

1) defined by P_{tot}

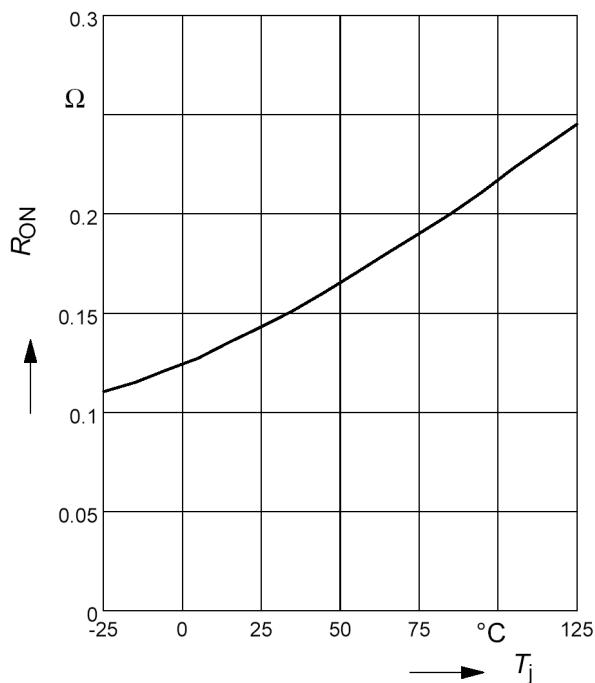
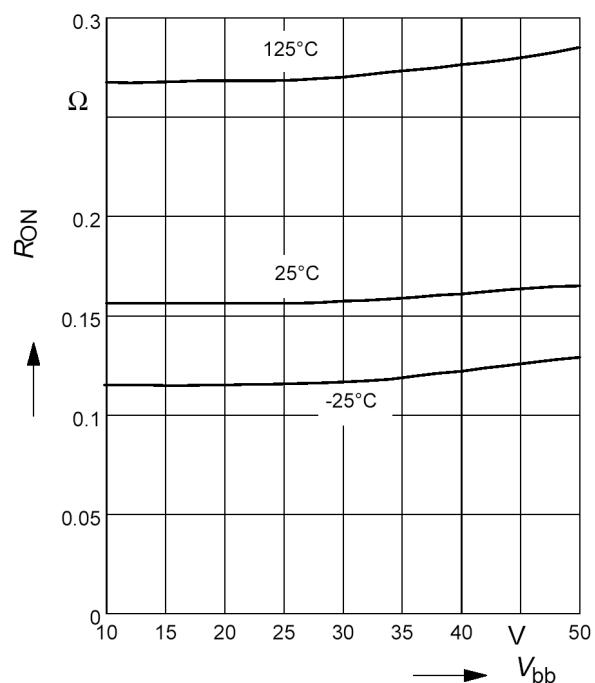
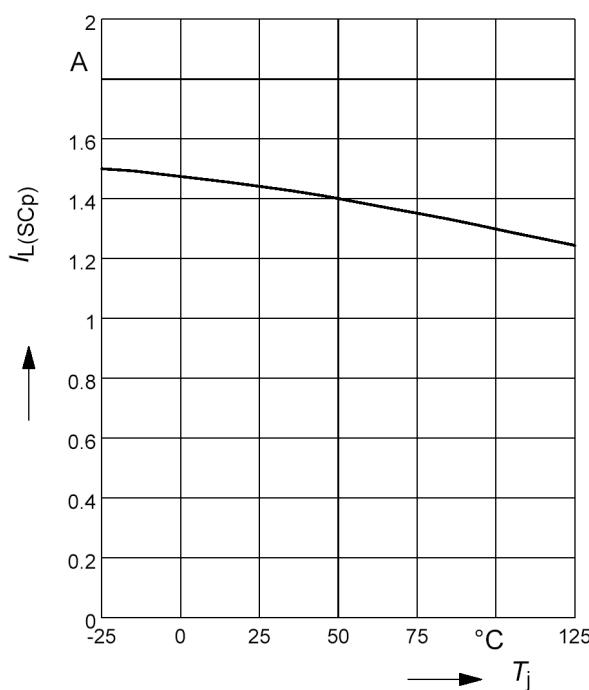
2) not subject to production test, specified by design

4.10 Isolation and Safety-Related Specification

| Parameter | Value | Unit | Conditions |
|---|--------------|-----------------|--|
| Measured from input terminals to output terminals, unless otherwise specified | | | |
| Rated dielectric isolation voltage V_{ISO} | 500 | V_{AC} | 1 minute duration ¹⁾ |
| Minimum external air gap (clearance) | 2.6 | mm | shortest distance through air. |
| Minimum external tracking (creepage) | 2.6 | mm | shortest distance path along body. |
| Minimum Internal Gap | 0.01 | mm | Insulation distance through insulation |

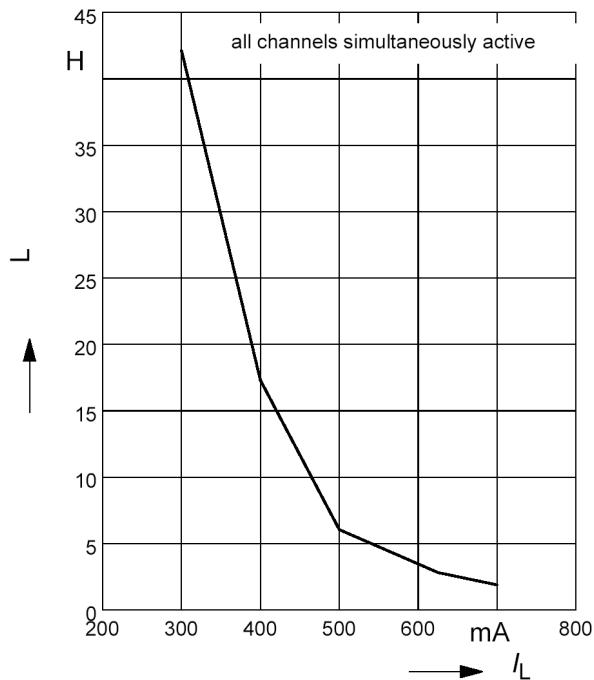
1) The parameter is not subject to production test, verified by characterization; Production Test with 1100V, 100ms duration

Note: For Qualification Report contact your local Infineon Technologies office!

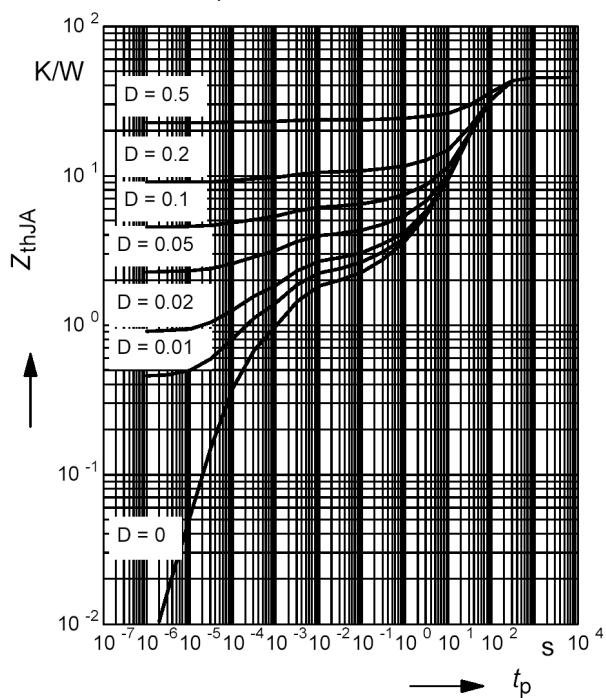
Typ. on-state resistance
 $R_{ON} = f(T_j)$; $V_{bb} = 15V$; $V_{in} = \text{high}$

Typ. on-state resistance
 $R_{ON} = f(V_{bb})$; $I_L = 0.5A$; $V_{in} = \text{high}$

Typ. initial peak short circuit current limit
 $I_{L(SCP)} = f(T_j)$; $V_{bb} = 24V$


Maximum allowable load inductance
for a single switch off, calculated

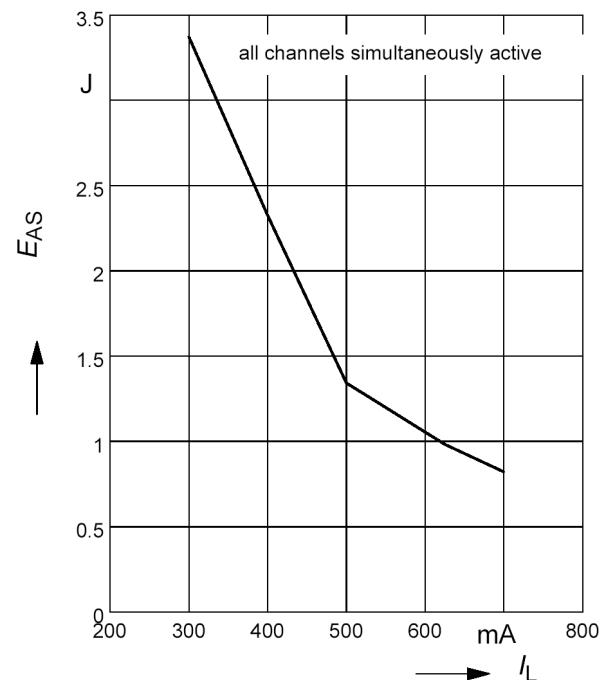
$$L = f(I_L); T_{jstart} = 125^\circ\text{C}, V_{bb} = 24\text{V}, R_L = 0\Omega$$


Typ. transient thermal impedance

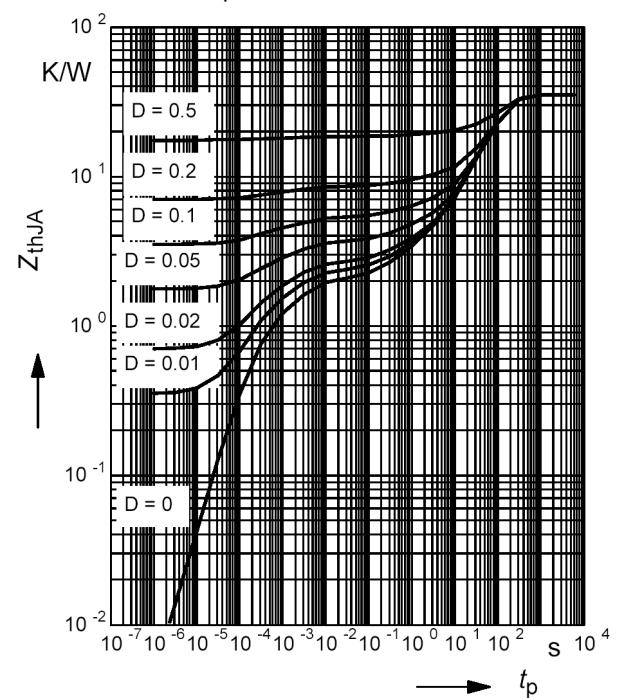
$$Z_{thJA} = f(t_p) \text{ @ min. footprint}$$

 Parameter: $D = t_p/T$

Maximum allowable inductive switch-off energy, single pulse

$$E_{AS} = f(I_L); T_{jstart} = 125^\circ\text{C}, V_{bb} = 24\text{V}$$

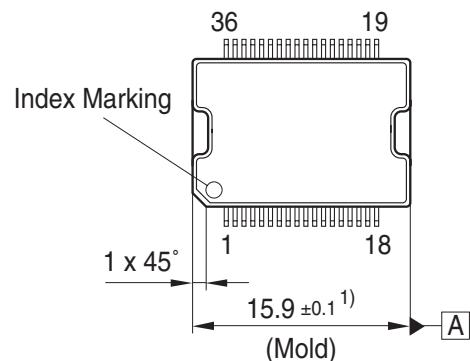
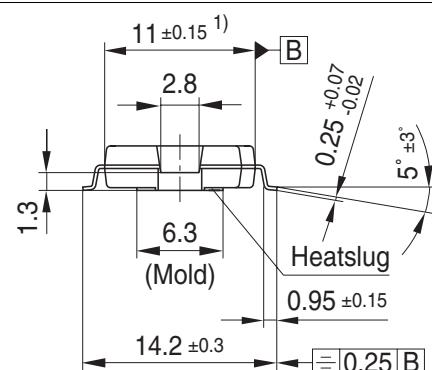
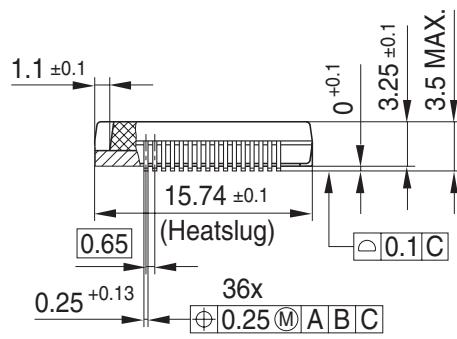

Typ. transient thermal impedance

$$Z_{thJA} = f(t_p) \text{ @ } 6\text{cm}^2 \text{ heatsink area}$$

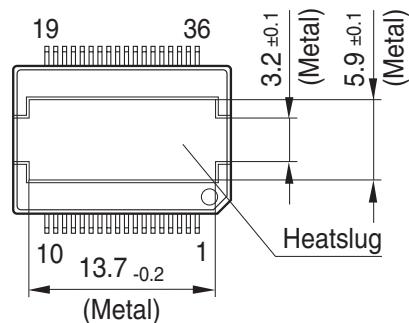
 Parameter: $D = t_p/T$


5 Package Outlines

PG-DSO-36
(Plastic Dual Small
Outline Package)



Bottom View



¹⁾ Does not include plastic or metal protrusion of 0.15 max. per side

gps09181_1

Figure 11 PG-DSO-36

Total Quality Management

Qualität hat für uns eine umfassende Bedeutung. Wir wollen allen Ihren Ansprüchen in der bestmöglichen Weise gerecht werden. Es geht uns also nicht nur um die Produktqualität – unsere Anstrengungen gelten gleichermaßen der Lieferqualität und Logistik, dem Service und Support sowie allen sonstigen Beratungs- und Betreuungsleistungen.

Dazu gehört eine bestimmte Geisteshaltung unserer Mitarbeiter. Total Quality im Denken und Handeln gegenüber Kollegen, Lieferanten und Ihnen, unserem Kunden. Unsere Leitlinie ist jede Aufgabe mit „Null Fehlern“ zu lösen – in offener Sichtweise auch über den eigenen Arbeitsplatz hinaus – und uns ständig zu verbessern.

Unternehmensweit orientieren wir uns dabei auch an „top“ (Time Optimized Processes), um Ihnen durch größere Schnelligkeit den entscheidenden Wettbewerbsvorsprung zu verschaffen. Geben Sie uns die Chance, hohe Leistung durch umfassende Qualität zu beweisen.

Wir werden Sie überzeugen.

Quality takes on an all-encompassing significance at Semiconductor Group. For us it means living up to each and every one of your demands in the best possible way. So we are not only concerned with product quality. We direct our efforts equally at quality of supply and logistics, service and support, as well as all the other ways in which we advise and attend to you.

Part of this is the very special attitude of our staff. Total Quality in thought and deed, towards co-workers, suppliers and you, our customer. Our guideline is “do everything with zero defects”, in an open manner that is demonstrated beyond your immediate workplace, and to constantly improve.

Throughout the corporation we also think in terms of Time Optimized Processes (top), greater speed on our part to give you that decisive competitive edge.

Give us the chance to prove the best of performance through the best of quality – you will be convinced.