

LOW CAPACITANCE TVS ARRAY

APPLICATIONS

- ✓ Ethernet - 10/100 Base T
- ✓ FireWire
- ✓ SCSI
- ✓ Bluetooth & RF

IEC COMPATIBILITY (EN61000-4)

- ✓ 61000-4-2 (ESD): Air - 15kV, Contact - 8kV
- ✓ 61000-4-4 (EFT): 40A - 5/50ns
- ✓ 61000-4-5 (Surge): 24A, 8/20 μ s - Level 2(Line-Gnd) & Level 3(Line-Line)

FEATURES

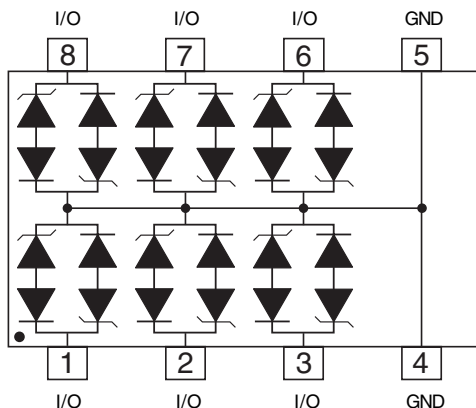
- ✓ 500 Watts Peak Pulse Power per Line (tp=8/20 μ s)
- ✓ Bidirectional Configuration
- ✓ Available in 5 Voltage Types: 3.3V to 15V
- ✓ Protects Up to Six (6) Lines
- ✓ ESD Protection > 40 kilovolts
- ✓ **LOW CAPACITANCE: 8pF**
- ✓ RoHS Compliant in Lead-Free Versions

MECHANICAL CHARACTERISTICS

- ✓ Molded JEDEC SO-8 Package
- ✓ Weight 70 milligrams (Approximate)
- ✓ Available in Tin-Lead or Lead-Free Pure-Tin Plating(Annealed)
- ✓ Solder Reflow Temperature:
 - Tin-Lead - Sn/Pb, 85/15: 240-245°C
 - Pure-Tin - Sn, 100: 260-270°C
- ✓ Flammability Rating UL 94V-0
- ✓ 12mm Tape and Reel Per EIA Standard 481
- ✓ Marking: Logo, Marking Code, Date Code & Pin One Defined By Dot on Top of Package



PIN CONFIGURATION



DEVICE CHARACTERISTICS

MAXIMUM RATINGS @ 25°C Unless Otherwise Specified

PARAMETER	SYMBOL	VALUE	UNITS
Peak Pulse Power ($t_p = 8/20\mu s$) - See Figure 1	P_{PP}	500	Watts
Operating Temperature	T_J	-55°C to 150°C	°C
Storage Temperature	T_{STG}	-55°C to 150°C	°C

ELECTRICAL CHARACTERISTICS PER LINE @ 25°C Unless Otherwise Specified

PART NUMBER	DEVICE MARKING	RATED STAND-OFF VOLTAGE V_{WM} VOLTS	MINIMUM BREAKDOWN VOLTAGE @ 1mA $V_{(BR)}$ VOLTS	MAXIMUM CLAMPING VOLTAGE (See Fig. 2) @ $I_p = 1A$ V_C VOLTS	MAXIMUM CLAMPING VOLTAGE (See Fig. 2) @ 8/20 μs V_C @ I_{PP}	MAXIMUM LEAKAGE CURRENT @ V_{WM} I_D μA	TYPICAL CAPACITANCE (See Note 1) 0V @ 1 MHz C pF
PLCDA03C-6	PRS	3.3	4.5	7.0	20.0V @ 35.0A	125	8
PLCDA05C-6	PRT	5.0	6.0	9.8	24.0V @ 42.0A	20	8
PLCDA08C-6	PRW	8.0	8.5	13.4	26.0V @ 34.0A	10	8
PLCDA12C-6	PRV	12.0	13.3	19.0	33.0V @ 21.0A	2	8
PLCDA15C-6	PRU	15.0	16.7	22.0	39.0V @ 17.0A	2	8

Note 1: Capacitance between I/O pins and ground (pins 4 & 5) is typically 8pF. Capacitance between I/O pins is typically 4 pF.

FIGURE 1
PEAK PULSE POWER VS PULSE TIME

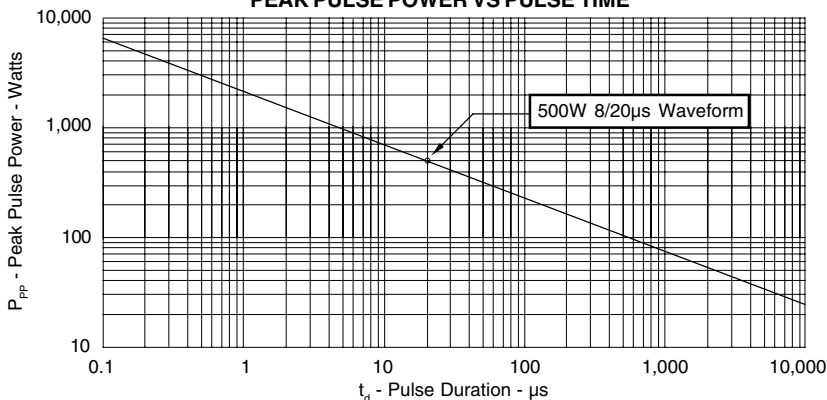
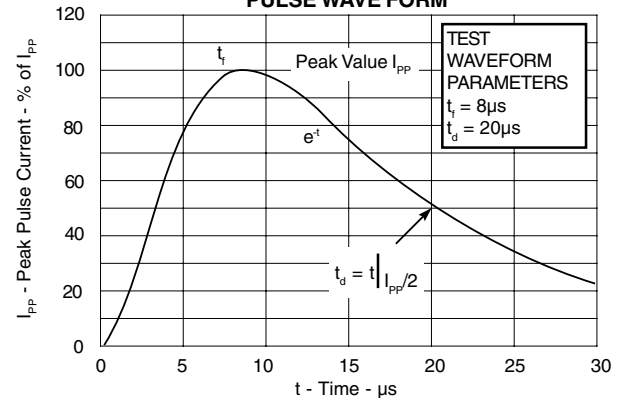


FIGURE 2
PULSE WAVE FORM



GRAPHS

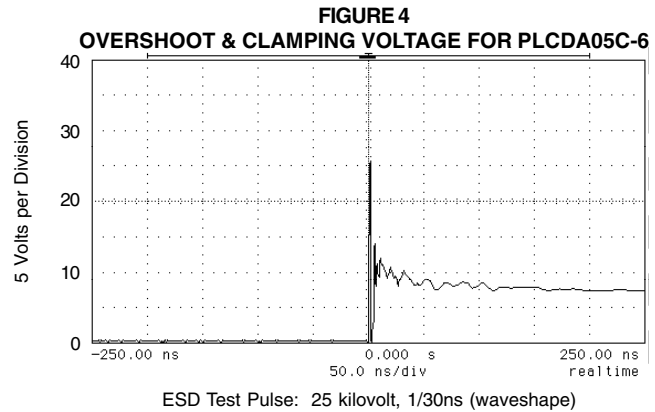
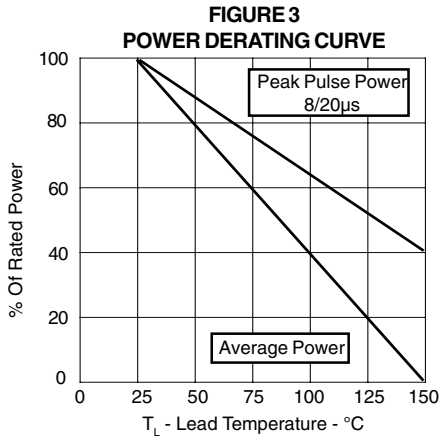
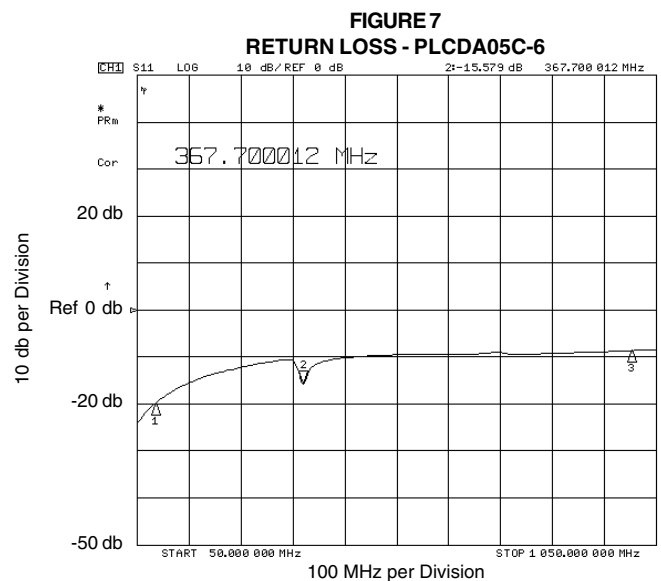
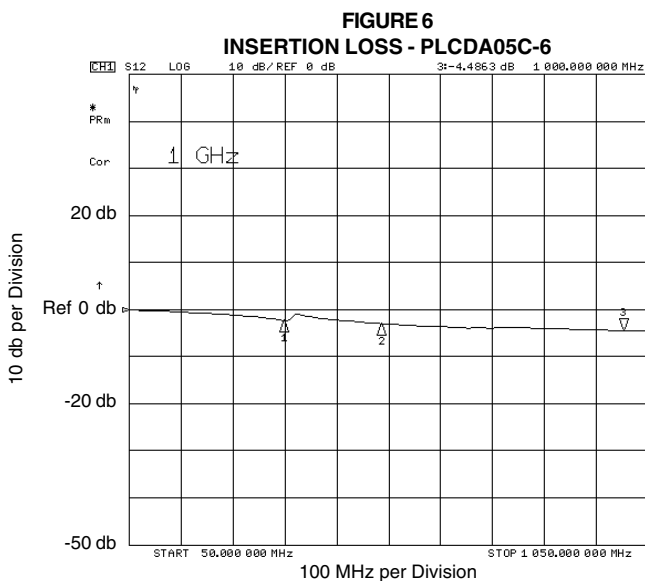
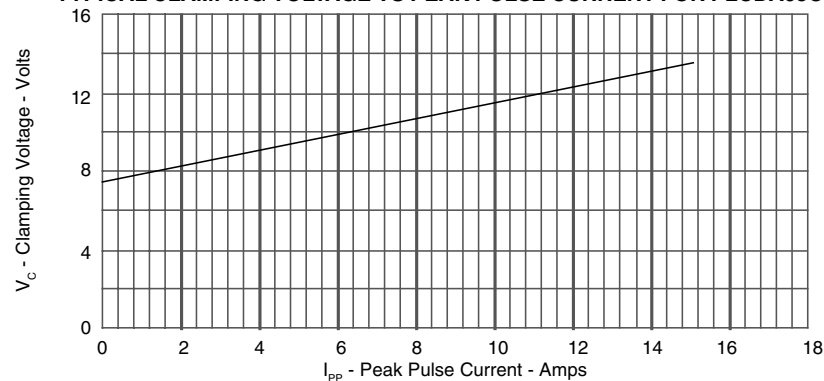


FIGURE 5
TYPICAL CLAMPING VOLTAGE VS PEAK PULSE CURRENT FOR PLCDA05C-6



APPLICATION NOTE

The PLCDAxxC-6 Series are low capacitance, bidirectional TVS arrays that are designed to protect I/O or high speed data lines from the damaging effects of ESD or EFT. This product series has a surge capability of 500 Watts P_{PP} per line for an 8/20 μ s waveshape and offers ESD protection > 40kv.

BIDIRECTIONAL COMMON-MODE CONFIGURATION (Figure 1)

Ideal for use multimode transceiver I/O lines, the PLCDAxxC-6 Series provides up to six (6) lines of protection in a common-mode configuration as depicted in Figure 1.

Circuit connectivity is as follows:

- ✓ Line 1 is connected to Pin 1.
- ✓ Line 2 is connected to Pin 2.
- ✓ Line 3 is connected to Pin 3.
- ✓ Line 4 is connected to Pin 8.
- ✓ Line 5 is connected to Pin 7.
- ✓ Line 6 is connected to Pin 6.
- ✓ Pins 4 and 5 are connected to Ground.

BIDIRECTIONAL COMMON-MODE CONFIGURATION (Figure 2)

The PLCDAxxC-6 Series also provides video line applications six (6) lines of protection in a common-mode configuration as depicted in Figure 2.

Circuit connectivity is as follows:

- ✓ Line 1 (Red) is connected to Pin 1.
- ✓ Line 2 (Green) is connected to Pin 2.
- ✓ Line 3 (Blue) is connected to Pin 3.
- ✓ Line 4 (VSYNC) is connected to Pin 6.
- ✓ Line 5 (HSYNC) is connected to Pin 7.
- ✓ Pins 4 and 5 are connected to Ground.

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Circuit board layout is critical for Electromagnetic Compatibility (EMC) protection. The following guidelines are recommended:

- ✓ The protection device should be placed near the input terminals or connectors, the device will divert the transient current immediately before it can be coupled into the nearby traces.
- ✓ The path length between the TVS device and the protected line should be minimized.
- ✓ All conductive loops including power and ground loops should be minimized.
- ✓ The transient current return path to ground should be kept as short as possible to reduce parasitic inductance.
- ✓ Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

Figure 1: Typical Transceiver Protection Circuit

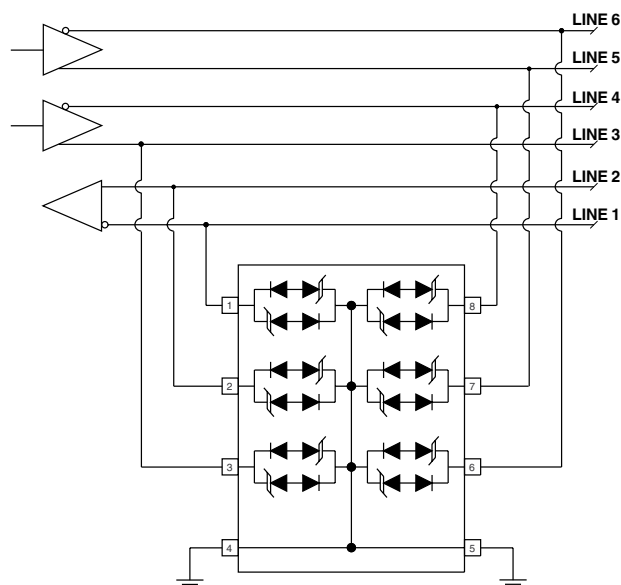
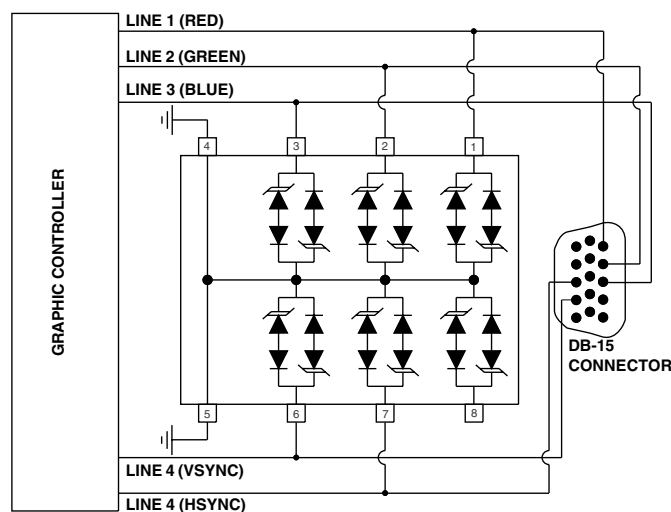
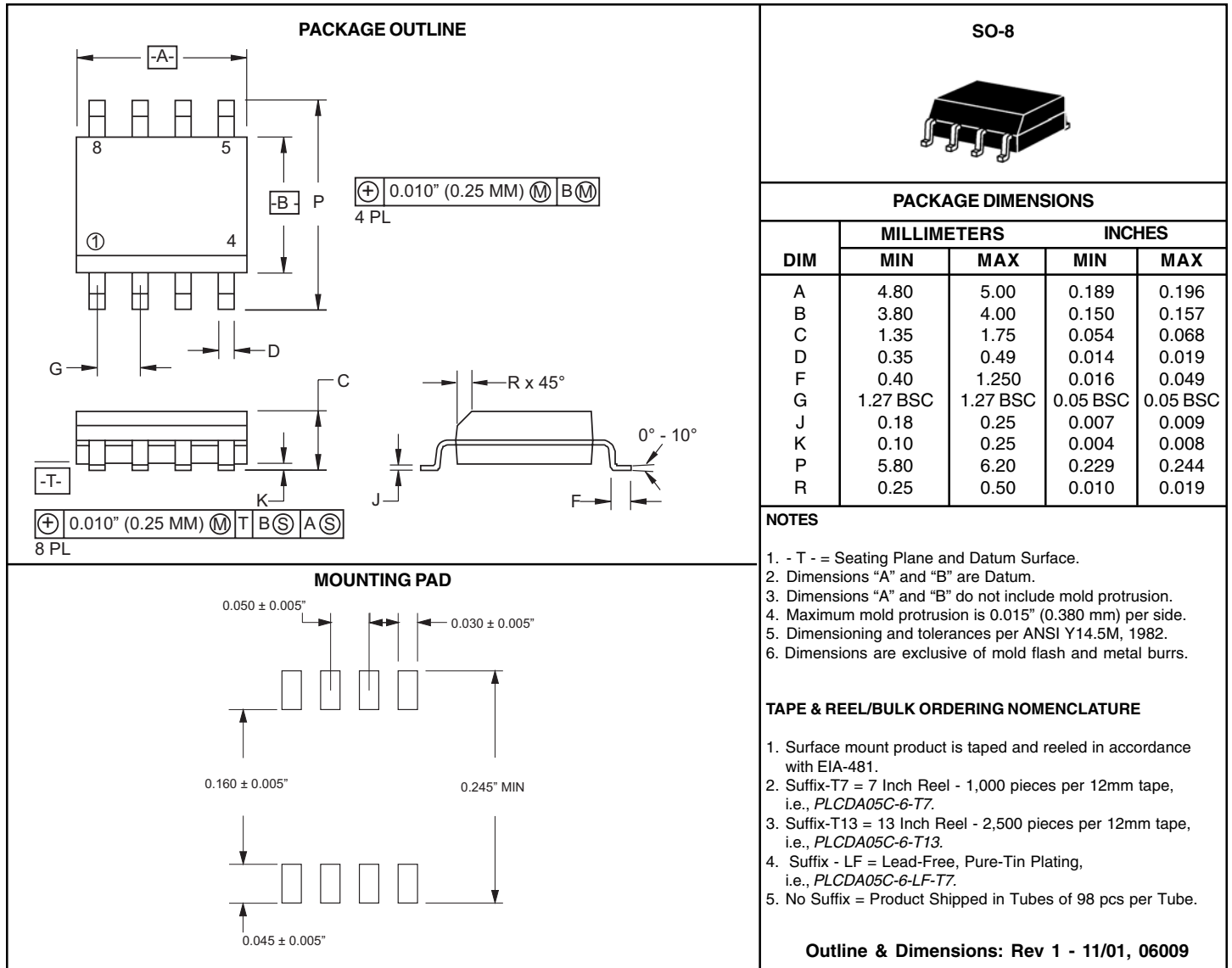


Figure 2: Typical Video Line Protection Circuit



PACKAGE OUTLINE & DIMENSIONS



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