Complete Thermal System Management Controller

ADM1026

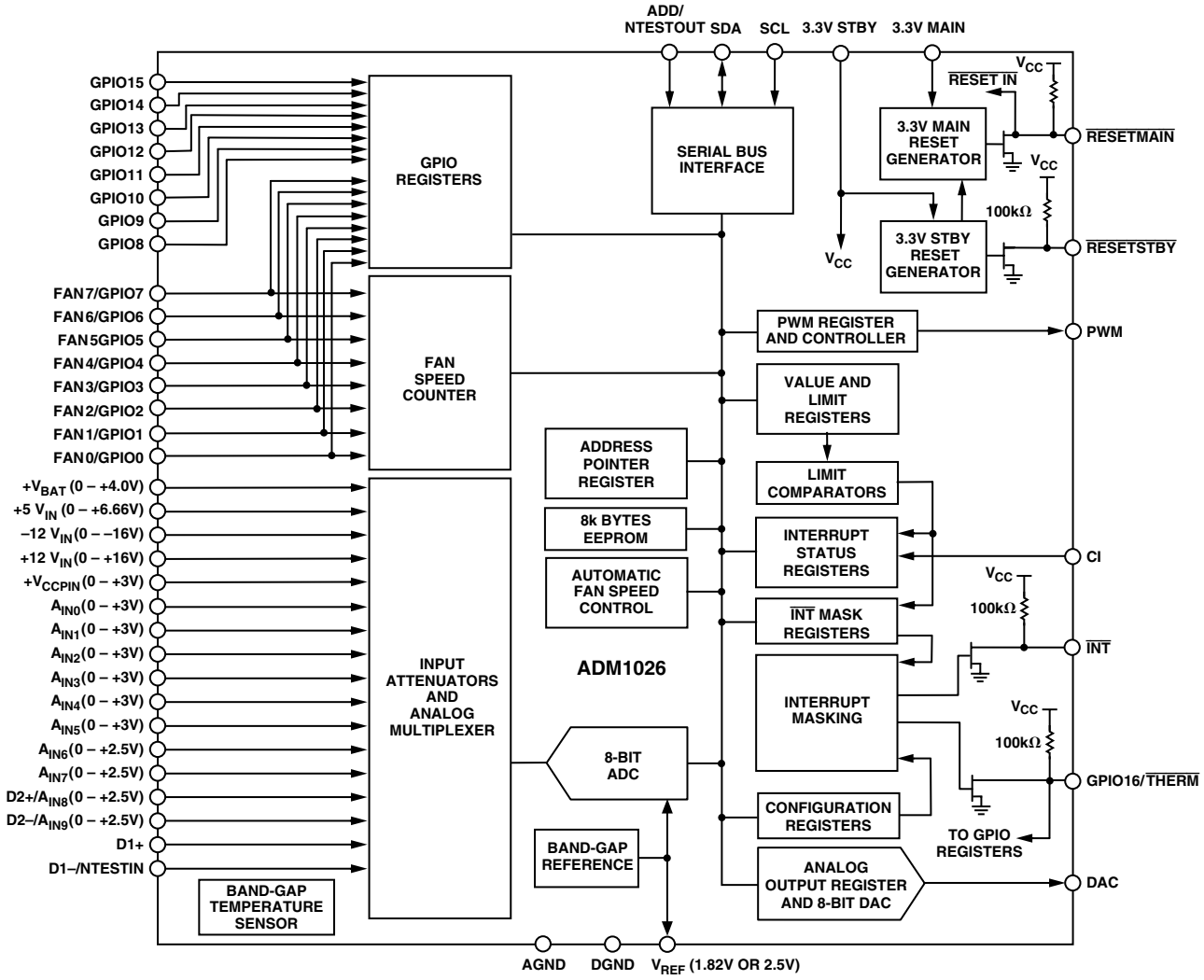
FEATURES

- Up to 19 Analog Measurement Channels (Including Internal Measurements)
- Up to 8 Fan Speed Measurement Channels
- Up to 17 General Purpose Logic I/O Pins
- Remote Temperature Measurement with Remote Diode (Two Channels)
- On-Chip Temperature Sensor
- Analog and PWM Fan Speed Control Outputs
- 2-Wire Serial System Management Bus (SMBus)
- 8 kB On-Chip EEPROM
- Full SMBus 1.1 Support Including Packet Error Checking (PEC)
- Chassis Intrusion Detection
- Interrupt Output (SMBAlert)
- Reset Input, Reset Outputs
- Thermal Interrupt ($\overline{\text{THERM}}$) Output
- Limit Comparison of All Monitored Values

APPLICATIONS

- Network Servers and Personal Computers
- Telecommunications Equipment
- Test Equipment and Measuring Instruments

FUNCTIONAL BLOCK DIAGRAM



REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700
www.analog.com
Fax: 781/326-8703

ADM1026–SPECIFICATIONS[1, 2, 3] ($T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted.)

Parameter	Min	Typ	Max	Test Conditions/Comments	Unit
POWER SUPPLY					
Supply Voltage, 3.3 V STBY, 3.3 V MAIN	3.0	3.3	5.5		V
Supply Current, I_{CC}		2.5	4.0	Interface Inactive, ADC Active	mA
TEMPERATURE-TO-DIGITAL CONVERTER					
Internal Sensor Accuracy			±3		°C
Resolution		±1			°C
External Diode Sensor Accuracy			±3	$0°C < T_D < 100°C$	°C
Resolution		±1			°C
Remote Sensor Source Current		90		High Level	µA
		5.5		Low Level	µA
ANALOG-TO-DIGITAL CONVERTER (INCLUDING MUX AND ATTENUATORS)					
Total Unadjusted Error, TUE			±2	See Note 4	%
Differential Nonlinearity, DNL			±1		LSB
Power Supply Sensitivity		±0.1			%/V
Conversion Time (Analog Input or Int.Temp)		11.38	12.06	See Note 5	ms
Conversion Time (External Temperature)		34.13	36.18	See Note 5	ms
Input Resistance (+5 V, V_{CCP}, $A_{IN0} – A_{IN5}$)	80	100	120		kΩ
Input Resistance of +12 V pin	70	100	115		kΩ
Input Resistance of –12 V pin	8	10	12		kΩ
Input Resistance ($A_{IN6} – A_{IN9}$)	5				MΩ
Input Resistance of V_{BAT} pin	80	100	120	See Note 4	kΩ
V_{BAT} Current Drain (when measured)		80	100	CR2032 Battery Life >10 years	nA
V_{BAT} Current Drain (when not measuring)		6			nA
ANALOG OUTPUT (DAC)					
Output Voltage Range		0–2.5			V
Total Unadjusted Error, TUE			±5	I_L = 2 mA	%
Zero Error		1		No Load	LSB
Differential Nonlinearity, DNL			±1	Monotonic by Design	LSB
Integral Nonlinearity		±0.5			LSB
Output Source Current		2			mA
Output Sink Current		1			mA
REFERENCE OUTPUT					
Output Voltage	1.8	1.82	1.84	Bit 2 of Register 07h = 0	V
Output Voltage	2.47	2.50	2.53	Bit 2 of Register 07h = 1	V
Load Regulation (I_{SINK} = 2 mA)		0.15			%
Load Regulation (I_{SOURCE} = 2 mA)		0.15			%
Short Circuit Current		25		V_{CC} = 3.3 V	mA
Output Current Source		2			mA
Output Current Sink		2			mA
FAN RPM-TO-DIGITAL CONVERTER				See Note 6	
Accuracy			±12		%
Full-Scale Count			255		
FAN0 to FAN7 Nominal Input RPM		8800		Divisor = 1, Fan Count = 153	RPM
(See Note 5)		4400		Divisor = 2, Fan Count = 153	RPM
		2200		Divisor = 4, Fan Count = 153	RPM
		1100		Divisor = 8, Fan Count = 153	RPM
Internal Clock Frequency	20	22.5	25		kHz
OPEN DRAIN O/Ps, PWM, GPIO0 – 16					
Output High Voltage, V_{OH}	2.4			I_{OUT} = 3.0 mA, V_{CC} = 3.3 V	V
High Level Output Leakage Current, I_{OH}		0.1	1	$V_{OUT} = V_{CC}$	µA
Output Low Voltage, V_{OL}			0.4	I_{OUT} = –3.0 mA, V_{CC} = 3.3 V	V
PWM Output Frequency		75			Hz
DIGITAL OUTPUTS ($\overline{INT}$, $\overline{RESETMAIN}$, $\overline{RESETSTBY}$)					
Output Low Voltage, V_{OL}			0.4	I_{OUT} = –3.0 mA, V_{CC} = 3.3 V	V
$\overline{RESET}$ Pulsewidth	140	180	240		ms

Parameter	Min	Typ	Max	Test Conditions/Comments	Unit
OPEN DRAIN SERIAL DATABUS OUTPUT (SDA)					
Output Low Voltage, V_{OL}			0.4	I_{OUT} = –3.0 mA, V_{CC} = 3.3 V	V
High Level Output Leakage Current, I_{OH}		0.1	1	V_{OUT} = V_{CC}	µA
SERIAL BUS DIGITAL INPUTS (SCL, SDA)					
Input High Voltage, V_{IH}	2.2				V
Input Low Voltage, V_{IL}			0.8		V
Hysteresis		500			mV
DIGITAL INPUT LOGIC LEVELS (ADD, CI, FAN 0–7, GPIO 0–16)				See Notes 7 and 8	
Input High Voltage, V_{IH}	2.4			V_{CC} = 3.3 V	V
Input Low Voltage, V_{IL}	0.8			V_{CC} = 3.3 V	V
Hysteresis (Fan 0–7)		250		V_{CC} = 3.3 V	mV
$\overline{\text{RESETMAIN}}$, $\overline{\text{RESETSTBY}}$					
$\overline{\text{RESETMAIN}}$ Threshold	2.89	2.94	2.97	Falling Voltage	V
$\overline{\text{RESETSTBY}}$ Threshold	3.01	3.05	3.10	Falling Voltage	V
$\overline{\text{RESETMAIN}}$ Hysteresis		60			mV
$\overline{\text{RESETSTBY}}$ Hysteresis		70			mV
DIGITAL INPUT CURRENT					
Input High Current, I_{IH}	–1			V_{IN} = V_{CC}	µA
Input Low Current, I_{IL}			1	V_{IN} = 0	µA
Input Capacitance, C_{IN}		20			pF
EEPROM RELIABILITY					
Endurance	100	700		See Note 9	Kcycles
Data Retention	10			See Note 10	Years
SERIAL BUS TIMING					
Clock Frequency, f_{SCLK}			400	See Figure 1	kHz
Glitch Immunity, t_{SW}			50	See Figure 1	ns
Bus Free Time, t_{BUF}	4.7			See Figure 1	µs
Start Setup Time, $t_{SU;\,STA}$	4.7			See Figure 1	µs
Start Hold Time, $t_{HD;\,STA}$	4			See Figure 1	µs
SCL Low Time, t_{LOW}	4.7			See Figure 1	µs
SCL High Time, t_{HIGH}	4			See Figure 1	µs
SCL, SDA Rise Time, t_r			1000	See Figure 1	ns
SCL, SDA Fall Time, t_f			300	See Figure 1	ns
Data Setup Time, $t_{SU;\,DAT}$	250			See Figure 1	ns
Data Hold Time, $t_{HD;\,DAT}$	300			See Figure 1	ns

NOTES

[1] All voltages are measured with respect to GND, unless otherwise specified.

[2] Typicals are at T_A = 25°C and represent most likely parametric norm. Shutdown current typ is measured with V_{CC} = 3.3 V.

[3] Timing specifications are tested at logic levels of V_{IL} = 0.8 V for a falling edge and V_{IH} = 2.1 V for a rising edge.

[4] TUE (Total Unadjusted Error) includes Offset, Gain, and Linearity errors of the ADC, multiplexer, and on-chip input attenuators. V_{BAT} input is only linear for V_{BAT} voltages greater than 1.5 V.

[5] Total analog monitoring cycle time is nominally 273 ms, made up of 18 × 11.38 ms measurements on analog input and internal temperature channels, and 2 × 34.13 ms measurements on external temperature channels.

[6] The total fan count is based on two pulses per revolution of the fan tachometer output. The total fan monitoring time depends on the number of fans connected and the fan speed. See Fan Speed Monitoring section for more details.

[7] ADD is a three-state input that may be pulled high, low, or left open-circuit.

[8] Logic inputs will accept input high voltages up to 5 V even when device is operating at supply voltages below 5 V.

[9] Endurance is qualified to 100,000 cycles as per JEDEC Std. 22 method A117, and measured at –40°C, 25°C, and 85°C. Typical endurance at 25°C is 700,000 cycles.

[10] Retention lifetime equivalent at junction temperature (T_J) = 55°C as per JEDEC Std. 22 method A117. Retention lifetime based on an activation energy of 0.6 V will derate with junction temperature as shown in Figure 2.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Positive Supply Voltage (V_{CC}) . . . . . 6.5 V
Voltage on +12 V V_{IN} Pin . . . . . +20 V
Voltage on –12 V V_{IN} Pin . . . . . –20 V
Voltage on Analog Pins . . . . . –0.3 V to (V_{CC} + 0.3 V)
Voltage on Open Drain Digital Pins . . . . . –0.3 V to +6.5 V
Input Current at any Pin . . . . . ±5 mA
Package Input Current . . . . . ±20 mA
Maximum Junction Temperature ($T_{J\,MAX}$) . . . . . 150°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . 215°C
Infrared (15 sec) . . . . . 200°C
ESD Rating, –12 V_{IN} Pin . . . . . 1000 V
ESD Rating, All Other Pins . . . . . 2000 V

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

48-Lead LQFP Package
θ_{JA} = 50°C/W, θ_{JC} = 10°C/W

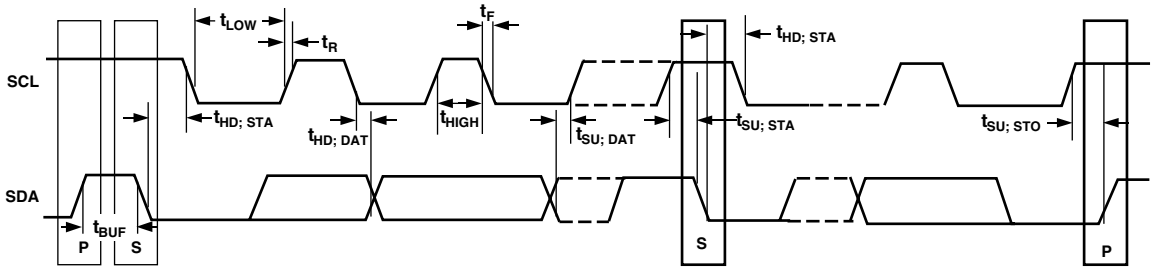


Figure 1. Serial Bus Timing Diagram

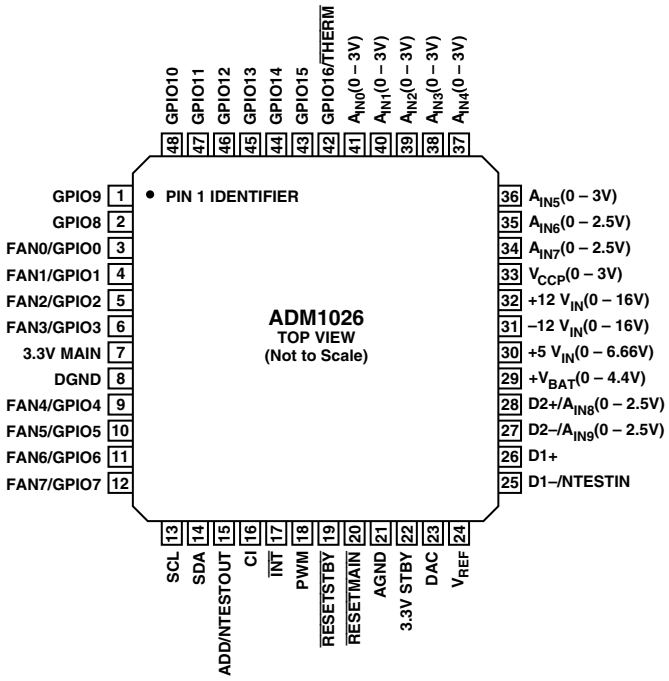
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADM1026JST-REEL	0°C to 100°C	48-Lead LQFP	ST-48
ADM1026JST-REEL7	0°C to 100°C	48-Lead LQFP	ST-48

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADM1026 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



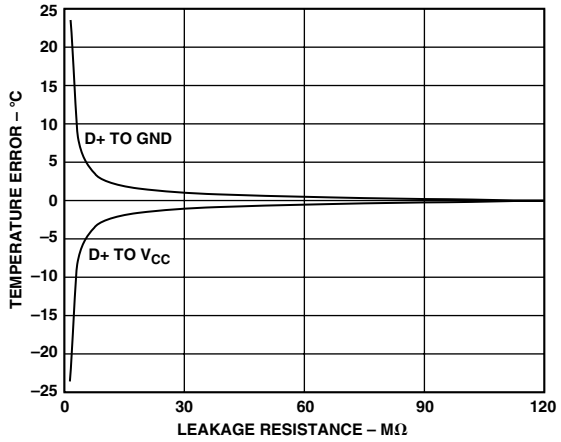
PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Type	Description
1	GPIO9	Digital I/O*	General purpose I/O pin can be configured as a digital input or output.
2	GPIO8	Digital I/O*	General purpose I/O pin can be configured as a digital input or output.
3	FAN0/GPIO0	Digital I/O	Fan tachometer input with internal 10 kΩ pull-up resistor to 3.3 V STBY. Can be reconfigured as a general purpose, open drain, digital I/O pin.
4	FAN1/GPIO1	Digital I/O	Fan tachometer input with internal 10 kΩ pull-up resistor to 3.3 V STBY. Can be reconfigured as a general purpose, open drain, digital I/O pin.
5	FAN2/GPIO2	Digital I/O	Fan tachometer input with internal 10 kΩ pull-up resistor to 3.3 V STBY. Can be reconfigured as a general purpose, open drain, digital I/O pin.
6	FAN3/GPIO3	Digital I/O	Fan tachometer input with internal 10 kΩ pull-up resistor to 3.3 V STBY. Can be reconfigured as a general purpose, open drain, digital I/O pin.
7	3.3 V MAIN	Analog Input	Monitors the main 3.3 V system supply. Does not power device.
8	DGND	Ground	Ground pin for digital circuits.
9	FAN4/GPIO4	Digital I/O	Fan tachometer input with internal 10 kΩ pull-up resistor to 3.3 V STBY. Can be reconfigured as a general purpose, open drain, digital I/O pin.
10	FAN5/GPIO5	Digital I/O	Fan tachometer input with internal 10 kΩ pull-up resistor to 3.3 V STBY. Can be reconfigured as a general purpose, open drain, digital I/O pin.
11	FAN6/GPIO6	Digital I/O	Fan tachometer input with internal 10 kΩ pull-up resistor to 3.3 V STBY. Can be reconfigured as a general purpose, open drain, digital I/O pin.
12	FAN7/GPIO7	Digital I/O	Fan tachometer input with internal 10 kΩ pull-up resistor to 3.3 V STBY. Can be reconfigured as a general purpose, open drain, digital I/O pin.
13	SCL	Digital Input	Open Drain Serial Bus Clock. Requires 2.2 kΩ pull-up resistor.
14	SDA	Digital I/O	Serial Bus Data. Open drain I/O. Requires 2.2 kΩ pull-up resistor.
15	ADD/NTESTOUT	Digital Input	This is a three-state input that controls the two LSBs of the Serial Bus Address. It also functions as the output for NAND tree testing.
16	CI	Digital Input	An active high input that captures a Chassis Intrusion event in Bit 6 of Status Register 4. This bit will remain set until cleared, so long as battery voltage is applied to the V_{BAT} input, even when the ADM1026 is powered off.

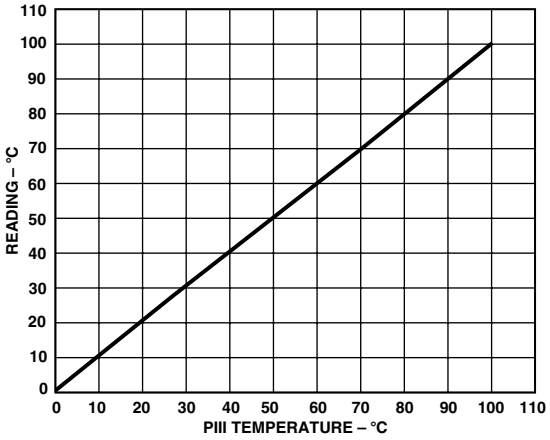
PIN FUNCTION DESCRIPTIONS (continued)

Pin No.	Mnemonic	Type	Description
17	$\overline{\text{INT}}$	Digital Output	Interrupt Request (open drain). The output is enabled when Bit 1 of the Configuration Register is set to 1. The default state is disabled. It has an on-chip 100 kΩ pull-up resistor.
18	PWM	Digital Output	Open drain pulsewidth modulated output for control of fan speed. This pin defaults to being high for 100% duty cycle for use with NMOS drive circuitry. If a PMOS device is used to drive the fan, the PWM output may be inverted by setting Bit 1 of Test Register 1 = 1.
19	$\overline{\text{RESETSTBY}}$	Digital Output	Power ON Reset. 5 mA driver (weak 100 kΩ pull-up), active low output (100 kΩ pull-up) with a 180 ms typical pulsewidth. $\overline{\text{RESETSTBY}}$ is asserted whenever 3.3 V STBY is below the reset threshold. It remains asserted for approximately 180 ms after 3.3 V STBY rises above the reset threshold.
20	$\overline{\text{RESETMAIN}}$	Digital I/O	Power ON Reset. 5 mA driver (weak 100 kΩ pull-up), active low output (100 kΩ pull-up) with a 180 ms typical pulsewidth. $\overline{\text{RESETMAIN}}$ is asserted whenever 3.3 V MAIN is below the reset threshold. It remains asserted for approximately 180 ms after 3.3 V MAIN rises above the reset threshold. If, however, 3.3 V STBY rises with or before 3.3 V MAIN, then $\overline{\text{RESETMAIN}}$ remains asserted for 180 ms after $\overline{\text{RESETSTBY}}$ is deasserted. Pin 20 also functions as an active low RESET input.
21	AGND	Ground	Ground pin for analog circuits
22	3.3 V STBY	Power Supply	Supplies 3.3 V power. Also monitors 3.3 V standby power rail.
23	DAC	Analog Output	0 to 2.5 V output for analog control of fan speed.
24	V_{REF}	Analog Output	Reference voltage output. Can be selected as 1.8 V (default) or 2.5 V.
25	D1–/NTESTIN	Analog Input	Connected to cathode of first remote temperature sensing diode. If held high at power up, it activates NAND tree test mode.
26	D1+	Analog Input	Connected to anode of first remote temperature sensing diode.
27	D2–/A_{IN9}	Programmable	Connected to cathode of second remote temperature sensing diode, or Analog Input may be reconfigured as a 0 V – 2.5 V analog input
28	D2+/A_{IN8}	Programmable	Connected to anode of second remote temperature sensing diode, or Analog Input may be reconfigured as a 0 V – 2.5 V analog input
29	V_{BAT}	Analog Input	Monitors battery voltage, nominally +3 V.
30	+5 V_{IN}	Analog Input	Monitors +5 V supply.
31	–12 V_{IN}	Analog Input	Monitors –12 V supply.
32	+12 V_{IN}	Analog Input	Monitors +12 V supply.
33	$+V_{CCP}$	Analog Input	Monitors processor core voltage (0 to 3.0 V).
34	A_{IN7}	Analog Input	General purpose 0 V to 2.5 V analog input.
35	A_{IN6}	Analog Input	General purpose 0 V to 2.5 V analog input.
36	A_{IN5}	Analog Input	General purpose 0 V to 3 V analog input.
37	A_{IN4}	Analog Input	General purpose 0 V to 3 V analog input.
38	A_{IN3}	Analog Input	General purpose 0 V to 3 V analog input.
39	A_{IN2}	Analog Input	General purpose 0 V to 3 V analog input.
40	A_{IN1}	Analog Input	General purpose 0 V to 3 V analog input.
41	A_{IN0}	Analog Input	General purpose 0 V to 3 V analog input.
42	GPIO16/$\overline{\text{THERM}}$	Digital I/O*	General purpose I/O pin can be configured as a digital input or output. Can also be configured as a bidirectional $\overline{\text{THERM}}$ pin (100 kΩ pull-up).
43	GPIO15	Digital I/O*	General purpose I/O pin can be configured as a digital input or output.
44	GPIO14	Digital I/O*	General purpose I/O pin can be configured as a digital input or output.
45	GPIO13	Digital I/O*	General purpose I/O pin can be configured as a digital input or output.
46	GPIO12	Digital I/O*	General purpose I/O pin can be configured as a digital input or output.
47	GPIO11	Digital I/O*	General purpose I/O pin can be configured as a digital input or output.
48	GPIO10	Digital I/O*	General purpose I/O pin can be configured as a digital input or output.

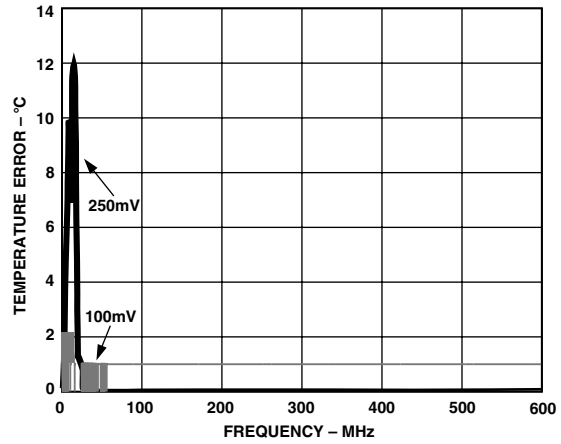
*GPIO pins are open drain and require external pull-up resistors. Fan inputs have integrated 10 kΩ pull-ups, but these pins become open drain when reconfigured as GPIOs.



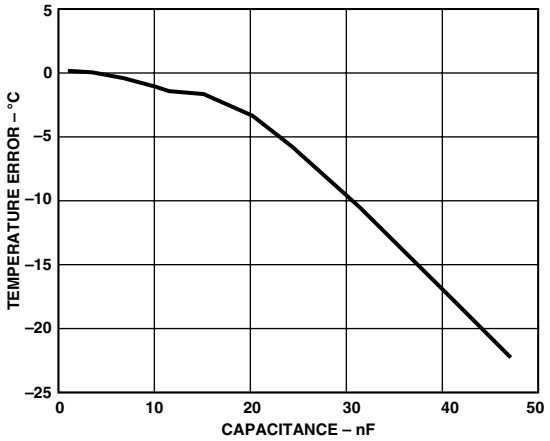
TPC 1. Temperature Error vs. PCB Track Resistance



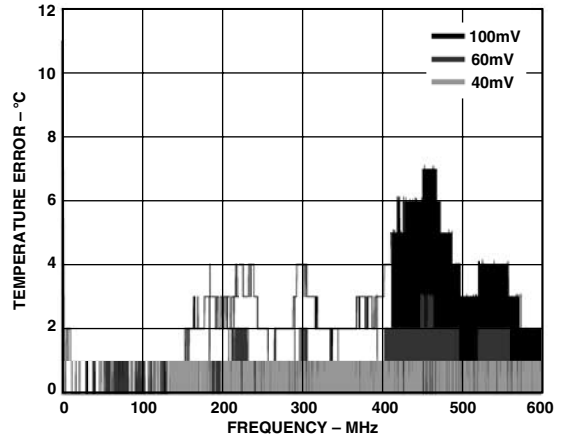
TPC 4. Pentium® III Temperature vs. ADM1026 Reading



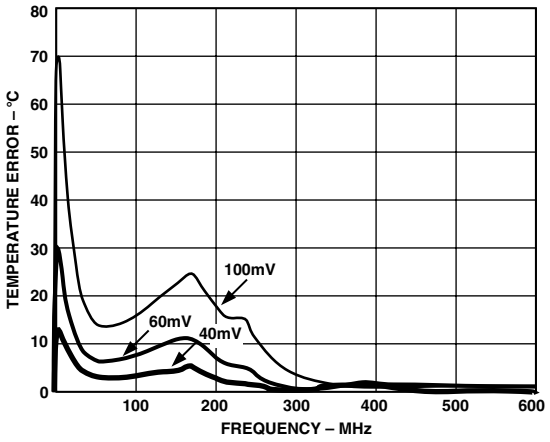
TPC 2. Temperature Error vs. Power Supply Noise Frequency



TPC 5. Temperature Error vs. Capacitance Between D+ and D–

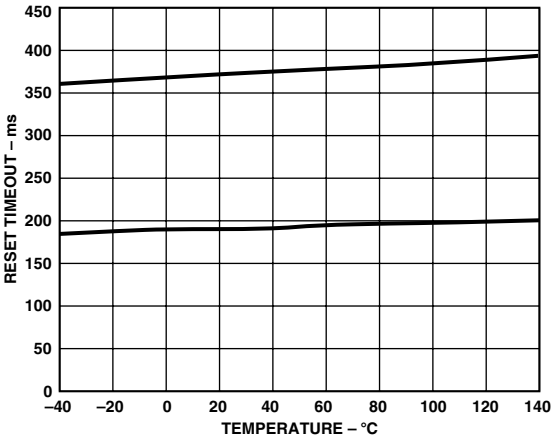


TPC 3. Temperature Error vs. Common-Mode Noise Frequency

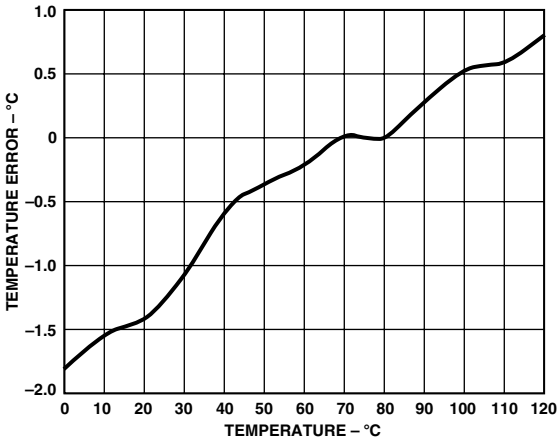


TPC 6. Temperature Error vs. Differential-Mode Noise Frequency

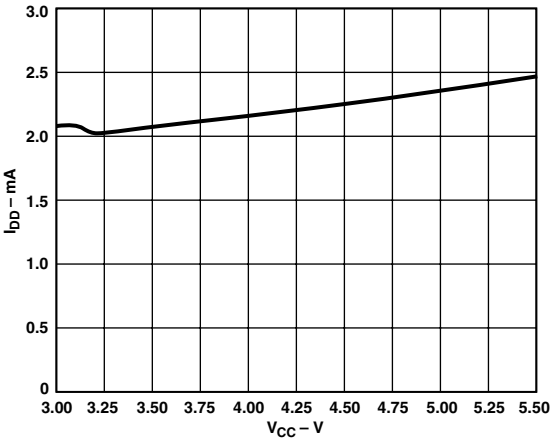
Pentium is a registered trademark of Intel Corporation.



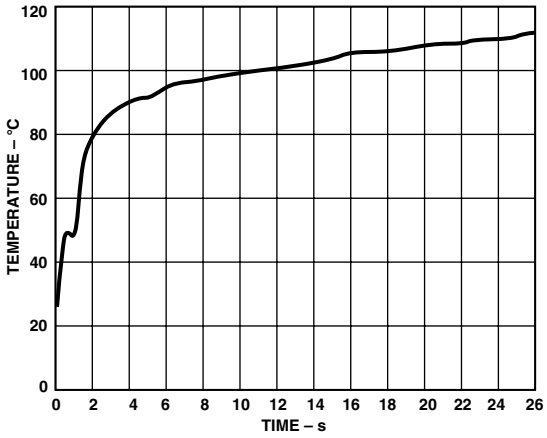
TPC 7. Power-up Reset Timeout vs. Temperature



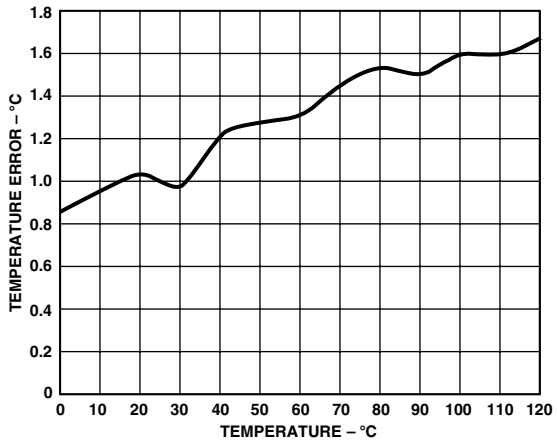
TPC 10. Remote Sensor Temperature Error



TPC 8. Supply Current vs. Supply Voltage



TPC 11. Response to Thermal Shock



TPC 9. Local Sensor Temperature Error

PRODUCT DESCRIPTION

The ADM1026 is a complete system hardware monitor for microprocessor-based systems, providing measurement and limit comparison of various system parameters. The ADM1026 has up to 19 analog measurement channels. Fifteen analog voltage inputs are provided, five of which are dedicated to monitoring +3.3 V, +5 V, and ±12 V power supplies, and the processor core voltage. The ADM1026 can monitor two further power supply voltages by measuring its own V_{CC} and the main system supply. One input (two pins) is dedicated to a remote temperature sensing diode. Two further pins can be configured as general purpose analog inputs to measure 0 to 2.5 V, or as a second temperature sensing input. The eight remaining inputs are general-purpose analog inputs with a range of 0 V to 2.5 V or 0 V to 3 V. Finally, the ADM1026 has an on-chip temperature sensor.

The ADM1026 has eight pins that can be configured for fan speed measurement or as general-purpose logic I/O pins. A further eight pins are dedicated to general-purpose logic I/O. An additional pin can be configured as a general-purpose I/O or as the bidirectional $\overline{\text{THERM}}$ pin.

Measured values can be read out via a 2-wire serial system management bus, and values for limit comparisons can be programmed in over the same serial bus. The high speed, successive approximation ADC allows frequent sampling of all analog channels to ensure a fast interrupt response to any out-of-limit measurement.

FUNCTIONAL DESCRIPTION

General Description

The ADM1026 is a complete system hardware monitor for microprocessor-based systems. The device communicates with the system via a serial system management bus. The serial bus controller has a hardwired address line for device selection (ADD, Pin 15), a serial data line for reading and writing addresses and data (SDA, Pin 14), and an input line for the serial clock (SCL, Pin 13). All control and programming functions of the ADM1026 are performed over the serial bus.

Measurement Inputs

Programmability of the analog and digital measurement inputs makes the ADM1026 extremely flexible and versatile. The device has an 8-bit A/D converter, and 17 analog measurement input pins that can be configured in different ways.

Pins 25 and 26 are dedicated temperature inputs and may be connected to the cathode and anode of a remote temperature-sensing diode.

Pins 27 and 28 may be configured as temperature inputs and connected to a second temperature-sensing diode, or may be reconfigured as analog inputs with a range of 0 V to 2.5 V.

Pins 29 to 33 are dedicated analog inputs with on-chip attenuators configured to monitor V_{BAT}, +5 V, –12 V, +12 V, and the processor core voltage V_{CCP}, respectively.

Pins 34 to 41 are general-purpose analog inputs with a range of 0 V to 2.5 V or 0 V to 3 V. These are mainly intended for monitoring SCSI termination voltages, but may be used for other purposes.

The ADC also accepts input from an on-chip band-gap temperature sensor that monitors system ambient temperature.

Finally, the ADM1026 monitors the supply from which it is powered, 3.3 V STBY, so there is no need for a separate pin to monitor this power supply voltage.

The ADM1026 has eight pins that are general-purpose logic I/O pins (Pins 1, 2, and 43 to 48), a pin that can be configured as GPIO or as a bidirectional thermal interrupt ($\overline{\text{THERM}}$) pin (Pin 42), and eight pins that can be configured for fan speed measurement or as general-purpose logic pins (Pins 3 to 6 and 9 to 12).

Sequential Measurement

When the ADM1026 monitoring sequence is started, it cycles sequentially through the measurement of analog inputs and the temperature sensor, while at the same time the fan speed inputs are independently monitored. Measured values from these inputs are stored in value registers. These can be read out over the serial bus, or can be compared with programmed limits stored in the limit registers. The results of out-of-limit comparisons are stored in the interrupt status registers, and will generate an interrupt on the $\overline{\text{INT}}$ line (Pin 17).

Any or all of the interrupt status bits can be masked by appropriate programming of the interrupt mask registers.

Chassis Intrusion

A chassis intrusion input (Pin 16) is provided to detect unauthorized tampering with the equipment. This event is latched in a battery-backed register bit.

Resets

The ADM1026 has two power-on reset outputs, $\overline{\text{RESETMAIN}}$ and $\overline{\text{RESETSTBY}}$, that are asserted when 3.3 V MAIN or 3.3 V STBY fall below the reset threshold. These give a 180 ms reset pulse at power-up. $\overline{\text{RESETMAIN}}$ also functions as an active-low RESET input.

Fan Speed Control Outputs

The ADM1026 has two outputs intended to control fan speed, though they can also be used for other purposes.

Pin 18 is an open drain, pulsewidth modulated (PWM) output with a programmable duty cycle and an output frequency of 75 Hz.

Pin 23 is connected to the output of an on-chip, 8-bit digital-to-analog converter with an output range of 0 V to 2.5 V.

Either or both of these outputs may be used to implement a temperature-controlled fan by controlling the speed of a fan dependent upon the temperature measured by the on-chip temperature sensor or remote temperature sensors.

INTERNAL REGISTERS

The ADM1026 contains a large number of data registers. A brief description of the principal registers is given below. More detailed descriptions are given in the relevant sections and in the tables at the end of the data sheet.

Address Pointer Register: This register contains the address that selects one of the other internal registers. When writing to the ADM1026, the first byte of data is always a register address, which is written to the address pointer register.

Configuration Registers: Provide control and configuration for various operating parameters of the ADM1026.

Fan Divisor Registers: Contain counter pre-scaler values for fan speed measurement.

DAC/PWM Control Registers: Contain speed values for PWM and DAC fan drive outputs.

GPIO Configuration Registers: These configure the GPIO pins as input or output and for signal polarity.

Value and Limit Registers: The results of analog voltage inputs, temperature and fan speed measurements are stored in these registers, along with their limit values.

Status Registers: These registers store events from the various interrupt sources.

Mask Registers: Allow masking of individual interrupt sources.

EEPROM

The ADM1026 has 8 kB of nonvolatile, Electrically-Erasable Programmable Read-Only Memory (EEPROM) from register addresses 8000h to 9FFFh. This may be used for permanent storage of data that will not be lost when the ADM1026 is powered down, unlike the data in the volatile registers. Although referred to as read-only memory, the EEPROM can be written to (as well as read from) via the serial bus in exactly the same way as the other registers. The only major differences between the EEPROM and other registers are:

1. An EEPROM location must be blank before it can be written to. If it contains data, it must first be erased.
2. Writing to EEPROM is slower than writing to RAM.
3. Writing to the EEPROM should be restricted because it has a limited cycle life of 100,000 write operations, due to the usual EEPROM wear-out mechanisms.

The EEPROM in the ADM1026 has been qualified for two key EEPROM memory characteristics: memory cycling endurance and memory data retention.

Endurance qualifies the ability of the EEPROM to be cycled through many Program, Read, and Erase cycles. In real terms, a single endurance cycle is composed of four independent, sequential events. These events are defined as follows:

(a) initial page erase sequence

(b) read/verify sequence

(c) program sequence

(d) second read/verify sequence

In reliability qualification, every byte is cycled from 00h to FFh until a first fail is recorded, signifying the endurance limit of the EEPROM memory.

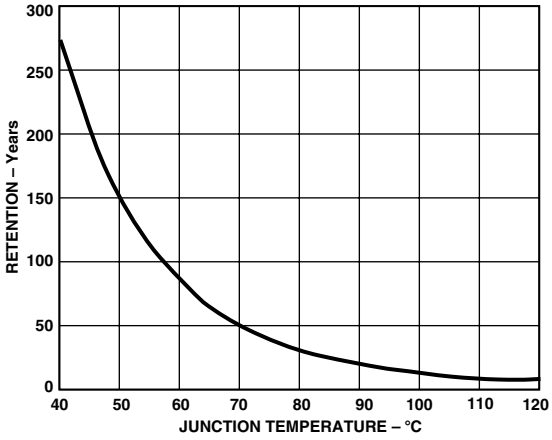


Figure 2. Typical EEPROM Memory Retention

Retention quantifies the ability of the memory to retain its programmed data over time. The EEPROM in the ADM1026 has been qualified in accordance with the formal JEDEC Retention Lifetime Specification (A117) at a specific junction temperature (T_J = 55°C) to guarantee a minimum of 10 years retention time. As part of this qualification procedure, the EEPROM memory is cycled to its specified endurance limit described above before data retention is characterized. This means that the EEPROM memory is guaranteed to retain its data for its full specified retention lifetime every time the EEPROM is reprogrammed. It should be noted that retention lifetime based on an activation energy of 0.6 V will derate with T_J, as shown in Figure 2.

Serial Bus Interface

Control of the ADM1026 is carried out via the serial System Management Bus (SMBus). The ADM1026 is connected to this bus as a slave device, under the control of a master device.

The ADM1026 has a 7-bit serial bus slave address. When the device is powered up, it will do so with a default serial bus address. The five MSB's of the address are set to 01011, the two LSB's are determined by the logical states of Pin 15 (ADD/NTESTOUT). This is a three-state input that can be grounded, connected to V_{CC}, or left open-circuit to give three different addresses.

Table I. Address Pin Truth Table

ADD Pin	A1	A0
GND	0	0
No Connect	1	0
V_{CC}	0	1

If ADD is left open-circuit, the default address will be 0101110 (0x5C). ADD is sampled only at power-up on the first valid SMBus transaction, so any changes made while power is on (and the address is locked) will have no effect.

The facility to make hardwired changes to device address allows the user to avoid conflicts with other devices sharing the same serial bus, for example if more than one ADM1026 is used in a system.

General SMBus Timing

Figures 3a and 3b show timing diagrams for general read and write operations using the SMBus. The SMBus specification defines specific conditions for different types of read and write operation, which are discussed later.

The general SMBus protocol* operates as follows:

1. The master initiates data transfer by establishing a START condition, defined as a high to low transition on the serial data line SDA while the serial clock line SCL remains high. This indicates that a data stream will follow. All slave peripherals connected to the serial bus respond to the START condition and shift in the next 8 bits, consisting of a 7-bit slave address (MSB first) plus an R/$\overline{W}$ bit, which determines the direction of the data transfer, i.e. whether data will be written to or read from the slave device (0 = write, 1 = read).

   The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the acknowledge bit, and holding it low during the high period of this clock pulse. All other devices on the bus now remain idle while the selected device waits for data to be read from or written to it. If the R/$\overline{W}$ bit is a 0, then the master will write to the slave device. If the R/$\overline{W}$ bit is a 1, the master will read from the slave device.

2. Data is sent over the serial bus in sequences of nine clock pulses, 8 bits of data followed by an acknowledge bit from the slave device. Data transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, as a low to high transition when the clock is high may be interpreted as a STOP signal.

   If the operation is a write operation, the first data byte after the slave address is a command byte. This tells the slave device what to expect next. It may be an instruction telling the slave device to expect a block write, or it may simply be a register address that tells the slave where subsequent data is to be written.

   Since data can flow in only one direction as defined by the R/$\overline{W}$ bit, it is not possible to send a command to a slave device during a read operation. Before doing a read operation, it may first be necessary to do a write operation to tell the slave what sort of read operation to expect and/or the address from which data is to be read.

3. When all data bytes have been read or written, stop conditions are established. In WRITE mode, the master will pull the data line high during the 10th clock pulse to assert a STOP condition. In READ mode, the master device will release the SDA line during the low period before the 9th clock pulse, but the slave device will not pull it low. This is known as No Acknowledge. The master will then take the data line low during the low period before the 10th clock pulse, then high during the 10th clock pulse to assert a STOP condition.

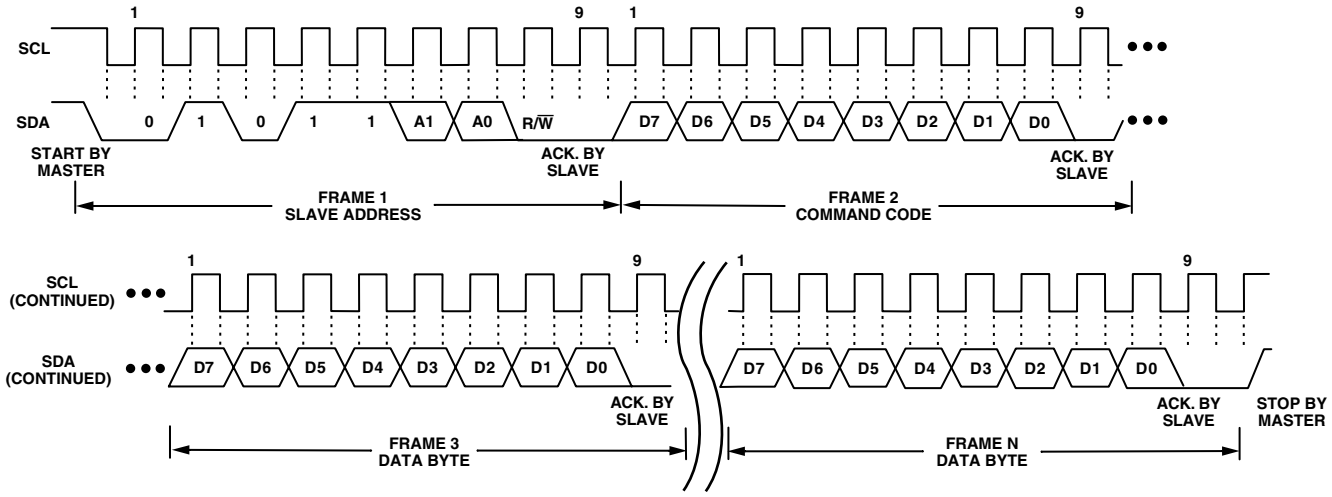


Figure 3a. General SMBus Write Timing Diagram

*If it is required to perform several read or write operations in succession, the master can send a repeat start condition instead of a stop condition to begin a new operation.

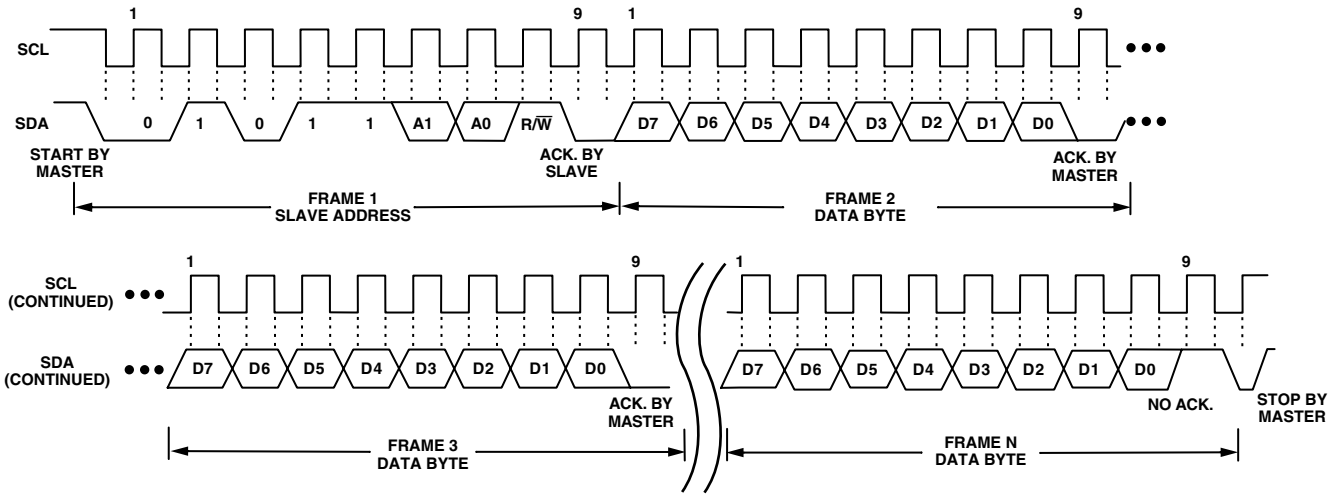


Figure 3b. General SMBus Read Timing Diagram

SMBUS PROTOCOLS FOR RAM AND EEPROM

The ADM1026 contains volatile registers (RAM) and nonvolatile EEPROM. RAM occupies address locations from 00h to 6Fh, while EEPROM occupies addresses from 8000h to 9FFFh.

Data can be written to and read from both RAM and EEPROM as single data bytes and as block (sequential) read or write operations of 32 data bytes, the maximum block size allowed by the SMBus specification.

Data can only be written to unprogrammed EEPROM locations. To write new data to a programmed location, it is first necessary to erase it. EEPROM erasure cannot be done at the byte level; the EEPROM is arranged as 128 pages* of 64 bytes, and an entire page must be erased.

The EEPROM has three RAM registers associated with it, EEPROM Registers 1, 2, and 3 at addresses 06h, 0Ch and 13h. EEPROM Registers 1 and 2 are for factory use only. EEPROM Register 3 is used to set up the EEPROM operating mode.

Setting Bit 0 of EEPROM Register 3 puts the EEPROM into read mode. Setting Bit 1 puts it into Programming Mode. Setting Bit 2 puts it into erase mode.

One, and only one of these bits must be set before the EEPROM may be accessed. Setting no bits or more than one of them will cause the device to respond with No Acknowledge if an EEPROM read, program, or erase operation is attempted.

It is important to distinguish between SMBus write operations, such as sending an address or command, and EEPROM programming operations. It is possible to write an EEPROM address over the SMBus, whatever the state of EEPROM Register 3. However, EEPROM Register 3 must be correctly set before a subsequent EEPROM operation can be performed. For example, when reading from the EEPROM, Bit 0 of EEPROM Register 3 can be set, even though SMBus write operations are required to set up the EEPROM address for reading.

Bit 3 of EEPROM Register 3 is used for EEPROM write protection. Setting this bit will prevent accidental programming or erasure of the EEPROM. If an EEPROM write or erase operation is attempted with this bit set, the ADM1026 will respond with No Acknowledge. This bit is write once and can only be cleared by power ON reset.

EEPROM Register 3 Bit 7 is used for clock extend. Programming an EEPROM byte takes approximately 250 µs, which would limit the SMBus clock for repeated or block write operations. Since EEPROM block read/write access is slow, it is recommended that this Clock Extend bit normally be set to 1. This allows the ADM1026 to pull SCL low and extend the clock pulse when it cannot accept any more data.

ADM1026 SMBus Operations

The SMBus specification defines several protocols for different types of read and write operations. The ones used in the ADM1026 are discussed below. The following abbreviations are used in the diagrams:

S – START	W – WRITE
P – STOP	A – ACKNOWLEDGE
R – READ	$\overline{A}$ – NO ACKNOWLEDGE

The ADM1026 uses the following SMBus write protocols:

Send Byte

In this operation, the master device sends a single command byte to a slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master asserts a STOP condition on SDA and the transaction ends.

In the ADM1026, the send byte protocol is used to write a register address to RAM for a subsequent single byte read from the same address or block read or write starting at that address. This is illustrated in Figure 4a.

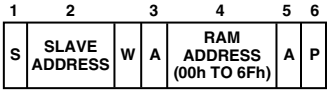


Figure 4a. Setting a RAM Address for Subsequent Read

*Although the EEPROM is arranged into 128 pages, only 124 pages are available to the user. The last four pages are reserved for manufacturing purposes and cannot be erased/rewritten.

If it is required to read data from the RAM immediately after setting up the address, the master can assert a repeat start condition immediately after the final ACK and carry out a single byte read, block read, or block write operation without asserting an intermediate stop condition.

Write Byte/Word

In this operation the master device sends a command byte and one or two data bytes to the slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master sends a data byte.
7. The slave asserts ACK on SDA.
8. The master sends a data byte (or may assert STOP at this point).
9. The slave asserts ACK on SDA.
10. The master asserts a STOP condition on SDA to end the transaction.

In the ADM1026, the write byte/word protocol is used for four purposes. The ADM1026 knows how to respond by the value of the command byte and EEPROM Register 3.

1. Write a single byte of data to RAM. In this case, the command byte is the RAM address from 00h to 6Fh and the (only) data byte is the actual data. This is illustrated in Figure 4b.

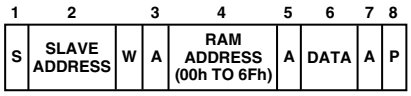


Figure 4b. Single Byte Write To RAM

2. Set up a 2-byte EEPROM address for a subsequent read or block read. In this case, the command byte is the high byte of the EEPROM address from 80h to 9Fh. The (only) data byte is the low byte of the EEPROM address. This is illustrated in Figure 4c.

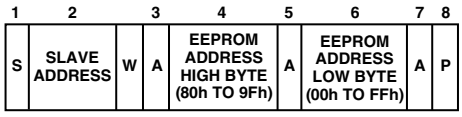


Figure 4c. Setting An EEPROM Address

If it is required to read data from the EEPROM immediately after setting up the address, the master can assert a repeat start condition immediately after the final ACK and carry out a single byte read, or block read operation without asserting an intermediate stop condition. In this case, Bit 0 of EEPROM Register 3 should be set.

3. Erase a page of EEPROM memory. EEPROM memory can be written to only if it is previously erased. Before writing to one or more EEPROM memory locations that are already programmed, the page or pages containing those locations must first be erased. EEPROM memory is erased by writing an EEPROM page address plus an arbitrary byte of data with Bit 2 of EEPROM Register 3 set to 1.

As the EEPROM consists of 128 pages of 64 bytes, the EEPROM page address consists of the EEPROM address high byte (from 80h to 9Fh) and the two MSBs of the low byte. The lower six bits of the EEPROM address low byte only specify addresses within a page and are ignored during an erase operation.

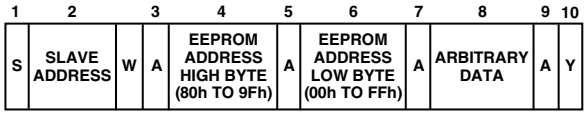


Figure 4d. EEPROM Page Erasure

Page erasure takes approximately 20ms. If the EEPROM is accessed before erasure is complete, the ADM1026 will respond with No Acknowledge.

4. Write a single byte of data to EEPROM. In this case, the command byte is the high byte of the EEPROM address from 80h to 9Fh. The first data byte is the low byte of the EEPROM address and the second data byte is the actual data. Bit 1 of EEPROM Register 3 must be set. This is illustrated in Figure 4e.

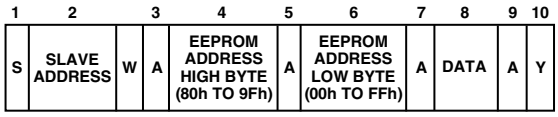


Figure 4e. Single Byte Write To EEPROM

Block Write

In this operation, the master device writes a block of data to a slave device. The start address for a block write must previously have been set. In the case of the ADM1026, this is done by a Send Byte operation to set a RAM address or a Write Byte/Word operation to set an EEPROM address.

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code that tells the slave device to expect a block write. The ADM1026 command code for a block write is A0h (10100000).
5. The slave asserts ACK on SDA.
6. The master sends a data byte (20h) that tells the slave device 32 data bytes will be sent to it. The master should always send 32 data bytes to the ADM1026.
7. The slave asserts ACK on SDA.
8. The master sends 32 data bytes.
9. The slave asserts ACK on SDA after each data byte.
10. The master sends a PEC (Packet Error Checking) byte.
11. The ADM1026 checks the PEC byte and issues an ACK if correct. If incorrect (NACK), the master should resend the data bytes.
12. The master asserts a STOP condition on SDA to end the transaction.

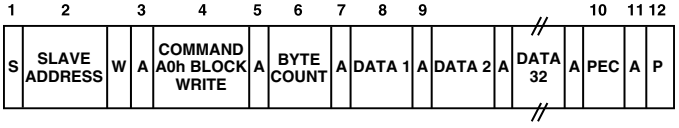


Figure 4f. Block Write To EEPROM or RAM

When performing a block write to EEPROM, Bit 1 of EEPROM Register 3 must be set.

Unlike some EEPROM devices that limit block writes to within a page boundary, there is no limitation on the start address when performing a block write to EEPROM, except:

1. There must be at least 32 locations from the start address to the highest EEPROM address (9FFF) to avoid writing to invalid addresses.
2. If the addresses cross a page boundary, both pages must be erased before programming.

ADM1026 READ OPERATIONS

The ADM1026 uses the following SMBus read protocols:

Receive Byte

In this operation, the master device receives a single byte from a slave device as follows:

1. The master device asserts a START condition on SDA.
2. The master sends the 7-bit slave address followed by the read bit (high).
3. The addressed slave device asserts ACK on SDA.
4. The master receives a data byte.
5. The master asserts NO ACK on SDA.
6. The master asserts a STOP condition on SDA and the transaction ends.

In the ADM1026, the receive byte protocol is used to read a single byte of data from a RAM or EEPROM location whose address has previously been set by a send byte or write byte/word operation. This is illustrated in Figure 4g. When reading from EEPROM, Bit 0 of EEPROM Register 3 must be set.

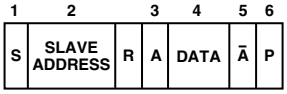


Figure 4g. Single Byte Read From EEPROM or RAM

Block Read

In this operation, the master device reads a block of data from a slave device. The start address for a block read must previously have been set. In the case of the ADM1026 this is done by a Send Byte operation to set a RAM address, or a Write Byte/Word operation to set an EEPROM address. The block read operation itself consists of a Send Byte operation that sends a block read command to the slave, immediately followed by a repeated start and a read operation that reads out multiple data bytes as follows:

1. The master device asserts a START condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code that tells the slave device to expect a block read. The ADM1026 command code for a block read is A1h (10100001).
5. The slave asserts ACK on SDA.
6. The master asserts a repeat start condition on SDA.
7. The master sends the 7-bit slave address followed by the read bit (high).
8. The slave asserts ACK on SDA.
9. The ADM1026 sends a byte count data byte that tells the master how many data bytes to expect. The ADM1026 will always return 32 data bytes (20h), the maximum allowed by the SMBus 1.1 specification.
10. The master asserts ACK on SDA.
11. The master receives 32 data bytes.
12. The master asserts ACK on SDA after each data byte.
13. The ADM1026 issues a PEC byte to the master. The master should check the PEC byte and issue another block read if the PEC byte is incorrect.
14. A NACK is generated after the PEC byte to signal the end of the read.
15. The master asserts a STOP condition on SDA to end the transaction.

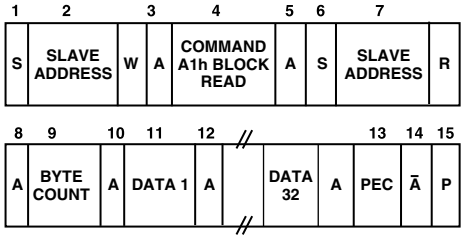


Figure 4h. Block Read From EEPROM or RAM

When block reading from EEPROM, Bit 0 of EEPROM Register 3 must be set.

NOTE

Although the ADM1026 supports Packet Error Checking (PEC), its use is optional. The PEC byte is calculated using CRC-8. The Frame Check Sequence (FCS) conforms to CRC-8 by the polynomial:

$$C(x) = x^8 + x^2 + x^1 + 1$$

Consult the SMBus 1.1 Specification for more information.

MEASUREMENT INPUTS

The ADM1026 has 17 external analog measurement pins, which can be configured to perform various functions. It also measures two supply voltages, 3.3 V MAIN and 3.3 V STBY, and the internal chip temperature.

Pins 25 and 26 are dedicated to remote temperature measurement, while Pins 27 and 28 can be configured as analog inputs with a range of 0 V to 2.5 V or as inputs for a second remote temperature sensor.

Pins 29 to 33 are dedicated to measuring V_{BAT}, +5 V, –12 V, +12 V supplies and the processor core voltage V_{CCP}. The remaining analog inputs, Pins 34 to 41, are general-purpose analog inputs with a range of 0 V to 2.5 V (Pins 34 and 35) or 0 V to 3 V (Pins 36 to 41).

A to D Converter (ADC)

These inputs are multiplexed into the on-chip, successive approximation, analog-to-digital converter. This has a resolution of 8 bits. The basic input range is 0 V to 2.5 V, which is the input range of A_{IN6} to A_{IN9}, but five of the inputs have built-in attenuators to allow measurement of V_{BAT}, +5 V, –12 V, +12 V and the processor core voltage V_{CCP}, without any external components. To allow for the tolerance of these supply voltages, the A to D converter produces an output of 3/4 full scale (decimal 192) for the nominal input voltage, and so has adequate headroom to cope with overvoltages. Table II shows the input ranges of the analog inputs and output codes of the A to D converter (ADC).

When the ADC is running, it samples and converts an analog or local temperature input every 711 µs (typical value). Each input is measured 16 times and the measurements averaged to reduce noise, so the total conversion time for each input is 11.38 ms.

Measurements on the remote temperature (D1 and D2) inputs take 2.13 ms. These are also measured 16 times and averaged, so the total conversion time for a remote temperature input is 34.13 ms.

Voltage Measurement Inputs

The internal structure for all the analog inputs is shown in Figure 5. Each input circuit consists of an input protection diode, an attenuator, plus a capacitor to form a first-order low-pass filter that gives each voltage measurement input immunity to high frequency noise. The –12 V input also has a resistor connected to the on-chip reference to offset the negative voltage range so that it is always positive and can be handled by the ADC. This allows most popular power supply voltages to be monitored directly by the ADM1026 without requiring any additional resistor scaling.

Table II. A to D Output Code vs. V_{IN}

Input Voltage								A to D Output	
+12 V_{IN}	–12 V_{IN}	+5 V_{IN}	3.3 V MAIN 3.3 V STBY	V_{BAT}	V_{CCP}	$A_{IN\ (0–5)}$	$A_{IN\ (6–9)}$	Decimal	Binary
< 0.0625	< –15.928	< 0.026	< 0.0172	< 0.016	< 0.012	< 0.012	< 0.010	0	00000000
0.062–0.125	–15.928–15.855	0.026–0.052	0.017–0.034	0.016–0.031	0.012–0.023	0.012–0.023	0.010–0.019	1	00000001
0.125–0.187	–15.855–15.783	0.052–0.078	0.034–0.052	0.031–0.047	0.023–0.035	0.023–0.035	0.019–0.029	2	00000010
0.188–0.250	–15.783–15.711	0.078–0.104	0.052–0.069	0.047–0.063	0.035–0.047	0.035–0.047	0.029–0.039	3	00000011
0.250–0.313	–15.711–15.639	0.104–0.130	0.069–0.086	0.063–0.077	0.047–0.058	0.047–0.058	0.039–0.049	4	00000100
0.313–0.375	–15.639–15.566	0.130–0.156	0.086–0.103	0.077–0.093	0.058–0.070	0.058–0.070	0.049–0.058	5	00000101
0.375–0.438	–15.566–15.494	0.156–0.182	0.103–0.120	0.093–0.109	0.070–0.082	0.070–0.082	0.058–0.068	6	00000110
0.438–0.500	–15.494–15.422	0.182–0.208	0.120–0.138	0.109–0.125	0.082–0.094	0.082–0.094	0.068–0.078	7	00000111
0.500–0.563	–15.422–15.349	0.208–0.234	0.138–0.155	0.125–0.140	0.094–0.105	0.094–0.105	0.078–0.087	8	00001000
	•								
	•								
	•								
4.000–4.063	–11.375–11.303	1.665–1.691	1.110–1.127	1.000–1.040	0.750–0.780	0.750–0.780	0.625–0.635	64 (¼-scale)	01000000
	•								
	•								
	•								
8.000–8.063	–6.750–6.678	3.330–3.560	2.220–2.237	2.000–2.016	1.500–1.512	1.500–1.512	1.250–1.260	128 (½-scale)	10000000
	•								
	•								
	•								
12.000–12.063	–2.125–2.053	4.995–5.021	3.330–3.347	3.000–3.016	2.250–2.262	2.250–2.262	1.875–1.885	192 (¾-scale)	11000000
	•								
	•								
	•								
15.313–15.375	1.705–1.777	6.374–6.400	4.249–4.267	3.828–3.844	2.871–2.883	2.871–2.883	2.392–2.402	245	11110101
15.375–15.437	1.777–1.850	6.400–6.426	4.267–4.284	3.844–3.860	2.883–2.895	2.883–2.895	2.402–2.412	246	11110110
15.437–15.500	1.850–1.922	6.426–6.452	4.284–4.301	3.860–3.875	2.895–2.906	2.895–2.906	2.412–2.422	247	11110111
15.500–15.563	1.922–1.994	6.452–6.478	4.301–4.319	3.875–3.890	2.906–2.918	2.906–2.918	2.422–2.431	248	11111000
15.562–15.625	1.994–2.066	6.478–6.504	4.319–4.336	3.890–3.906	2.918–2.930	2.918–2.930	2.431–2.441	249	11111001
15.625–15.688	2.066–2.139	6.504–6.530	4.336–4.353	3.906–3.921	2.930–2.941	2.930–2.941	2.441–2.451	250	11111010
15.688–15.750	2.139–2.211	6.530–6.556	4.353–4.371	3.921–3.937	2.941–2.953	2.941–2.953	2.451–2.460	251	11111011
15.750–15.812	2.211–2.283	6.556–6.582	4.371–4.388	3.937–3.953	2.953–2.965	2.953–2.965	2.460–2.470	252	11111100
15.812–15.875	2.283–2.355	6.582–6.608	4.388–4.405	3.953–3.969	2.965–2.977	2.965–2.977	2.470–2.480	253	11111101
15.875–15.938	2.355–2.428	6.608–6.634	4.405–4.423	3.969–3.984	2.977–2.988	2.977–2.988	2.480–2.490	254	11111110
> 15.938	> 2.428	> 6.634	> 4.423	> 3.984	> 2.988	> 2.988	> 2.490	255	11111111

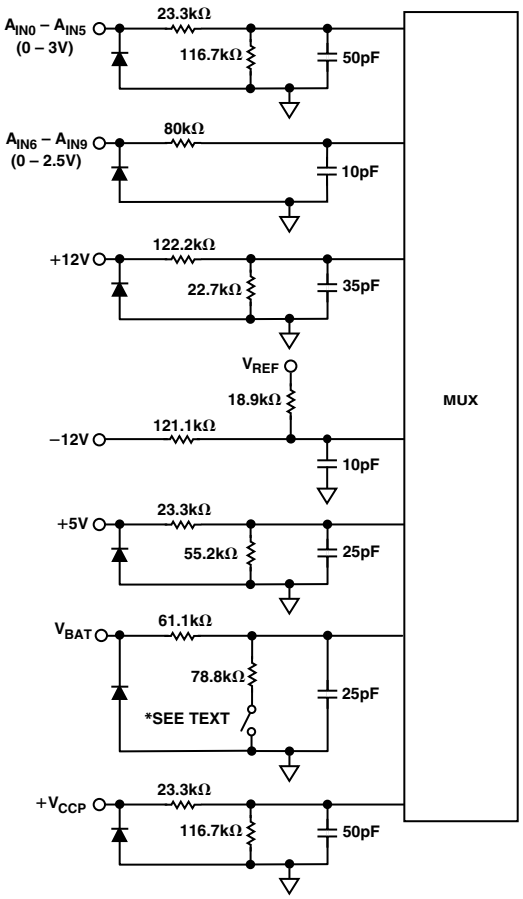


Figure 5. Voltage Measurement Inputs

Setting Other Input Ranges

A_{IN0} to A_{IN9} can easily be scaled to voltages other than 2.5 V or 3 V. If the input voltage range is zero to some positive voltage, then all that is required is an input attenuator, as shown in Figure 6.

However, when scaling A_{IN0} to A_{IN5}, it should be noted that these inputs already have an on-chip attenuator, since their primary function is to monitor SCSI termination voltages. This attenuator will load any external attenuator. The input resistance of the on-chip attenuator can be between 100 kΩ and 200 kΩ. For this tolerance not to affect the accuracy, the output resistance of the external attenuator should be very much lower than this, i.e., 1 kΩ in order to add not more than 1% to the TUE (Total Unadjusted Error). Alternatively, the input can be buffered using an op amp.

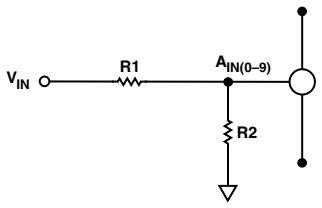


Figure 6. Scaling A_{IN0} – A_{IN9}

$$\frac{R1}{R2} = \frac{(V_{fs} - 3.0)}{3.0} \left(for\ A_{IN0}\ to\ A_{IN5} \right)$$

$$\frac{R1}{R2} = \frac{(V_{fs} - 2.5)}{2.5} \left(for\ A_{IN6}\ to\ A_{IN9} \right)$$

Negative and bipolar input ranges can be accommodated by using a positive reference voltage to offset the input voltage range so that it is always positive.

To monitor a negative input voltage, an attenuator can be used as shown in Figure 7.

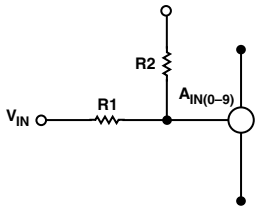


Figure 7. Scaling and Offsetting A_{IN0} – A_{IN9} for Negative Inputs

This offsets the negative voltage so that the ADC always sees a positive voltage. R1 and R2 are chosen so that the ADC input voltage is zero when the negative input voltage is at its maximum (most negative) value, i.e.:

$$\frac{R1}{R2} = \frac{|V_{fs-}|}{V_{OS}}$$

This is a simple and low cost solution, but the following points should be noted:

1. Since the input signal is offset but not inverted, the input range is transposed. An increase in the magnitude of the negative voltage (going more negative) will cause the input voltage to fall and give a lower output code from the ADC. Conversely, a decrease in the magnitude of the negative voltage will cause the ADC code to increase. The maximum negative voltage corresponds to zero output from the ADC. This means that the upper and lower limits will be transposed.
2. For the ADC output to be full scale when the negative voltage is zero, V_{OS} must be greater than the full-scale voltage of the ADC, because V_{OS} is attenuated by R1 and R2. If V_{OS} is equal to or less than the full-scale voltage of the ADC, the input range is bipolar but not necessarily symmetrical.

This is only a problem if the ADC output must be full scale when the negative voltage is zero.

Symmetrical bipolar input ranges can easily be accommodated by making V_{OS} equal to the full-scale voltage of the analog input, and adding a third resistor to set the positive full scale.

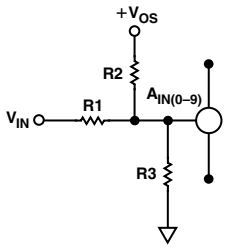


Figure 8. Scaling and Offsetting A_{IN0} – A_{IN9} for Bipolar Inputs

$$\frac{R1}{R2} = \frac{|V_{fs-}|}{V_{OS}}$$

(R3 has no effect as the input voltage at the device pin is zero when V_{IN} = minus full scale)

$$\frac{R1}{R3} = \frac{(V_{fs} - 3.0)}{3.0} \left(for\ A_{IN0}\ to\ A_{IN5}\right)$$

$$\frac{R1}{R3} = \frac{(V_{fs} - 2.5)}{2.5} \left(for\ A_{IN6}\ to\ A_{IN9}\right)$$

(R2 has no effect as the input voltage at the device pin is equal to V_{OS} when V_{IN} = plus full scale).

Battery Measurement Input (V_{BAT})

The V_{BAT} input allows the condition of a CMOS backup battery to be monitored. This is typically a lithium coin cell such as a CR2032. Normally, the battery in a system is required to keep some device powered when the system is in a powered-off state. The V_{BAT} measurement input is specially designed to minimize battery drain. To reduce current drain from the battery, the lower resistor of the V_{BAT} attenuator is not connected, except whenever a V_{BAT} measurement is being made. The total current drain on the V_{BAT} pin is 80 nA typical (for a maximum V_{BAT} voltage = 4 V), so a CR2032 CMOS battery will function in a system in excess of the expected 10 years. Note that when a V_{BAT} measurement is not being made, the current drain is reduced to 6 nA typical. Under normal voltage measurement operating conditions, all measurements are made in a round-robin format, and each reading is actually the result of 16 digitally averaged measurements. However, averaging is not carried out on the V_{BAT} measurement to reduce measurement time and therefore reduce the current drain from the battery. The V_{BAT} current drain when a measurement is being made is calculated by:

$$I = \frac{V_{BAT}}{100\ k\Omega} \times \frac{T_{PULSE}}{T_{PERIOD}}$$

For V_{BAT} = 3 V,

$$I = \frac{3\ V}{100\ k\Omega} \times \frac{711\ \mu s}{273\ ms} = 78\ nA$$

where T_{PULSE} = V_{BAT} measurement time (711 µs typical), T_{PERIOD} = time to measure all analog inputs (273 ms typical), and V_{BAT} input battery protection.

V_{BAT} Input Battery Protection

In addition to minimizing battery current drain, the V_{BAT} measurement circuitry was specifically designed with battery protection in mind. Internal circuitry prevents the battery from being back-biased by the ADM1026 supply or through any other path under normal operating conditions. In the unlikely event of some catastrophic ADM1026 failure, the ADM1026 includes a second level of battery protection including a series 3 kΩ resistor to limit current to the battery, as recommended by UL. It is therefore not necessary to add a series resistor between the battery and the V_{BAT} input; the battery should be connected directly to the V_{BAT} input to improve voltage measurement accuracy.

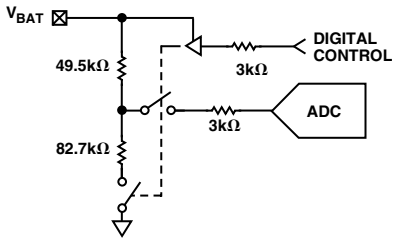


Figure 9. Equivalent V_{BAT} Input Protection Circuit

Reference Output (V_{REF})

The ADM1026 offers an on-chip reference voltage (Pin 24) that can be used to provide a 1.82 V or 2.5 V reference voltage output. This output is buffered and specified to sink or source a load current of 2 mA. The reference voltage outputs 1.82 V if Bit 2 of Configuration Register 3 (address 07h) is 0; it outputs 2.5 V when this bit is set to 1. This voltage reference output can be used to provide a stable reference voltage to external circuitry such as LDOs. The load regulation of the V_{REF} output is typically 0.15% for a sink current of 2 mA and 0.15% for 2 mA source current. There may be some ripple present on the V_{REF} output that requires filtering (±4 m V_{MAX}). Figure 11 shows the recommended circuitry for the V_{REF} output for loads less than 2 mA. For loads in excess of 2 mA, external circuitry, such as that shown in Figure 12, should be used to buffer the V_{REF} output.

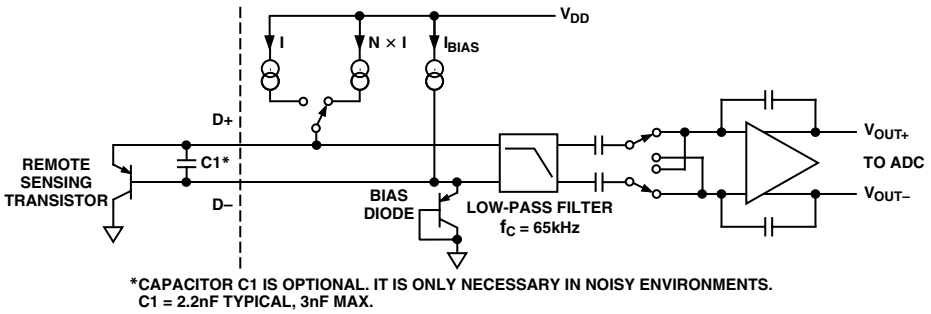


Figure 10. Signal Conditioning for Remote Diode Temperature Sensors

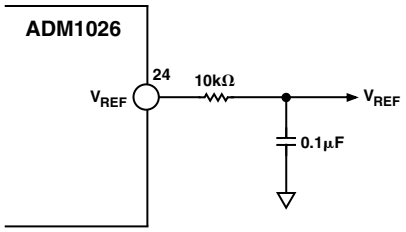


Figure 11. V_{REF} Interface Circuit for V_{REF} Loads < 2 mA

If the V_{REF} output is not being used, it should be left unconnected. Do not connect V_{REF} to GND using a capacitor. The internal output buffer on the voltage reference will be capacitively loaded and this can cause the voltage reference to oscillate. This will affect temperature readings reported back by the ADM1026. The recommended interface circuit for the V_{REF} output is shown in Figure 12.

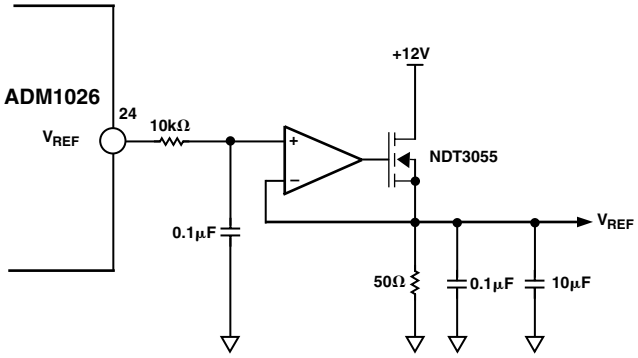


Figure 12. V_{REF} Interface Circuit for V_{REF} Loads > 2 mA

TEMPERATURE MEASUREMENT SYSTEM

Local Temperature Measurement

The ADM1026 contains an on-chip bandgap temperature sensor whose output is digitized by the on-chip ADC. The temperature data is stored in the Local Temperature Value Register (address 1Fh). As both positive and negative temperatures can be measured, the temperature data is stored in two's complement format, as shown in Table III. Theoretically, the temperature sensor and ADC can measure temperatures from –128°C to +127°C with a resolution of 1°C. However, temperatures below T_{MIN} and above T_{MAX} are outside the operating temperature range of the device, so local temperature measurements outside this range are not possible. Temperature measurement from –128°C to +127°C is possible using a remote sensor.

Remote Temperature Measurement

The ADM1026 can measure the temperature of two remote diode sensors or diode-connected transistors, connected to Pins 25 and 26, or 27 and 28.

Pins 25 and 26 are a dedicated temperature input channel. Pins 27 and 28 can be configured to measure a diode sensor by clearing Bit 3 of Configuration Register 1 (address 00h) to 0. If this bit is 1, then Pins 27 and 28 are A_{IN8} and A_{IN9}.

The forward voltage of a diode or diode-connected transistor, operated at a constant current, exhibits a negative temperature coefficient of about –2 mV/°C. Unfortunately, the absolute value of V_{be} varies from device to device, and individual calibration is required to null this out, so the technique is unsuitable for mass production.

The technique used in the ADM1026 is to measure the change in V_{be} when the device is operated at two different currents, given by:

$$\Delta V_{be} = \frac{K \times T}{q} \times \log n(N)$$

where K is Boltzmann's constant, q is charge on the carrier, T is absolute temperature in Kelvins, and N is the ratio of the two currents.

Figure 10 shows the input signal conditioning used to measure the output of a remote temperature sensor. This figure shows the external sensor as a substrate transistor provided for temperature monitoring on some microprocessors, but it could equally well be a discrete transistor such as a 2N3904.

If a discrete transistor is used, the collector will not be grounded and should be linked to the base. If a PNP transistor is used, the base is connected to the D– input and the emitter to the D+ input. If an NPN transistor is used, the emitter is connected to the D– input and the base to the D+ input.

To prevent ground noise interfering with the measurement, the more negative terminal of the sensor is not referenced to ground but is biased above ground by an internal diode at the D– input.

To measure ΔV_{be}, the sensor is switched between operating currents of I and N × I. The resulting waveform is passed through a 65 kHz low-pass filter to remove noise, and to a chopper-stabilized amplifier that performs the functions of amplification and rectification of the waveform to produce a DC voltage proportional to ΔV_{be}. This voltage is measured by the ADC to give a temperature output in 8-bit two's complement format. To further reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles. A remote temperature measurement takes nominally 2.14 ms.

The results of external temperature measurements are stored in 8-bit, two's complement format, as illustrated in Table III.

Table III. Temperature Data Format

Temperature	Digital Output
–128°C	1000 0000
–125°C	1000 0011
–100°C	1001 1100
–75°C	1011 0101
–50°C	1100 1110
–25°C	1110 0111
–10°C	11110110
0°C	0000 0000
+10°C	0000 1010
+25°C	0001 1001
+50°C	0011 0010
+75°C	0100 1011
+100°C	0110 0100
+125°C	0111 1101
+127°C	0111 1111

Layout Considerations

Digital boards can be electrically noisy environments and care must be taken to protect the analog inputs from noise, particularly when measuring the very small voltages from a remote diode sensor. The following precautions should be taken:

1. Place the ADM1026 as close as possible to the remote sensing diode. Provided that the worst noise sources such as clock generators, data/address buses and CRTs are avoided, this distance can be 4 to 8 inches.
2. Route the D+ and D– tracks close together, in parallel, with grounded guard tracks on each side. Provide a ground plane under the tracks if possible.
3. Use wide tracks to minimize inductance and reduce noise pickup. 10 mil track minimum width and spacing is recommended.

Figure 13. Arrangement of Signal Tracks

4. Try to minimize the number of copper/solder joints, which can cause thermocouple effects. Where copper/solder joints are used, make sure that they are in both the D+ and D– path and at the same temperature.

   Thermocouple effects should not be a major problem as 1°C corresponds to about 240 μV, and thermocouple voltages are about 3 μV/°C of temperature difference. Unless there are two thermocouples with a big temperature differential between them, thermocouple voltages should be much less than 200 mV.
5. Place a 0.1 μF bypass capacitor close to the ADM1026.
6. If the distance to the remote sensor is more than 8 inches, the use of twisted pair cable is recommended. This will work up to about 6 to 12 feet.
7. For very long distances (up to 100 feet), use shielded twisted pair such as Belden #8451 microphone cable. Connect the twisted pair to D+ and D– and the shield to GND close to the ADM1026. Leave the remote end of the shield unconnected to avoid ground loops.

Because the measurement technique uses switched current sources, excessive cable and/or filter capacitance can affect the measurement. When using long cables, the filter capacitor may be reduced or removed.

Cable resistance can also introduce errors. 1 Ω series resistance introduces about 0.5°C error.

Limit Values

Limit values for analog measurements are stored in the appropriate limit registers. In the case of voltage measurements, high and low limits can be stored so that an interrupt request will be generated if the measured value goes above or below acceptable values. In the case of temperature, a hot temperature or high limit can be programmed, and a hot temperature hysteresis or low limit, which will usually be some degrees lower. This can be useful as it allows the system to be shut down when the hot limit is exceeded, and restarted automatically when it has cooled down to a safe temperature.

Analog Monitoring Cycle Time

The analog monitoring cycle begins when a one is written to the start bit (Bit 0), and a 0 to the INT_Clear bit (Bit 2) of the configuration register. INT_Enable (Bit 1) should be set to one to enable the INT output. The ADC measures each analog input in turn, starting with remote temperature channel 1 and ending with local temperature. As each measurement is completed the result is automatically stored in the appropriate value register. This "round-robin" monitoring cycle continues until it is disabled by writing a 0 to Bit 0 of the Configuration Register.

As the ADC will normally be left to free-run in this manner, the time taken to monitor all the analog inputs will normally not be of interest, as the most recently measured value of any input can be read out at any time.

For applications where the monitoring cycle time is important, it can easily be calculated.

The total number of channels measured is:

Five dedicated supply voltage inputs
Ten general purpose analog inputs
3.3 V MAIN
3.3 V STBY
Local temperature
Two remote temperature

Pins 28 and 27 are measured both as analog inputs A_{IN8}/A_{IN9} and as remote temperature input D2+/D2–, irrespective of which configuration is selected for these pins.

If Pins 28 and 27 are configured as A_{IN8}/A_{IN9}, the measurements for these channels are stored in Registers 27h and 29h and the invalid temperature measurement is discarded. On the other hand, if Pins 28 and 27 are configured as D2+/D2–, the temperature measurement is stored in Register 29h and there will be no valid result in Register 27h.

As mentioned previously, the ADC performs a conversion every 711 μs on the analog and local temperature inputs and every 2.13 ms on the remote temperature inputs. Each input is measured 16 times and averaged to reduce noise.

The total monitoring cycle time for voltage and temperature inputs is therefore nominally:

$$(18 \times 16 \times 0.711) + (2 \times 16 \times 2.13) = 273\ ms$$

The ADC uses the internal 22.5 kHz clock, which has a tolerance of ±6%, so the worst case monitoring cycle time is 290 ms. The fan speed measurement uses a completely separate monitoring loop, as described later.

Input Safety

Scaling of the analog inputs is performed on-chip, so external attenuators are normally not required. However, since the power supply voltages will appear directly at the pins, it is advisable to add small external resistors (i.e., 500 Ω) in series with the supply traces to the chip to prevent damaging the traces or power supplies should an accidental short such as a probe connect two power supplies together.

As the resistors will form part of the input attenuators, they will affect the accuracy of the analog measurement if their value is too high.

The worst such accident would be connecting –12 V to +12 V– a total of 24 V difference. With the series resistors, this would draw a maximum current of approximately 24 mA.

ANALOG OUTPUT

The ADM1026 has a single analog output from an unsigned 8-bit DAC that produces 0 V to 2.5 V (independent of the reference voltage setting). The input data for this DAC is contained in the DAC control register (address 04h) The DAC control register defaults to FFh during power ON reset, which produces maximum fan speed. The analog output may be amplified and buffered with external circuitry such as an op amp and transistor to provide fan speed control. During automatic fan speed control, described later, the four MSBs of this register set the minimum fan speed.

Suitable fan drive circuits are given in Figures 14a to 14e. When using any of these circuits, the following points should be noted:

1. All of these circuits will provide an output range from zero to almost +12 V, apart from Figure 14a, which loses the base-emitter voltage drop of Q1 due to the emitter-follower configuration.
2. To amplify the 2.5 V range of the analog output up to 12 V, the gain of these circuits needs to be around 4.8.
3. Care must be taken when choosing the op amp to ensure that its input common-mode range and output voltage swing are suitable.
4. The op amp may be powered from the +12 V rail alone or from ±12 V. If it is powered from +12 V then the input common-mode range should include ground to accommodate the minimum output voltage of the DAC, and the output voltage should swing below 0.6 V to ensure that the transistor can be turned fully off.
5. If the op amp is powered from –12 V then precautions such as a clamp diode to ground may be needed to prevent the base-emitter junction of the output transistor being reverse-biased in the unlikely event that the output of the op amp should swing negative for any reason.
6. In all these circuits, the output transistor must have an I_{CMAX} greater than the maximum fan current, and be capable of dissipating power due to the voltage dropped across it when the fan is not operating at full speed.
7. If the fan motor produces a large back EMF when switched off, it may be necessary to add clamp diodes to protect the output transistors in the event that the output goes from full scale to zero very quickly.

PWM Output

Fan speed may also be controlled using pulsewidth modulation (PWM). The PWM output (Pin 18) produces a pulsed output with a frequency of approximately 75 Hz and a duty cycle defined by the contents of the PWM Control Register (address 05h). During automatic fan speed control, described below, the four MSBs of this register set the minimum fan speed.

The open drain PWM output must be amplified and buffered to drive the fans. The PWM output is intended to be used with an NMOS driver, but may be inverted by setting Bit 1 of Test Register 1 (address 14h) if using PMOS drivers. Figure 14f shows how a fan may be driven under PWM control using an N-channel MOSFET.

Automatic Fan Speed Control

The ADM1026 offers a simple method of controlling fan speed according to temperature without intervention from the host processor.

To enable automatic fan speed control, monitoring must be enabled by setting Bit 0 of Configuration Register 1 (address 00h).

Automatic fan speed control can be applied to the DAC output, the PWM output, or both, by setting Bit 5 and/or Bit 6 of Configuration Register 1.

The T_{MIN} registers (addresses 10h to 12h) contain minimum temperature values for the three temperature channels (on-chip sensor and two remote diodes). This is the temperature at which a fan will start to operate when the temperature sensed by the controlling sensor exceeds T_{MIN}. T_{MIN} can be the same or different for all three channels. T_{MIN} is set by writing a two's complement temperature value to the T_{MIN} registers. If any sensor channel is not required for automatic fan speed control, T_{MIN} for that channel should be set to +127°C (01111111).

In Automatic Fan Speed Control Mode, (Figure 15a and 15b) the four MSBs of the DAC Control Register (address 04h) and PWM Control Register (address 05h) set the minimum values for the DAC and PWM outputs. Note, if both DAC Control and PWM Control is enabled (Bits 5 and 6 of Configuration Register 1 = 1), the four MSBs of the DAC Control Register (address 04h) define the minimum fan speed values for both the DAC and PWM outputs. The value in the PWM Control Register (address 05h) has no effect.

$$Minimum\ DAC\ Code\ DAC_{MIN} = 16 \times D$$

$$DAC\ Output\ Voltage = 2.5 \times \frac{Code}{256}$$

$$Minimum\ PWM\ Duty\ Cycle\ PWM_{MIN} = 6.67 \times D$$

where D is the decimal equivalent of Bits 7 to 4 of the register.

When the temperature measured by any of the sensors exceeds the corresponding T_{MIN}, the fan is spun up for 2 seconds with the fan drive set to maximum (full scale from the DAC or 100% PWM duty cycle. The fan speed is then set to the minimum as previously defined. As the temperature increases, the fan drive will increase until the temperature reaches T_{MIN} + 20°C.

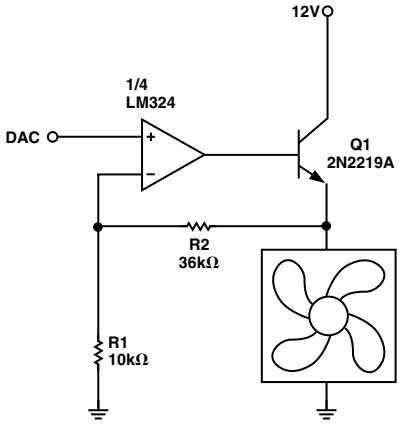


Figure 14a. Fan Drive Circuit with Op Amp and Emitter–Follower

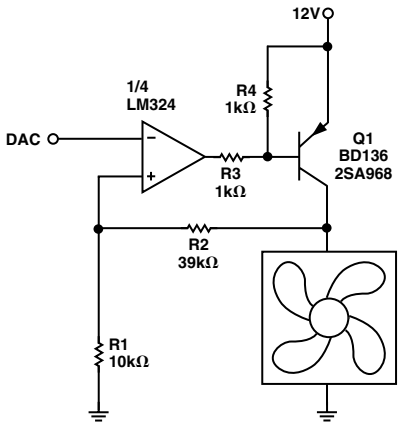


Figure 14b. Fan Drive Circuit with Op Amp and PNP Transistor

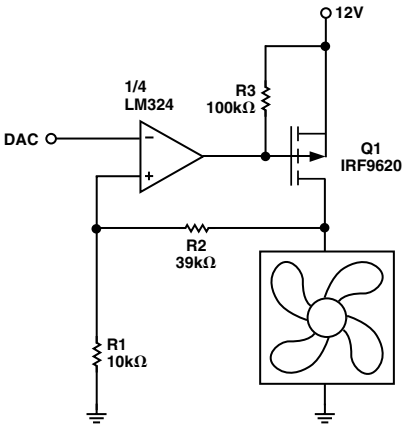


Figure 14c. Fan Drive Circuit with Op Amp and P-Channel MOSFET

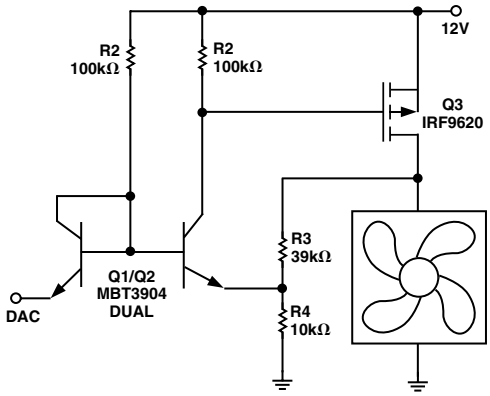


Figure 14d. Discrete Fan Drive Circuit with P-Channel MOSFET, Single Supply

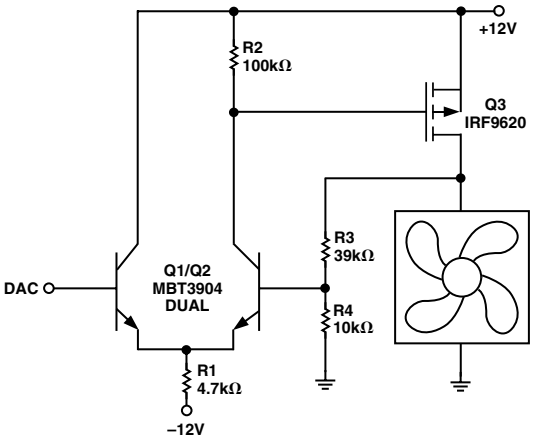


Figure 14e. Discrete Fan Drive Circuit with P-Channel MOSFET, Dual Supply

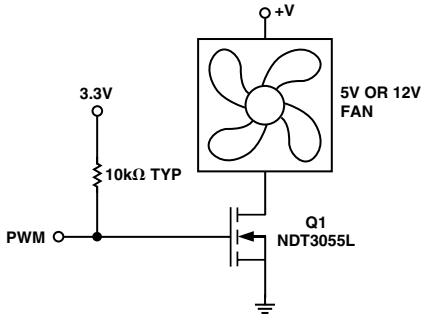


Figure 14f. PWM Fan Drive Circuit Using an N-Channel MOSFET

The fan drive at any temperature up to 20°C above T_{MIN} is given by:

$$PWM = PWM_{MIN} + \left(100 - PWM_{MIN}\right) \times \frac{T_{ACTUAL} - T_{MIN}}{20}$$

or,

$$DAC = DAC_{MIN} + \left(240 - DAC_{MIN}\right) \times \frac{T_{ACTUAL} - T_{MIN}}{20}$$

For simplicity of the automatic fan speed algorithm, the DAC code increases linearly up to 240, not its full scale of 255. However, when the temperature exceeds T_{MIN} +20°C, the DAC output will jump to full scale. To ensure that the maximum cooling capacity is always available, the fan drive is always set by the sensor channel demanding the highest fan speed.

If the temperature falls, the fan will not turn off until the temperature measured by all three temperature sensors has fallen to their corresponding T_{MIN} – 4°C. This prevents the fan from cycling on and off continuously when the temperature is close to T_{MIN}.

Whenever a fan starts or stops during automatic fan speed control, a one-off interrupt is generated at the INT output. This is described in more detail in the section on the ADM1026 Interrupt Structure.

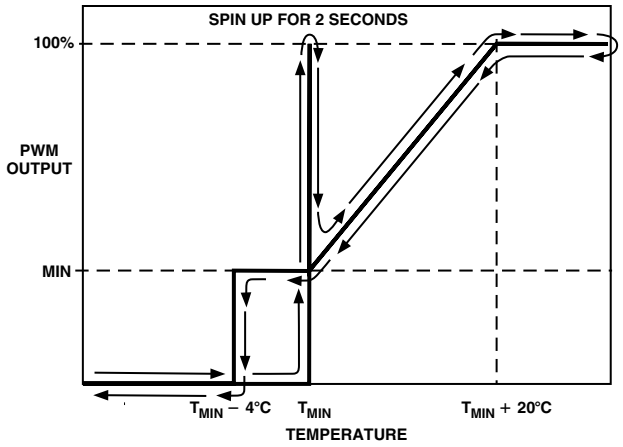


Figure 15a. Automatic PWM Fan Control Transfer Function

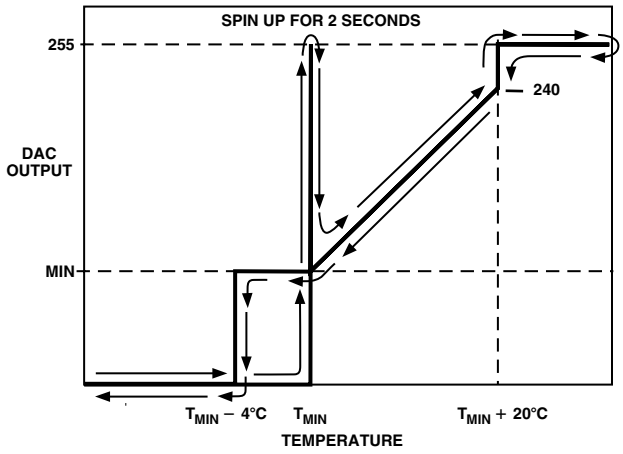


Figure 15b. Automatic DAC Fan Control Transfer Function

Fan Inputs

Pins 3 to 6 and 9 to 12 may be configured as fan speed measuring inputs by clearing the corresponding bit(s) of Configuration Register 2 (Address 01h), or as general-purpose logic inputs/outputs by setting bits in this register. The power-on default value for this register is 00h, which means all the inputs are set for fan speed measurement.

Signal conditioning in the ADM1026 accommodates the slow rise and fall times typical of fan tachometer outputs. The Fan Tach inputs have internal 10 kΩ pull-up resistors to 3.3 V STBY. In the event that these inputs are supplied from fan outputs that exceed the supply, either resistive attenuation of the fan signal or diode clamping must be included to keep inputs within an acceptable range.

Figures 16a to 16d show circuits for most common fan tacho outputs.

If the fan tacho output is open-drain or has a resistive pull-up to V_{CC}, then it can be connected directly to the fan input, as shown in Figure 16a.

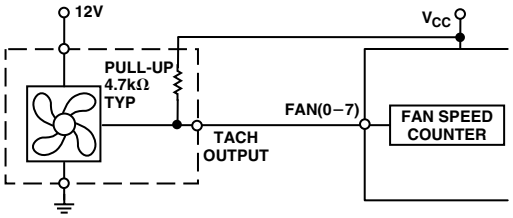


Figure 16a. Fan With Tach Pull-Up To +V_{CC}

If the fan output has a resistive pull-up to +12 V (or other voltage greater than 3.3 V STBY) then the fan output can be clamped with a zener diode, as shown in Figure 16b. The zener voltage should be chosen so that it is greater than V_{IH} but less than 3.3 V STBY, allowing for the voltage tolerance of the zener.

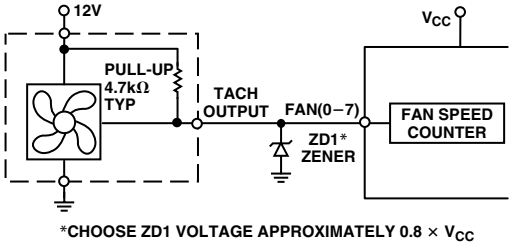


Figure 16b. Fan with Tach Pull-Up to Voltage >V_{CC} (e.g. 12 V) Clamped with Zener Diode

If the fan has a strong pull-up (less than 1k Ω) to +12 V, or a totem-pole output, then a series resistor can be added to limit the zener current, as shown in Figure 16c. Alternatively, a resistive attenuator may be used, as shown in Figure 16d.

R1 and R2 should be chosen such that:

$$2V < V_{PULLUP} \times \frac{R2}{\left(R_{PULLUP} + R1 + R2\right)} < 3.3V\ STBY$$

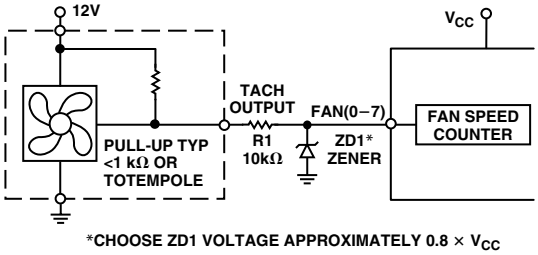


Figure 16c. Fan with Strong Tach Pull-Up to > V_{CC} or Totem Pole Output, Clamped with Zener and Resistor

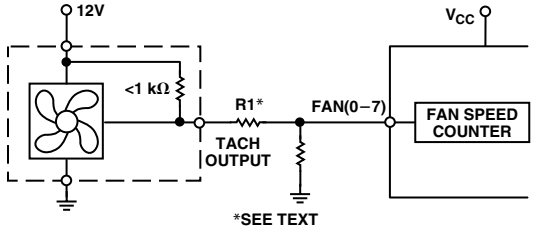


Figure 16d. Fan with Strong Tach Pull-Up to >V_{CC} or Totem Pole Output, Attenuated with R1/R2

FAN SPEED MEASUREMENT

The fan counter does not count the fan tacho output pulses directly because the fan speed may be less than 1000 RPM and it would take several seconds to accumulate a reasonably large and accurate count. Instead, the period of the fan revolution is measured by gating an on-chip 22.5 kHz oscillator into the input of an 8-bit counter for two periods of the fan tacho output, as shown in Figure 17, so the accumulated count is actually proportional to the fan tacho period and inversely proportional to the fan speed.

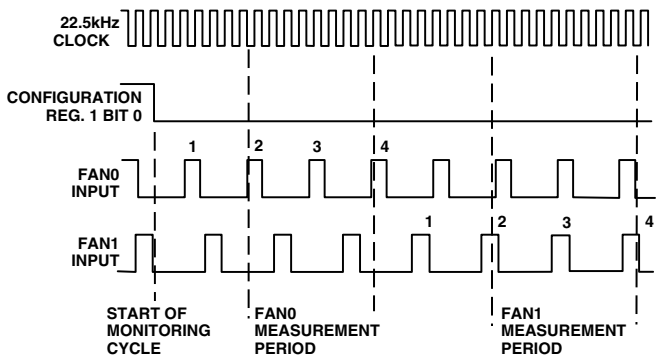


Figure 17. Fan Speed Measurement

The monitoring cycle begins when a 1 is written to the Monitor bit (Bit 0 of Configuration Register 1). The INT_Enable (Bit 1) should be set to one to enable the INT output.

The fan speed counter starts counting as soon as the Fan Channel has been switched to. If the Fan Tach Count reaches 0xFF, the fan has failed or is not connected. If a fan is connected and running, the counter gets reset on the second tach rising edge, and oscillator pulses are actually counted from the second rising tach edge to the fourth rising edge. The measurement then switches to the next fan channel. Here again, the counter begins counting and is reset on the second tach rising edge, and oscillator pulses are counted from the second rising edge to the fourth rising edge. This is repeated for the other six fan channels.

Note that fan speed measurement does not occur until 1.8 seconds after the monitor bit has been set. This is to allow the fans adequate time to spin up. Otherwise, the ADM1026 could generate false fan failure interrupts. During the 1.8 second fan spin-up time, all Fan Tach Registers read 0x00.

To accommodate fans of different speed and/or different numbers of output pulses per revolution, a pre-scaler (divisor) of 1, 2, 4, or 8 may be added before the counter. Divisor values for Fans 0 to 3 are contained in the Fan 0–3 Divisor Register (Address 02h) and those for Fans 4 to 7 in the Fan 4–7 Divisor Register (Address 03h). The default value is 2, which gives a count of 153 for a fan running at 4400 RPM producing two output pulses per revolution.

The count is calculated by the equation:

$$Count = \frac{27.5 \times 10^3 \times 60}{RPM \times Divisor}$$

For constant speed fans, fan failure is normally considered to have occurred when the speed drops below 70% of nominal, which would correspond to a count of 219. Full scale (255) would be reached if the fan speed fell to 60% of its nominal value. For temperature-controlled variable speed fans, the situation will be different.

Table IV shows the relationship between fan speed and time per revolution at 60%, 70%, and 100% of nominal RPM for fan speeds of 1100, 2200, 4400, and 8800 RPM, and the divisor that would be used for each of these fans, based on two tacho pulses per revolution.

Table IV. Fan Speeds and Divisors

Divisor RPM	Nominal Rev	Time per RPM (ms)	70%	Time per Rev (70%) (ms)	60% RPM	Time per Rev (60%) (ms)
÷ 1	8800	6.82	6160	9.74	5280	11.36
÷ 2	4400	13.64	3080	19.48	2640	22.73
÷ 4	2200	27.27	1540	38.96	1320	45.45
÷ 8	1100	54.54	770	77.92	660	90.9

Limit Values

Fans generally do not overspeed if run from the correct voltage, so the failure condition of interest is underspeed due to electrical or mechanical failure. For this reason, only low speed limits are programmed into the limit registers for the fans. It should be noted that since fan period rather than speed is being measured, a fan failure interrupt will occur when the measurement exceeds the limit value.

Fan Monitoring Cycle Time

The fan speeds are measured in sequence from 0 to 7. The monitoring cycle time depends on the fan speed, the number of tacho output pulses per revolution and the number of fans being monitored.

If a fan is stopped or running so slowly that the fan speed counter reaches 255 before the second tach pulse after initialization, or before the fourth tach pulse during measurement, the measurement will be terminated. This will also occur if an input is configured as GPIO instead of fan. Any channels so connected will time out after 255 clock pulses.

The worst-case measurement time for a fan-configured channel occurs when the counter reaches 254 from start to the second tach pulse and reaches 255 after the second tach pulse. Taking into account the tolerance of the oscillator frequency, the worst-case measurement time is:

$$509 \times D \times 0.047\ ms$$

where:
509 is the total number of clock pulses.
D is the divisor: 1, 2, 4, or 8.
0.047 is the worst-case oscillator period in ms.
The worst-case fan monitoring cycle time is the sum of the worst case measurement time for each fan.

Although the fan monitoring cycle and the analog input monitoring cycle are started together, they are not synchronized in any other way.

Chassis Intrusion Input

The Chassis Intrusion input is an active high input intended for detection and signalling of unauthorized tampering with the system. When this input goes high, the event is latched in Bit 6 of Status Register 4 and an interrupt will be generated. The bit will remain set until cleared by writing a 0 to it, so long as battery voltage is connected to the V_{BAT} input, even if the ADM1026 is powered off.

The CI input will detect chassis intrusion events even when the ADM1026 is powered off (provided battery voltage is applied to

V_{BAT}) but will not immediately generate an interrupt. Once a chassis intrusion event has been detected and latched, an interrupt will be generated when the system is powered up.

The actual detection of chassis intrusion is performed by an external circuit that will detect, for example, when the cover has been removed. A wide variety of techniques may be used for the detection, for example:

- A microswitch that opens or closes when the cover is removed.
- Reed switch operated by magnet fixed to the cover.
- Hall-effect switch operated by magnet fixed to the cover.
- Phototransistor that detects light when cover is removed.

The chassis intrusion input can also be used for other types of alarm input. Figure 18 shows a temperature alarm circuit using an AD22105 temperature switch sensor. This produces a low-going output when the preset temperature is exceeded, so the output is inverted by Q1 to make it compatible with the CI input. Q1 can be almost any small-signal NPN transistor, or a TTL or CMOS inverter gate may be used if one is available. See the AD22105 data sheet for information on selecting R_{SET}.

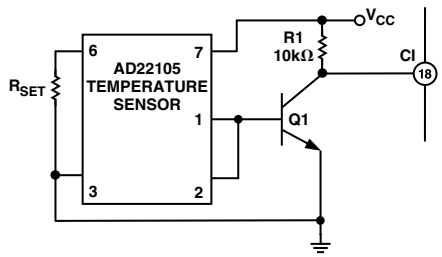


Figure 18. Using the CI Input with a Temperature Sensor

GENERAL-PURPOSE I/O PINS (OPEN DRAIN)

The ADM1026 has eight pins that are dedicated to general-purpose logic input/output (Pins 1, 2, and 43 to 48), eight pins that can be configured as general-purpose logic pins or fan speed inputs (Pins 3 to 6, and 9 to 12), and one pin that can be configured as GPIO16 or the bidirectional THERM pin (Pin 42). The GPIO/FAN pins are configured as general-purpose logic pins by setting Bits 0 to 7 of Configuration Register 2 (Address 01h). Pin 42 is configured as GPIO16 by setting Bit 0 of Configuration Register 3, or as the THERM function by clearing this bit.

Each GPIO pin has four data bits associated with it, two bits in one of the GPIO Configuration Registers (Addresses 08h to 0Bh), one in the GPIO Status Registers (Addresses 24h and 25h), and one in the GPIO Mask Registers (Addresses 1Ch and 1Dh)

SETTING a Direction Bit = 1 in one of the GPIO configuration registers makes the corresponding GPIO pin an OUTPUT. CLEARING the direction bit to 0 makes it an INPUT.

SETTING a Polarity Bit = 1 in one of the GPIO configuration registers makes the corresponding GPIO pin active HIGH. CLEARING the polarity bit to 0 makes it active LOW.

When a GPIO pin is configured as an INPUT, the corresponding bit in one of the GPIO status registers is read-only, and is set when the input is asserted ("asserted" may be high or low depending on the setting of the Polarity Bit).

When a GPIO pin is configured as an OUTPUT, the corresponding bit in one of the GPIO status registers becomes read/write. Setting this bit will then assert the GPIO output. (Here again, "asserted" may be high or low depending on the setting of the polarity bit.)

The effect of a GPIO Status Register bit on the INT output can be masked out by setting the corresponding bit in one of the GPIO mask registers. When the pin is configured as an output, this bit will automatically be masked to prevent the data written to the status bit from causing an interrupt, with the exception of GPIO16, which must be masked manually by setting Bit 7 of Mask Register 4 (Reg 1Bh).

When configured as inputs, the GPIO pins may be connected to external interrupt sources such as temperature sensors with digital output. Another application of the GPIO pins would be to monitor a processor's Voltage ID code (VID code).

The ADM1026 Interrupt Structure

The Interrupt Structure of the ADM1026 is shown in Figure 19. Interrupts can come from a number of sources, which are combined to form a common $\overline{INT}$ output. When $\overline{INT}$ is asserted, this output pulls low. The $\overline{INT}$ pin has an internal, 100 kΩ pull-up resistor.

1. Analog/Temperature Inputs. As each analog measurement value is obtained and stored in the appropriate value register, the value and the limits from the corresponding limit registers are fed to the high and low limit comparators. The ADM1026 performs greater than comparisons to the high limits. An out-of-limit is also generated if a result is less than or equal to a low limit. The result of each comparison (1 = out of limit, 0 = in limit) is routed to the corresponding bit input of Interrupt Status Register 1, 2, or 4 via a data demultiplexer, and used to set that bit high or low as appropriate. Status bits are self-clearing. If a bit in a status register is set due to an out-of-limit measurement, it will continue to cause $\overline{INT}$ to be asserted as long as it remains set, as described below. However, if a subsequent measurement is in limit it will be reset and will not cause $\overline{INT}$ to be reasserted. Status bits are unaffected by clearing the interrupt.

   Interrupt Mask Registers, 1, 2, and 4 have bits corresponding to each of the interrupt status register bits. Setting an interrupt mask bit high forces the corresponding status bit output low, while setting an interrupt mask bit low allows the corresponding status bit to be asserted. After mask gating, the status bits are all OR'd together to produce the analog and fan interrupt, which is used to set a latch. The output of this latch is OR'd with other interrupt sources to produce the $\overline{INT}$ output. This will pull low if any unmasked status bit goes high, i.e. when any measured value goes out of limit.

   When an $\overline{INT}$ output due to an out-of-limit analog/temperature measurement is cleared by one of the methods described later, the latch is reset. It will not be set again, and $\overline{INT}$ will not be reasserted until after two Local Temperature Measurements have been taken, even if the status bit remains set or a new analog/temperature event occurs, as shown in Figure 20. This delay corresponds to almost 2 monitoring cycles, and is about 530 ms. However, interrupts from other sources such as a fan or GPIO can still occur. This is illustrated in Figure 21.

   Status Register 4 also stores inputs from two other interrupt sources, which operate in a different way from the other status bits. If automatic fan speed control (AFC) is enabled, Bit 4 of Status Register 4 will be set whenever a fan starts or stops. This bit causes a one-off $\overline{INT}$ output as shown in Figure 22.

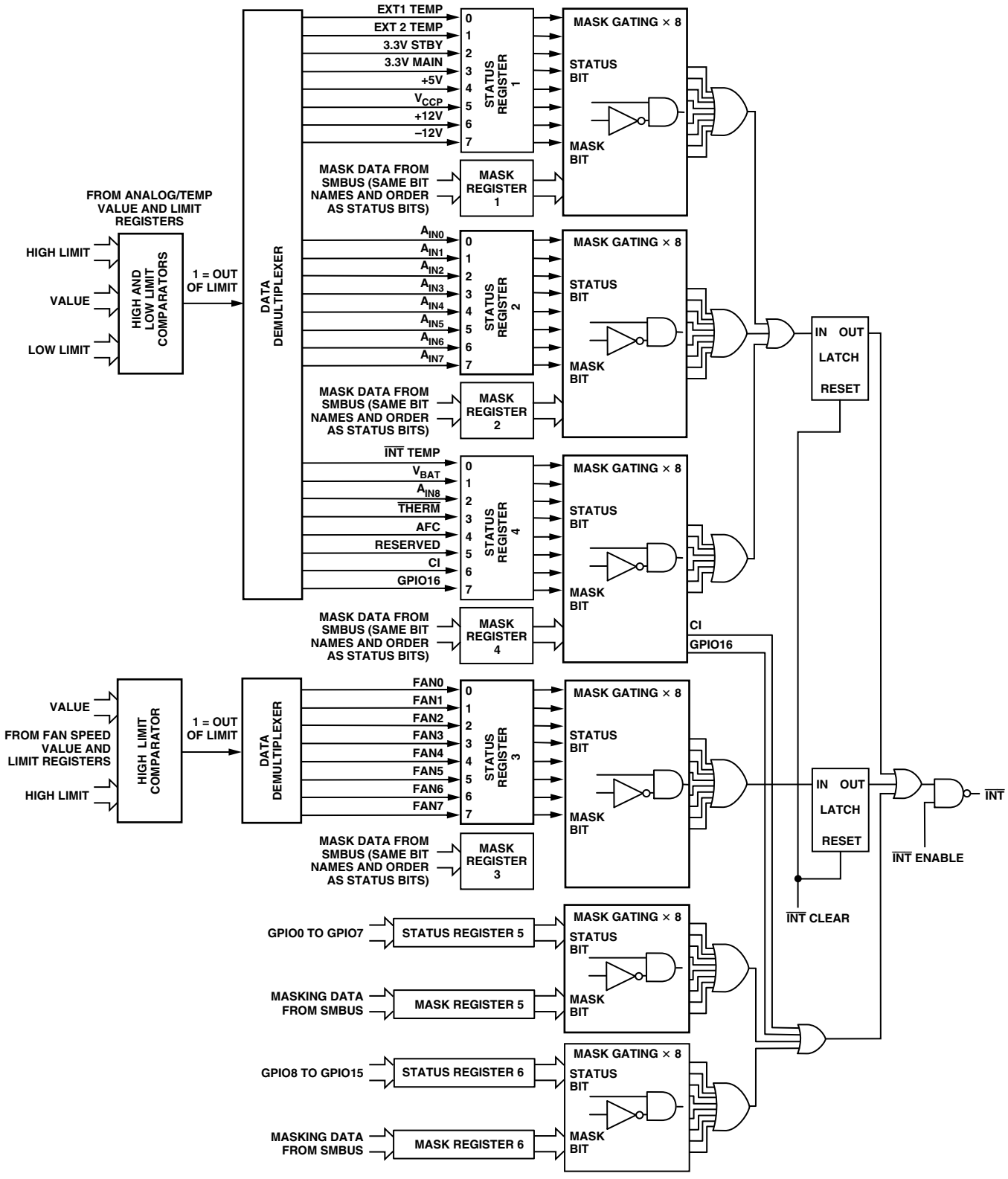


Figure 19. Interrupt Structure

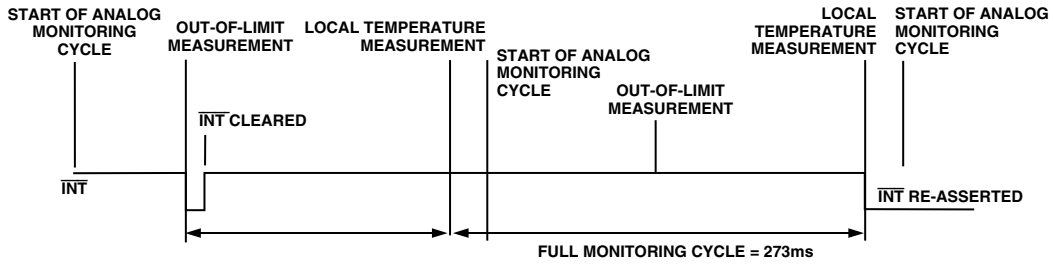


Figure 20. Delay After Clearing $\overline{INT}$ Before Re-Assertion

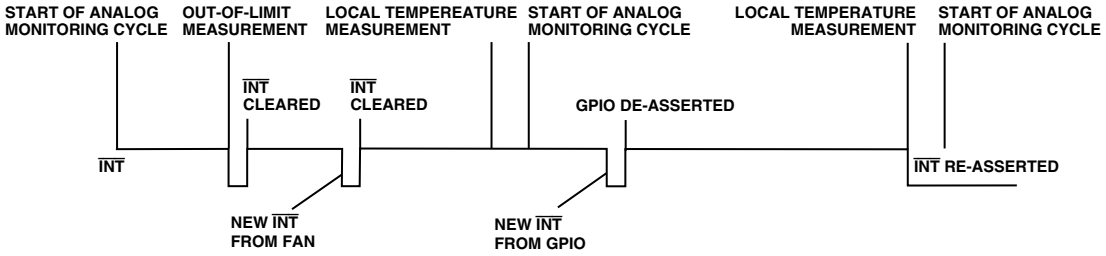


Figure 21. Other Interrupt Sources Can Re-Assert $\overline{INT}$ Immediately

It is cleared during the next monitoring cycle and if $\overline{INT}$ has been cleared, it will not cause $\overline{INT}$ to be reasserted.

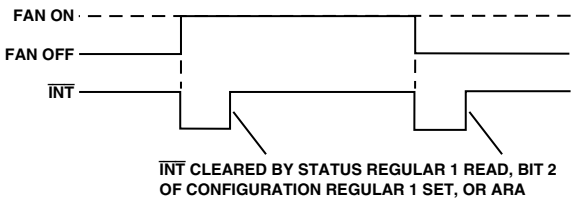


Figure 22. Assertion of INT Due to AFC Event

In a similar way, a change of state at the THERM output (described in more detail later), sets bit 3 of Status Register 4 and causes a one-off INT output. A change of state at the THERM output also causes Bit 0 of Status Register 1, Bit 1 of Status Register 1, or Bit 0 of Status Register 4 to be set, depending on which temperature channel caused the THERM event. This bit will be reset during the next monitoring cycle, provided the temperature channel is within the normal high and low limits.

2. Fan Inputs. Fan inputs generate interrupts in a similar way to analog/temp inputs, but as the analog/temperature inputs and fan inputs have different monitoring cycles, they have separate interrupt circuits. As the speed of each fan is measured, the output of the fan speed counter is stored in a value register. The result is compared to the fan speed limit and used to set or clear a bit in Status Register 3. In this case, the fan is only monitored for under-speed (fan counter > fan speed limit). Mask Register 3 is used to mask fan interrupts. After mask gating, the fan status bits are OR'd together and used to set a latch, whose output is OR'd with other interrupt sources to produce the $\overline{INT}$ output.

   Like the analog/temp interrupt, an $\overline{INT}$ output caused by an out-of-limit fan speed measurement, once cleared, will not be reasserted until the end of the next monitoring cycle, although other interrupt sources may cause $\overline{INT}$ to be asserted.

3. GPIO and CI Pins. When GPIO pins are configured as inputs, asserting a GPIO input (high or low, depending on polarity) sets the corresponding GPIO status bit in Status Registers 5 and 6, or Bit 7 of Status Register 4 (GPIO16). A chassis intrusion event sets Bit 6 of Status Register 4.

   The GPIO and CI status bits, after mask gating, are OR'd together and OR'd with other interrupt sources to produce the $\overline{INT}$ output. GPIO and CI interrupts are not latched and cannot be cleared by normal interrupt clearing. They can only be cleared by masking the status bits or by removing the source of the interrupt.

ENABLING AND CLEARING INTERRUPTS

The INT output is enabled when Bit 1 of Configuration Register 1 INT_Enable) is high, and Bit 2 (INT_Clear) is low.

$\overline{INT}$ may be cleared if:

- Status Register 1 is read. Ideally, if polling the status registers trying to identify interrupt sources, Status Register 1 should be polled last, since a read of Status Register 1 clears all the other interrupt status registers.
- The ADM1026 receives the Alert Response Address (0001 100) over the SMBus.
- Bit 2 of Configuration Register 1 is set.

Bidirectional $\overline{THERM}$ Pin

The ADM1026 has a second interrupt pin (GPIO16/$\overline{THERM}$, Pin 42) that responds only to critical thermal events. The $\overline{THERM}$ pin goes low whenever a $\overline{THERM}$ limit is exceeded. This function is useful for CPU throttling or system shutdown. In addition, whenever $\overline{THERM}$ is activated, the PWM and DAC outputs go full scale to provide failsafe system cooling. This output is enabled by setting Bit 4 of Configuration Register 1 (Regular 00h). Whenever a $\overline{THERM}$ limit gets exceeded, Bit 3 of Status Register 4 (Reg 23h) gets set, even if the $\overline{THERM}$ function is disabled (Bit 4 of Configuration Register 1 = 0). In this case, the $\overline{THERM}$ status bit gets set, but the PWM and DAC outputs are not forced to full scale.

Three thermal limit registers are provided for the three temperature sensors at addresses 0Dh to 0Fh. These registers are dedicated to the $\overline{\text{THERM}}$ function and none of the other limit registers have any effect on the $\overline{\text{THERM}}$ output.

If any of the temperature measurements exceed the corresponding limit, $\overline{\text{THERM}}$ will be asserted (low) and the DAC and PWM outputs will go to maximum to drive any cooling fans to full speed.

To avoid cooling fans cycling on and off continually when the temperature is close to the limit, a fixed hysteresis of 5°C is provided. $\overline{\text{THERM}}$ will only be de-asserted when the measured temperature of all three sensors is 5°C below the limit.

Whenever the $\overline{\text{THERM}}$ output changes, $\overline{\text{INT}}$ will be asserted, as shown in Figure 23. However, this is edge-triggered, so if $\overline{\text{INT}}$ is subsequently cleared by one of the methods previously described, it will not be reasserted, even if THERM remains asserted. $\overline{\text{THERM}}$ will only cause $\overline{\text{INT}}$ to be asserted again when it changes state.

Note that the $\overline{\text{THERM}}$ pin is bidirectional, so $\overline{\text{THERM}}$ may be pulled low externally as an input. This will cause the PWM and DAC outputs to go to full scale until $\overline{\text{THERM}}$ is returned high again. To disable $\overline{\text{THERM}}$ as an input, set Bit 0 of Configuration Register 3 (Reg 07h). This will configure Pin 42 as GPIO16 and prevent a low on Pin 42 from driving the fans at full speed.

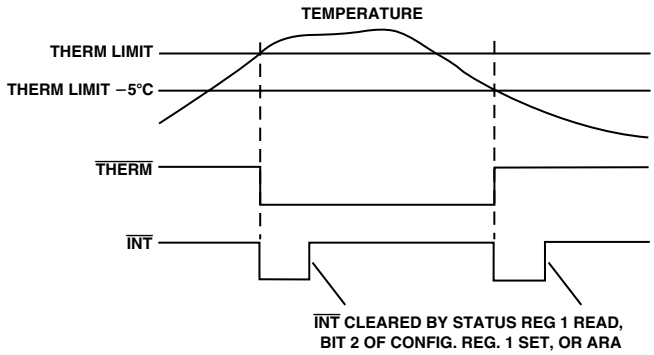


Figure 23. Assertion of $\overline{\text{INT}}$ Due to $\overline{\text{THERM}}$ Event

Reset Input and Outputs

The ADM1026 has two active low, power-on reset outputs, $\overline{\text{RESETMAIN}}$ and $\overline{\text{RESETSTBY}}$. These operate as follows:

RESETSTBY monitors 3.3 V STBY. At power-up, RESETSTB will be asserted (pulled low) until 180 ms after 3.3 V STBY rises above the reset threshold.

$\overline{\text{RESETMAIN}}$ monitors 3.3 V MAIN. At power-up, $\overline{\text{RESETMAIN}}$ will be asserted (pulled low) until 180 ms after 3.3 V MAIN rises above the reset threshold.

If 3.3 V MAIN rises with or before DV_{CC}, RESETMAIN will remain asserted until 180 ms after RESETMAIN is negated. RESETMAIN can also function as a RESET input. Pulling this pin low will reset the system to power-on defaults.

Note that the 3.3 V STBY pin supplies power to the ADM1026. In applications that do not require monitoring of a 3.3 V STBY and 3.3 V MAIN supply, these two pins should be connected together (3.3 V MAIN should not be left floating).

To ensure that the 3.3 V STBY pin does not get backdriven, the 3.3 V STBY supply should power up before all other voltages in the system.

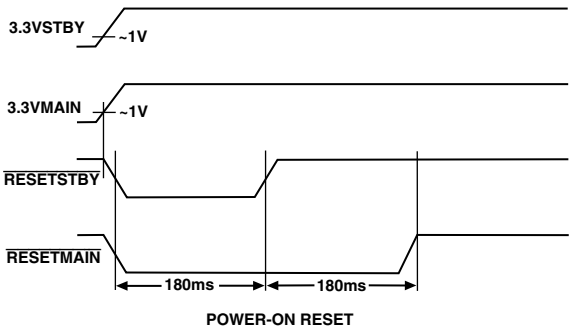


Figure 24. Operation of Offset Outputs

NAND TREE TESTS

A NAND tree is provided in the ADM1026 for Automated Test Equipment (ATE) board level connectivity testing. This allows the functionality of all digital inputs to be tested in a simple manner and any pins that are nonfunctional or shorted together to be identified. The structure of the NAND tree is shown in Figure 25. The device is placed into NAND Tree Test Mode by powering up with Pin 25 held high. This pin is sampled automatically after power-up, and if it is connected high, then the NAND test mode is invoked.

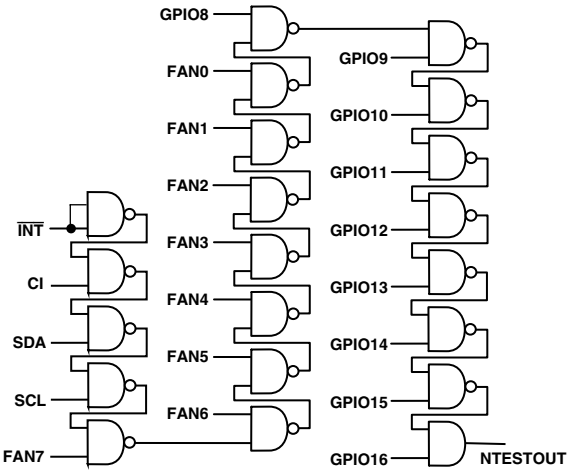


Figure 25. NAND Tree

NOTE

For NAND Tree Test to work, all outputs (INT, RSTMAIN, RSTSTBY, and PWM) must remain high during the test.

The NAND tree test may be carried out in one of two ways.

1. Start with all inputs low and take them high in turn, starting with the input nearest to NTEST_OUT (GPIO16/$\overline{\text{THERM}}$) and working back up the tree to the input furthest from NTESTOUT ($\overline{\text{INT}}$). This should give the characteristic output pattern shown in Figure 26, with NTESTOUT toggling each time an input is taken high.

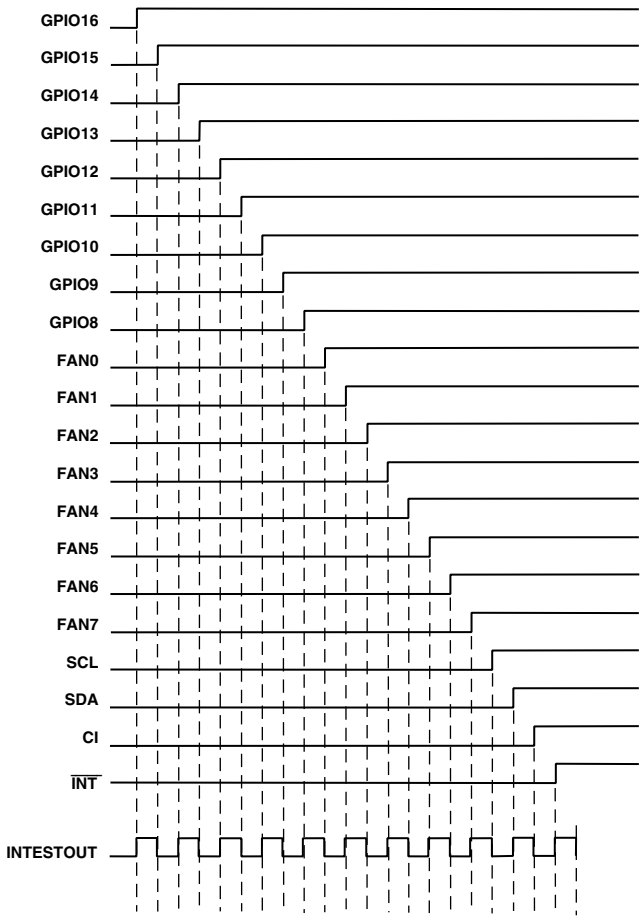


Figure 26. NAND Tree Test Taking Inputs High In Turn

2. Start with all inputs high and take them low in turn, starting with the input furthest from NTEST_OUT ($\overline{\text{INT}}$) and working down the tree to the input nearest to NTEST_OUT (GPIO16/$\overline{\text{THERM}}$). This should give a similar output pattern to Figure 27.

NOTES

1. When generating test waveforms, a typical propagation delay of 500 ns through the NAND tree should be allowed for.
2. If any of the inputs shown in Figure 25 are unused, they should not be connected direct to ground, but via a resistor such as 10 kΩ. This will allow the ATE (Automatic Test Equipment) to drive every input high so that the NAND tree test can be properly carried out.

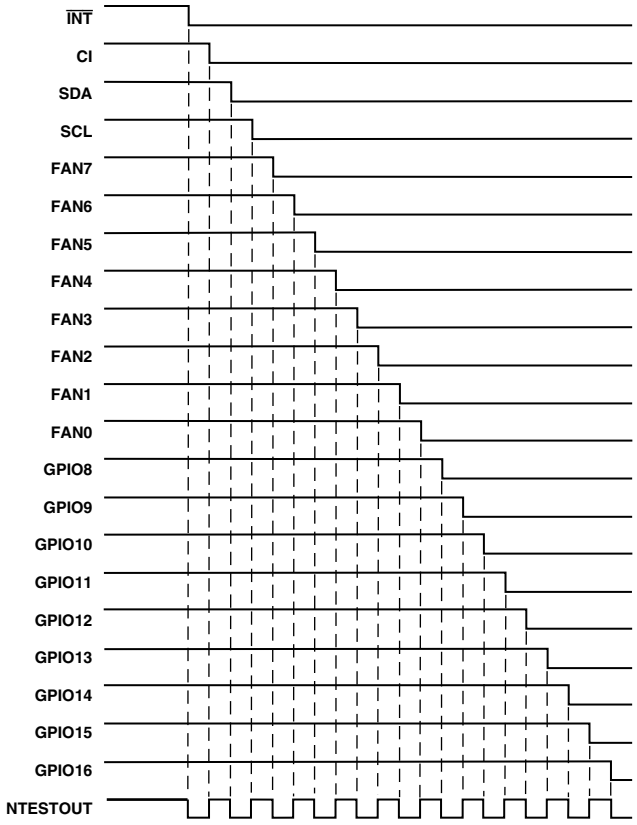


Figure 27. NAND Tree Test taking Inputs Low In Turn

In the event of an input being nonfunctional (stuck high or low) or two inputs shorted together, the output pattern will be different.

Some examples are given in Figures 28 to 30.

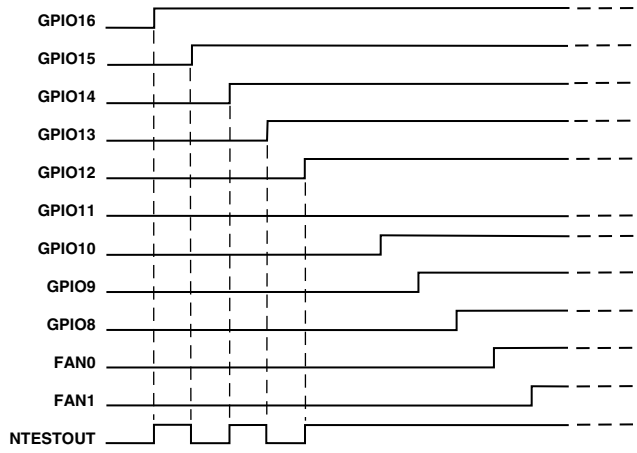


Figure 28. NAND Tree Test With GPIO11 Stuck Low

Figure 28 shows the effect of one input being stuck low.

The output pattern is normal until the stuck input is reached. Because that input is permanently low, neither it nor any inputs further up the tree can have any effect on the output.

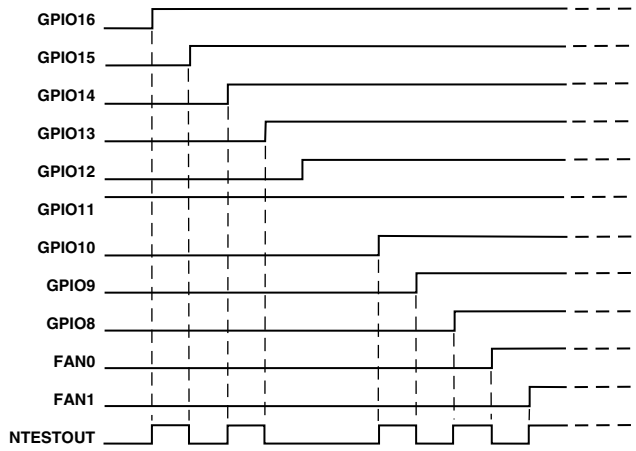


Figure 29. NAND Tree Test With One Input Stuck High

Figure 29 shows the effect of one input being stuck high. Taking GPIO12 high should take the output high. However, the next input up the tree, GPIO11, is already high, so the output immediately goes low again, causing a missing pulse in the output pattern.

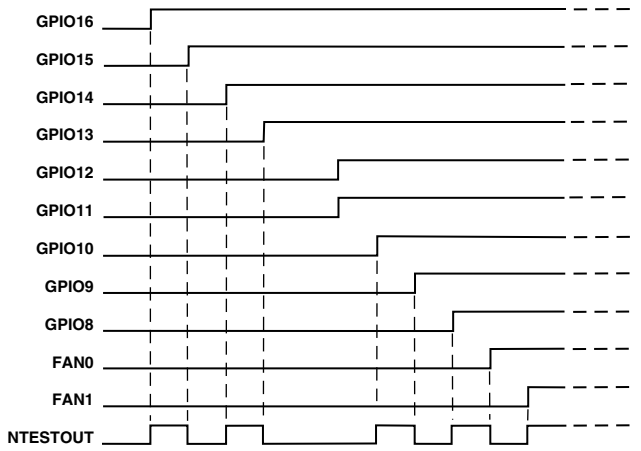


Figure 30. NAND Tree Test With Two Inputs Shorted

A similar effect occurs if two adjacent inputs are shorted together. The example in Figure 30 assumes that the current sink capability of the circuit driving the inputs is considerably higher than the source capability, so the inputs will be low if either is low, but high only if both are high.

When GPIO12 goes high the output should go high. But since GPIO12 and GPIO11 are shorted, they both go high together, causing a missing pulse in the output pattern.

USING THE ADM1026

When power is first applied, the ADM1026 performs a power-on reset on all its registers (not EEPROM), which sets them to default conditions as shown in Table VI. In particular, it should be noted that all GPIO pins are configured as inputs to avoid possible conflicts with circuits trying to drive these pins.

The ADM1026 can also be initialized at any time by writing a 1 to Bit 7 of Configuration Register 1, which sets some registers to their default power-on conditions. This bit should be cleared by writing a 0 to it.

After power-up, the ADM1026 must be configured to the user's specific requirements. This consists of:

- Writing values to the limit registers.
- Configuring Pins 3 to 6, and 9 to 12 as fan inputs or GPIO, using Configuration Register 2 (Address 01h)
- Setting the fan divisors using the fan divisor registers (Addresses 02h and 03h).
- Configuring the GPIO pins for input/output, polarity, using GPIO Configuration Registers 1 to 4 (Addresses 08h to 0Bh) and Bits 6 and 7 of Configuration Register 3.
- Setting mask bits in Mask Registers 1 to 6 (Addresses 18h to 1Dh) for any inputs that are to be masked out.
- Setting up Configuration Registers 1 and 3, as follows:

Configuration Register 1

Bit 0 controls the monitoring loop of the ADM1026. Setting Bit 0 low stops the monitoring loop and puts the ADM1026 into a low power mode thereby reducing power consumption. Serial bus communication is still possible with any register in the ADM1026 while in low power mode. Setting bit 0 high starts the monitoring loop.

Bit 1 enables or disables the $\overline{INT}$ Interrupt output. Setting Bit 1 high enables the $\overline{INT}$ output, setting Bit 1 low disables the output.

Bit 2 is used to clear the $\overline{INT}$ interrupt output when set high. GPIO pins and interrupt status register contents will not be affected.

Bit 3 configures Pins 27 and 28 as the second external temperature channel when 0, and as A_{IN8} and A_{IN9} when set to 1.

Bit 4 enables the $\overline{THERM}$ output when set to 1.

Bit 5 enables automatic fan speed control on the DAC output when set to 1.

Bit 6 enables automatic fan speed control on the PWM output when set to 1.

Bit 7 performs a soft reset when set to 1.

Configuration Register 3

Bit 0 configures Pin 42 as GPIO when set to 1 or as $\overline{THERM}$ when cleared to 0.

Bit 1 clears the CI latch when set to 1. A 0 must be written thereafter to allow subsequent CI detection.

Bit 2 selects V_{REF} as 2.5 V when set to 1 or as 1.82 V when cleared to 0.

Bits 3 to 5 are unused.

Bits 6 and 7 set up GPIO16 for direction and polarity.

Starting Conversion

The monitoring function (analog inputs, temperature, and fan speeds) in the ADM1026 is started by writing to Configuration Register 1 and setting Start (Bit 0) high. The $\overline{\text{INT}}$_Enable (Bit 1) should be set to 1, and $\overline{\text{INT}}$ Clear (Bit 2) set to 0 to enable interrupts. The $\overline{\text{THERM}}$ enable bit (Bit 4) should be set to 1 to enable temperature interrupts at the $\overline{\text{THERM}}$ pin. Apart from initially starting together, the analog measurements and fan speed measurements proceed independently, and are not synchronized in any way.

Reduced Power Mode

The ADM1026 can be placed in a low power mode by setting Bit 0 of the configuration register to 0. This disables the internal ADC.

Software Reset Function

As previously mentioned, the ADM1026 can be reset in software by setting Bit 7 of Configuration Register 1 (Reg. 00h) = 1. This bit should then be cleared to 0. Note that the software reset differs from a power-on reset in that only some of the ADM1026 registers get reinitialized to their power-on default values. The registers that are initialized to their default values by the Software Reset are:

- Configuration Registers (Registers 00h to 0Bh)
- Mask Registers 1 to 6, internal temp offset, and Status Registers 4, 5, and 6 (Registers 18h to 25h)
- All value registers (Registers 1Fh, 20h to 3Fh)
- External 1 and External 2 Offset Registers (6Eh, 6Fh)

Note that the Limit Registers (0Dh to 12h, 40h to 6Dh) are not reset by the Software Reset function. This can be useful if you need to reset the part but do not want to have to reprogram all parameters again. Note that a power-on reset initializes all registers on the ADM1026, including the limit registers.

Application Schematic

Figure 31 shows how the ADM1026 could be used in an application that requires system management of a PC or server. Several GPIOs are used to read the VID codes of the CPU. Up to two CPU temperature measurements can be read back. All power supply voltages are monitored in the system. Up to eight fan speeds can be measured, irrespective of whether they are controlled by the ADM1026 or hard-wired to a system supply. The V_{REF} output includes the recommended filtering circuitry.

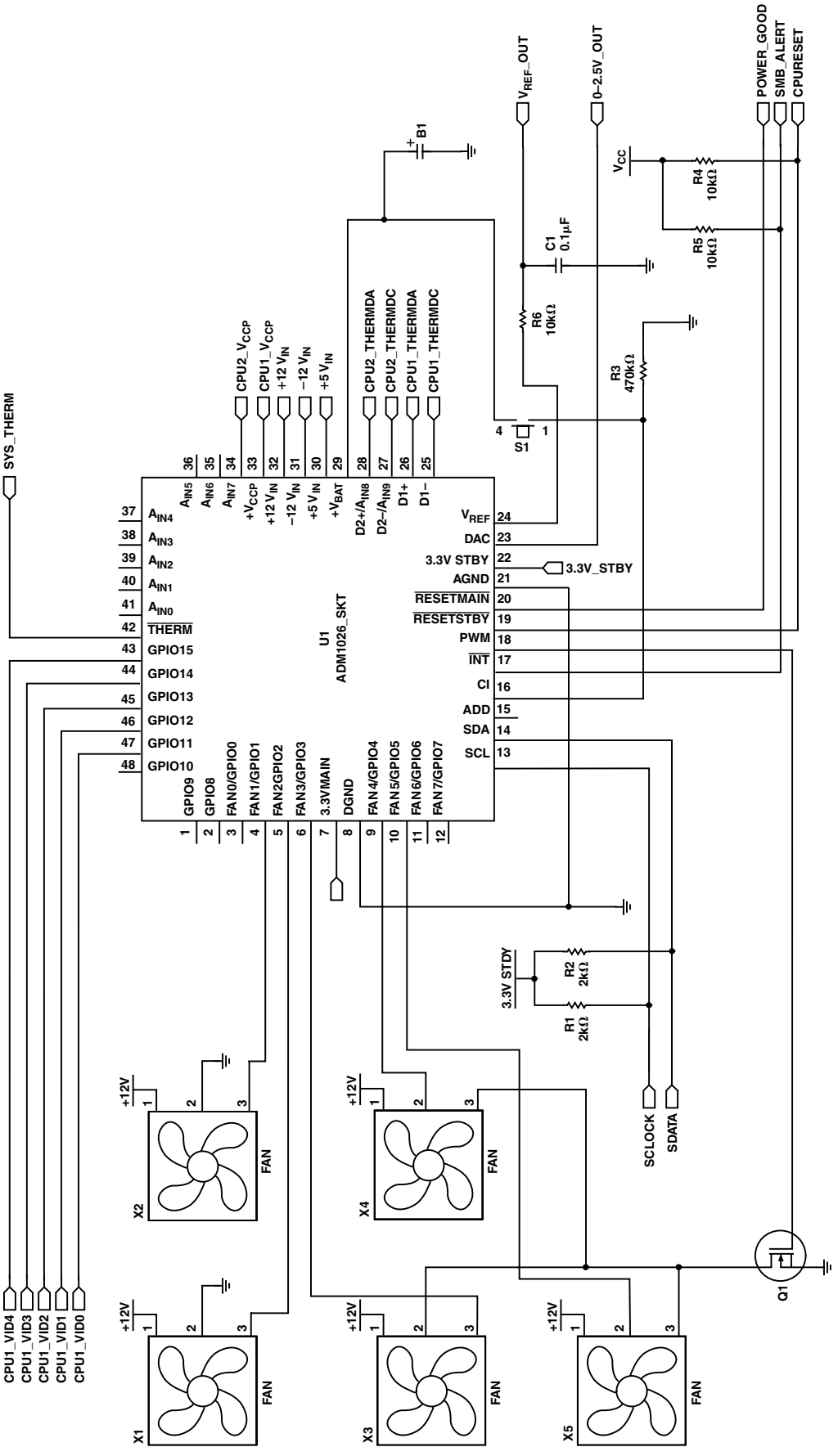


Figure 31. ADM1026 Schematic

REGISTERS

Table V. Address Pointer Register

Bit	Name	R/$\overline{W}$	Description
7–0	Address Pointer	Write	Address of ADM1026 registers. See the tables below for detail

Table VI. List of Registers

Hex Address	Name	Power ON Value (Hex or Binary Bit 7–0)	Description
00	Configuration 1	00h	Configures various operating parameters
01	Configuration 2	00h	Configures Pins 3–6 and 9–12 as fan inputs or GPIO
02	Fan 0–3 Divisor	55h	Sets oscillator frequency for Fan 0–3 speed measurement
03	Fan 4–7 Divisor	55h	Sets oscillator frequency for Fan 4–7 speed measurement
04	DAC Control	FFh	Contains value for fan speed DAC (analog fan speed control) or minimum value for automatic fan speed control
05	PWM Control	FFh	Contains value for PWM fan speed control or minimum value for automatic fan speed control
06	EEPROM Register	100h	For factory use only
07	Configuration Register	300h	Configuration register for $\overline{THERM}$, V_{REF} and GPIO16
08	GPIO Config 1	00h	Configures GPIO0 to GPIO3 as input or output and as active high or active low
09	GPIO Config 2	00h	Configures GPIO4 to GPIO7 as input or output and as active high or active low
0A	GPIO Config 3	00h	Configures GPIO8 to GPIO11 as input or output and as active high or active low
0B	GPIO Config 4	00h	Configures GPIO12 to GPIO15 as input or output and as active high or active low
0C	EEPROM Register 2	00h	For factory use only
0D	Int Temp $\overline{THERM}$ Limit	37h (55°C)	High limit for $\overline{THERM}$ interrupt output based on internal temperature measurement
0E	TDM1 $\overline{THERM}$ Limit	50h (80°C)	High limit for $\overline{THERM}$ interrupt output based on Remote Channel 1(D1) temperature measurement
0F	TDM2 $\overline{THERM}$ Limit	50h (80°C)	High limit for $\overline{THERM}$ interrupt output based on Remote Channel 2 (D2) temperature measurement
10	Int Temp T_{MIN}	28h (40°C)	T_{MIN} value for automatic fan speed control based on internal temperature measurement
11	TDM1 T_{MIN}	40h (64°C)	T_{MIN} value for automatic fan speed control based on Remote Channel 1 (D1) temperature measurement
12	TDM2 T_{MIN}	40h (64°C)	T_{MIN} value for automatic fan speed control based on Remote Channel 2 (D2) temperature measurement
13	EEPROM Register 3	00h	Configures EEPROM for read/write/erase, etc.
14	Test Register 1	00h	Manufacturer's test register
15	Test Register 2	00h	For manufacturer's use only
16	Manufacturer's ID	41h	Contains manufacturer's ID code
17	Revision	4xh	Contains code for major and minor revisions
18	Mask Register 1	00h	Interrupt Mask register for temperature and supply voltage faults
19	Mask Register 2	00h	Interrupt mask register for analog input faults
1A	Mask Register 3	00h	Interrupt mask register for fan faults
1B	Mask Register 4	00h	Interrupt mask register for local temp, V_{BAT}, $A_{IN8,}$ $\overline{THERM}$, AFC, CI and GPIO16
1C	Mask Register 5	00h	Interrupt mask register for GPIO0 to GPIO7
1D	Mask Register 6	00h	Interrupt mask register for GPIO8 to GPIO15
1E	Int Temp Offset	00h	Offset register for internal temperature measurement
1F	Int Temp Value	00h	Measured temperature from on–chip sensor
20	Status Register 1	00h	Interrupt status register for external temp and supply voltage faults
21	Status Register 2	00h	Interrupt status register for analog input faults
22	Status Register 3	00h	Interrupt status register for fan faults
23	Status Register 4	00h	Interrupt status register for local temp, V_{BAT}, A_{IN8}, $\overline{THERM}$, AFC, CI and GPIO16
24	Status Register 5	00h	Interrupt status register for GPIO0 to GPIO7
25	Status Register 6	00h	Interrupt status register for GPIO8 to GPIO15
26	V_{BAT} Value	00h	Measured value of V_{BAT}
27	A_{IN8} Value	00h	Measured value of A_{IN8}
28	TDM1 Value	00h	Measured value of remote temperature channel 1 (D1)

Table VI. List of Registers (Continued)

Hex Address	Name	Power ON Value (Hex or Binary Bit 7–0)	Description
29	TDM2/A_{IN9} Value	00h	Measured value of remote temperature channel 2 (D2) or A_{IN9}
2A	3.3 V STBY Value	00h	Measured value of 3.3 V STBY
2B	3.3 V MAIN Value	00h	Measured value of 3.3 V MAIN
2C	+5 V Value	00h	Measured value of +5 V supply
2D	V_{CCP} Value	00h	Measured value of processor core voltage
2E	+12 V Value	00h	Measured value of +12 V supply
2F	–12 V Value	00h	Measured value of –12 V supply
30	A_{IN0} Value	00h	Measured value of A_{IN0}
31	A_{IN1} Value	00h	Measured value of A_{IN1}
32	A_{IN2} Value	00h	Measured value of A_{IN2}
33	A_{IN3} Value	00h	Measured value of A_{IN3}
34	A_{IN4} Value	00h	Measured value of A_{IN4}
35	A_{IN5} Value	00h	Measured value of A_{IN5}
36	A_{IN6} Value	00h	Measured value of A_{IN6}
37	A_{IN7} Value	00h	Measured value of A_{IN7}
38	FAN0 Value	00h	Measured speed of Fan 0
39	FAN1 Value	00h	Measured speed of Fan 1
3A	FAN2 Value	00h	Measured speed of Fan 2
3B	FAN3 Value	00h	Measured speed of Fan 3
3C	FAN4 Value	00h	Measured speed of Fan 4
3D	FAN5 Value	00h	Measured speed of Fan 5
3E	FAN6 Value	00h	Measured speed of Fan 6
3F	FAN7 Value	00h	Measured speed of Fan 7
40	TDM1 High Limit	64h (100°C)	High limit for Remote Temperature Channel 1 (D1) measurement
41	TDM2/A_{IN9} High Limit	64h (100°C)	High limit for Remote Temperature Channel 2 (D2) or A_{IN9} measurement
42	3.3 V STBY High Limit	FFh	High limit for 3.3 V STBY measurement
43	3.3 V MAIN High Limit	FFh	High limit for 3.3 V MAIN measurement
44	+5 V High Limit	FFh	High limit for +5 V supply measurement
45	V_{CCP} High Limit	FFh	High limit for processor core voltage measurement
46	+12 V High Limit	FFh	High limit for +12 V supply measurement
47	–12 V High Limit	FFh	High limit for –12 V supply measurement
48	TDM1 Low Limit	80h	Low limit for Remote Temperature Channel 1 (D1) measurement
49	TDM2/A_{IN9} Low Limit	80h	Low limit for Remote Temperature Channel 2 (D2) or A_{IN9} measurement
4A	3.3 V STBY Low Limit	00h	Low limit for 3.3 V STBY measurement
4B	3.3 V MAIN Low Limit	00h	Low limit for 3.3 V MAIN measurement
4C	+5 V Low Limit	00h	Low limit for +5 V supply
4D	V_{CCP} Low Limit	00h	Low limit for processor core voltage measurement
4E	+12 V Low Limit	00h	Low limit for +12 V supply measurement
4F	–12 V Low Limit	00h	Low limit for –12 V supply measurement
50	A_{IN0} High Limit	FFh	High limit for A_{IN0} measurement
51	A_{IN1} High Limit	FFh	High limit for A_{IN1} measurement
52	A_{IN2} High Limit	FFh	High limit for A_{IN2} measurement
53	A_{IN3} High Limit	FFh	High limit for A_{IN3} measurement
54	A_{IN4} High Limit	FFh	High limit for A_{IN4} measurement
55	A_{IN5} High Limit	FFh	High limit for A_{IN5} measurement
56	A_{IN6} High Limit	FFh	High limit for A_{IN6} measurement
57	A_{IN7} High Limit	FFh	High limit for A_{IN7} measurement
58	A_{IN0} Low Limit	00h	Low limit for A_{IN0} measurement
59	A_{IN1} Low Limit	00h	Low limit for A_{IN1} measurement
5A	A_{IN2} Low Limit	00h	Low limit for A_{IN2} measurement
5B	A_{IN3} Low Limit	00h	Low limit for A_{IN3} measurement
5C	A_{IN4} Low Limit	00h	Low limit for A_{IN4} measurement
5D	A_{IN5} Low Limit	00h	Low limit for A_{IN5} measurement
5E	A_{IN6} Low Limit	00h	Low limit for A_{IN6} measurement
5F	A_{IN7} Low Limit	00h	Low limit for A_{IN7} measurement

Table VI. List of Registers (Continued)

Hex Address	Name	Power-On Value (Hex or Binary Bit 7– 0)	Description
60	FAN0 High Limit	FFh	High limit for Fan 0 speed measurement (no low limit)
61	FAN1 High Limit	FFh	High limit for Fan 1 speed measurement (no low limit)
62	FAN2 High Limit	FFh	High limit for Fan 2 speed measurement (no low limit)
63	FAN3 High Limit	FFh	High limit for Fan 3 speed measurement (no low limit)
64	FAN4 High Limit	FFh	High limit for Fan 4 speed measurement (no low limit)
65	FAN5 High Limit	FFh	High limit for Fan 5 speed measurement (no low limit)
66	FAN6 High Limit	FFh	High limit for Fan 6 speed measurement (no low limit)
67	FAN7 High Limit	FFh	High limit for Fan 7 speed measurement (no low limit)
68	Int. Temp. High Limit	50h (80°C)	High limit for local temperature measurement
69	Int. Temp. Low Limit	80h	Low limit for local temperature measurement
6A	V_{BAT} High Limit	FFh	High limit for V_{BAT} measurement
6B	V_{BAT} Low Limit	00h	Low limit for V_{BAT} measurement
6C	A_{IN8} High Limit	FFh	High limit for A_{IN8} measurement
6D	A_{IN8} Low Limit	00h	Low limit for A_{IN8} measurement
6E	Ext1 Temp Offset	00h	Offset register for Remote Temperature Channel 1
6F	Ext2 Temp Offset	00h	Offset register for Remote Temperature Channel 2

DETAILED REGISTER DESCRIPTIONS

Table VII. Register 00h, Configuration Register 1 (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
0	Monitor = 0	R/$\overline{W}$	When this bit is set the ADM1026 monitors all voltage, temperature and fan channels in a round robin manner.
1	Int Enable = 0	R/$\overline{W}$	When this bit is set, the $\overline{INT}$ output pin is enabled.
2	Int Clear = 0	R/$\overline{W}$	Setting this bit will clear an interrupt from the voltage, temperature or fan speed channels. Because GPIO interrupts are level triggered, this bit will have no effect on interrupts originating from GPIO channels. This bit is cleared by writing a 0 to it. If in monitoring mode voltages, temperatures and fan speeds will continue to be monitored after writing to this bit to clear an interrupt, so an interrupt may be set again on the next monitoring cycle.
3	Enable Voltage/Ext2 = 0	R/$\overline{W}$	When this bit is 1, the ADM1026 monitors voltage (A_{IN8} and A_{IN9}) on Pins 28 and 27 respectively. When this bit is 0, the ADM1026 monitors a second thermal diode temperature channel, D2, on these pins. If the second thermal diode channel is not being used, it is recommended that the bit be set to 1.
4	Enable $\overline{THERM}$ = 0	R/$\overline{W}$	When this bit is 1, the $\overline{THERM}$ pin (Pin 42) will be asserted (go low) if any of the $\overline{THERM}$ limits are exceeded. If $\overline{THERM}$ is pulled low as an input, the DAC and PWM outputs are forced to full scale until $\overline{THERM}$ is taken high.
5	Enable DAC AFC = 0	R/$\overline{W}$	When this bit is 1, the DAC output is enabled for automatic fan speed control (AFC) based on temperature. When this bit is 0, the DAC Output reflects the value in Reg 04h, DAC Control Register.
6	Enable PWM AFC = 0	R/$\overline{W}$	When this bit is 1, the PWM output is enabled for automatic fan speed control (AFC) based on temperature. When this bit is 0, the PWM Output reflects the value in Reg 05h, PWM Control Register.
7	Software Reset = 0	R/$\overline{W}$	Writing a 1 to this bit restores all registers to the power on defaults. This bit is cleared by writing a 0 to it. For more info, see S/W Reset section.

Table VIII. Register 01h, Configuration Register 2 (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
0	Enable GPIO0/Fan0 = 0	R/$\overline{W}$	When this bit is 1, pin 3 is enabled as a General Purpose I/O pin (GPIO0), otherwise it is a Fan Tach measurement input (Fan 0).
1	Enable GPIO1/Fan1 = 0	R/$\overline{W}$	When this bit is 1, pin 4 is enabled as a General Purpose I/O pin (GPIO1), otherwise it is a Fan Tach measurement input (Fan 1).
2	Enable GPIO2/Fan2 = 0	R/$\overline{W}$	When this bit is 1, pin 5 is enabled as a General Purpose I/O pin (GPIO2), otherwise it is a Fan Tach measurement input (Fan 2).
3	Enable GPIO3/Fan3 = 0	R/$\overline{W}$	When this bit is 1, pin 6 is enabled as a General Purpose I/O pin (GPIO3), otherwise it is a Fan Tach measurement input (Fan 3).
4	Enable GPIO4/Fan4 = 0	R/$\overline{W}$	When this bit is 1, pin 9 is enabled as a General Purpose I/O pin (GPIO4), otherwise it is a Fan Tach measurement input (Fan 4).
5	Enable GPIO5/Fan5 = 0	R/$\overline{W}$	When this bit is 1, pin 10 is enabled as a General Purpose I/O pin (GPIO5), otherwise it is a Fan Tach measurement input (Fan 5).
6	Enable GPIO6/Fan6 = 0	R/$\overline{W}$	When this bit is 1, pin 11 is enabled as a General Purpose I/O pin (GPIO6), otherwise it is a Fan Tach measurement input (Fan 6).
7	Enable GPIO7/Fan7 = 0	R/$\overline{W}$	When this bit is 1, pin 12 is enabled as a General Purpose I/O pin (GPIO7), otherwise it is a Fan Tach measurement input (Fan 7).

Table IX. Register 02h, Fans 0 to 3 FAN DIVISOR Register (Power-On Default 55h)

Bit	Name	R/$\overline{W}$	Description
1–0	Fan 0 Divisor	R/$\overline{W}$	Sets the oscillator prescaler division ratio for Fan 0 speed measurement. The division ratios, oscillator frequencies and typical fan speeds (based on 2 tach pulses per rev.) are as follows:
			Code / **Divide-by** / **Oscillator Frequency (kHz)** / **Fan Speed (RPM)**
			00 / 1 / 22.5 / 8800, nominal, for count of 153
			01 / 2 / 11.25 / 4400, nominal, for count of 153
			10 / 4 / 5.62 / 2200, nominal, for count of 153
			11 / 8 / 2.81 / 1100, nominal, for count of 153
3–2	Fan 1 Divisor	R/$\overline{W}$	Same as for Fan 0
5–4	Fan 2 Divisor	R/$\overline{W}$	Same as for Fan 0
7–6	Fan 3 Divisor	R/$\overline{W}$	Same as for Fan 0

Table X. Register 03h, Fans 4 to 7 FAN DIVISOR Register (Power-On Default 55h)

Bit	Name	R/$\overline{W}$	Description
1–0	Fan 4 Divisor	R/$\overline{W}$	Sets the oscillator prescaler division ratio for Fan 4 speed measurement. The division ratios, oscillator frequencies and typical fan speeds (based on 2 tach pulses per rev.) are as follows:
			Code / **Divide–by** / **Oscillator Frequency (kHz)** / **Fan Speed (RPM)**
			00 / 1 / 22.5 / 8800, nominal, for count of 153
			01 / 2 / 11.25 / 4400, nominal, for count of 153
			10 / 4 / 5.62 / 2200, nominal, for count of 153
			11 / 8 / 2.81 / 1100, nominal, for count of 153
3–2	Fan 5 Divisor	R/$\overline{W}$	Same as for Fan 4
5–4	Fan 6 Divisor	R/$\overline{W}$	Same as for Fan 4
7–6	Fan 7 Divisor	R/$\overline{W}$	Same as for Fan 4

Table XI. Register 04h, DAC Control Register (Power-On Default FFh)

Bit	Name	R/$\overline{W}$	Description
7–0	DAC Control	R/$\overline{W}$	This register contains the value to which the fan speed DAC is programmed in normal mode, or the 4 MSBs contain the Min Fan Speed in Auto Fan Speed control mode.

Table XII. Register 05h, PWM Control Register (Power-On Default FFh)

Bit	Name	R/$\overline{W}$	Description
7–4	PWM Control	R/$\overline{W}$	This register contains the value to which the PWM fan speed is programmed in normal mode, or the 4 MSBs contain the Min Fan Speed in Auto Fan Speed control mode. 0000 = 0% Duty Cycle 0001 = 7% Duty Cycle 0101 = 33% Duty Cycle 0110 = 40% Duty Cycle 0111 = 47% Duty Cycle 1110 = 93% Duty Cycle 1111 = 100% Duty Cycle
3–0	Unused	R	Undefined.

Table XIII. Register 06h, EEPROM Register 1 (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	Factory Use	R/$\overline{W}$	For factory use only. Do not write to this register.

Table XIV. Register 07h, Configuration Register 3 (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
0	Enable GPIO16/$\overline{THERM}$ = 0	R/$\overline{W}$	When this bit is 1, Pin 42 is enabled as a General Purpose I/O pin (GPIO16), otherwise it is the $\overline{THERM}$ output.
1	CI Clear = 0	R/$\overline{W}$	Writing a 1 to this bit will clear the CI latch. This bit is cleared by writing a 0 to it.
2	V_{REF} Select = 0	R/$\overline{W}$	When this bit is 0, V_{REF} (Pin 24) outputs 1.82 V, otherwise it outputs 2.5 V.
5–3	Unused	R	Undefined, will read back 0.
6	GPIO16 Direction	R/$\overline{W}$	When this bit is 0, GPIO16 is configured as an input; otherwise, it is an output.
7	GPIO16 Polarity	R/$\overline{W}$	When this bit is 0, GPIO16 is active low; otherwise, it is active high.

Table XV. Register 08h, GPIO Configuration Register 1 (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
0	GPIO0 Direction	R/$\overline{W}$	When this bit is 0, GPIO0 is configured as an input; otherwise, it is an output.
1	GPIO0 Polarity	R/$\overline{W}$	When this bit is 0, GPIO0 is active low; otherwise it is active high.
2	GPIO1 Direction	R/$\overline{W}$	When this bit is 0, GPIO1 is configured as an input; otherwise, it is an output.
3	GPIO1 Polarity	R/$\overline{W}$	When this bit is 0, GPIO1 is active low; otherwise it is active high.
4	GPIO2 Direction	R/$\overline{W}$	When this bit is 0, GPIO2 is configured as an input; otherwise, it is an output.
5	GPIO2 Polarity	R/$\overline{W}$	When this bit is 0, GPIO2 is active low; otherwise it is active high.
6	GPIO3 Direction	R/$\overline{W}$	When this bit is 0, GPIO3 is configured as an input; otherwise, it is an output.
7	GPIO3 Polarity	R/$\overline{W}$	When this bit is 0, GPIO3 is active low; otherwise it is active high.

Table XVI. Register 09h, GPIO Configuration Register 2 (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
0	GPIO4 Direction	R/$\overline{W}$	When this bit is 0, GPIO4 is configured as an input; otherwise, it is an output.
1	GPIO4 Polarity	R/$\overline{W}$	When this bit is 0, GPIO4 is active low; otherwise it is active high.
2	GPIO5 Direction	R/$\overline{W}$	When this bit is 0, GPIO5 is configured as an input; otherwise, it is an output.
3	GPIO5 Polarity	R/$\overline{W}$	When this bit is 0, GPIO5 is active low; otherwise it is active high.
4	GPIO6 Direction	R/$\overline{W}$	When this bit is 0, GPIO6 is configured as an input; otherwise, it is an output.
5	GPIO6 Polarity	R/$\overline{W}$	When this bit is 0, GPIO6 is active low; otherwise it is active high.
6	GPIO7 Direction	R/$\overline{W}$	When this bit is 0, GPIO7 is configured as an input; otherwise, it is an output.
7	GPIO7 Polarity	R/$\overline{W}$	When this bit is 0, GPIO7 is active low; otherwise it is active high.

Table XVII. Register 0Ah, GPIO Configuration Register 3 (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
0	GPIO8 Direction	R/$\overline{W}$	When this bit is 0, GPIO8 is configured as an input; otherwise, it is an output.
1	GPIO8 Polarity	R/$\overline{W}$	When this bit is 0, GPIO8 is active low; otherwise it is active high.
2	GPIO9 Direction	R/$\overline{W}$	When this bit is 0, GPIO9 is configured as an input; otherwise, it is an output.
3	GPIO9 Polarity	R/$\overline{W}$	When this bit is 0, GPIO9 is active low; otherwise it is active high.
4	GPIO10 Direction	R/$\overline{W}$	When this bit is 0, GPIO10 is configured as an input; otherwise, it is an output.
5	GPIO10 Polarity	R/$\overline{W}$	When this bit is 0, GPIO10 is active low; otherwise it is active high.
6	GPIO11 Direction	R/$\overline{W}$	When this bit is 0, GPIO11 is configured as an input; otherwise, it is an output.
7	GPIO11 Polarity	R/$\overline{W}$	When this bit is 0, GPIO11 is active low; otherwise it is active high.

Table XVIII. Register 0Bh, GPIO Configuration Register 4 (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
0	GPIO12 Direction	R/$\overline{W}$	When this bit is 0, GPIO12 is configured as an input; otherwise, it is an output.
1	GPIO12 Polarity	R/$\overline{W}$	When this bit is 0, GPIO12 is active low; otherwise it is active high.
2	GPIO13 Direction	R/$\overline{W}$	When this bit is 0, GPIO13 is configured as an input; otherwise, it is an output.
3	GPIO13 Polarity	R/$\overline{W}$	When this bit is 0, GPIO13 is active low; otherwise it is active high.
4	GPIO14 Direction	R/$\overline{W}$	When this bit is 0, GPIO14 is configured as an input; otherwise, it is an output.
5	GPIO14 Polarity	R/$\overline{W}$	When this bit is 0, GPIO14 is active low; otherwise it is active high.
6	GPIO15 Direction	R/$\overline{W}$	When this bit is 0, GPIO15 is configured as an input; otherwise, it is an output.
7	GPIO15 Polarity	R/$\overline{W}$	When this bit is 0, GPIO15 is active low; otherwise it is active high.

Table XIX. Register 0ch, EEPROM Register 2 (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	Factory Use	R	For factory use only. Do not write to this register.

Table XX. Register 0Dh, Internal Temperature $\overline{THERM}$ Limit (Power-On Default 37h (55°C))

Bit	Name	R/$\overline{W}$	Description
7–0	Int Temp $\overline{THERM}$ Limit	R/$\overline{W}$	This register contains the $\overline{THERM}$ limit for the Internal Temperature Channel. Exceeding this limit will cause the $\overline{THERM}$ output pin to be asserted.

Table XXI. Register 0Eh, TDM1 $\overline{THERM}$ Limit (Power-On Default 50h (80°C))

Bit	Name	R/$\overline{W}$	Description
7–0	TDM1 $\overline{THERM}$ Limit	R/$\overline{W}$	This register contains the $\overline{THERM}$ limit for the TDM1 Temperature Channel. Exceeding this limit will cause the $\overline{THERM}$ output pin to be asserted.

Table XXII. Register 0Fh, TDM2 $\overline{THERM}$ Limit (Power-On Default 50h (80°C))

Bit	Name	R/$\overline{W}$	Description
7–0	TDM2 $\overline{THERM}$ Limit	R/$\overline{W}$	This register contains the $\overline{THERM}$ limit for the TDM2 Temperature Channel. Exceeding this limit will cause the $\overline{THERM}$ output pin to be asserted.

Table XXIII. Register 10h, Internal Temperature T_{MIN} (Power-On Default 28h (40°C))

Bit	Name	R/$\overline{W}$	Description
7–0	Internal Temp T_{MIN}	R/$\overline{W}$	This register contains the T_{MIN} value for automatic fan speed control based on the Internal Temperature Channel.

Table XXIV. Register 11h, TDM1 Temperature T_{MIN} (Power-On Default 40h (64°C))

Bit	Name	R/$\overline{W}$	Description
7–0	TDM1 Temp T_{MIN}	R/$\overline{W}$	This register contains the T_{MIN} value for automatic fan speed control based on the TDM1 Temperature Channel.

Table XXV. Register 12h, TDM2 Temperature T_{MIN} (Power-On Default 40h (64°C))

Bit	Name	R/$\overline{W}$	Description
7–0	TDM2 Temp T_{MIN}	R/$\overline{W}$	This register contains the T_{MIN} value for automatic fan speed control based on the TDM2 Temperature Channel.

Table XXVI. Register 13h, EEPROM REGISTER 3 (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
0	Read	R/$\overline{W}$	Setting this bit puts the EEPROM into Read mode.
1	Write	R/$\overline{W}$	Setting this bit puts the EEPROM in Write (program) mode.
2	Erase	R/$\overline{W}$	Setting this bit puts the EEPROM into Erase mode.
3	Write Protect	R/$\overline{W}$ Once	Setting this bit protects the EEPROM against accidental writing or erasure. This bit is write–once and can only be cleared by power-on reset.
4	Test Mode bit 0	R/$\overline{W}$	Test mode bit. For factory use only.
5	Test Mode bit 1	R/$\overline{W}$	Test mode bit. For factory use only.
6	Test Mode bit 2	R/$\overline{W}$	Test mode bit. For factory use only.
7	Clock Extend	R/$\overline{W}$	Setting this bit enables SMBus clock extension. The ADM1026 can pull SCL low to extend the clock pulse if it cannot accept any more data. It is recommended to set this bit to 1 to extend the clock pulse during repeated EEPROM write or block write operations.

Table XXVII. Register 14h, Manufacturer's Test Register 1 (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	Manufacturer's Test 1	R/$\overline{W}$	This register is used by the manufacturer for test purposes. It should not be read from or written to in normal operation.

Table XXVIII. Register 15h, Manufacturer's Test Register 2 (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	Manufacturer's Test 2	R/$\overline{W}$	This register is used by the manufacturer for test purposes. It should not be read from or written to in normal operation.

Table XXIX. Register 16h, Manufacturer's ID (Power-On Default 41h)

Bit	Name	R/$\overline{W}$	Description
7–0	Manufacturer's ID Code	R	This register contains the manufacturer's ID code.

Table XXX. Register 17h, Revision Register (Power-On Default 4xh)

Bit	Name	R/$\overline{W}$	Description
3–0	Minor Revision Code	R	This nibble contains the manufacturer's code for minor revisions to the device. Rev 1 = 0h, Rev 2 = 1h, and so on.
7–4	Major Revision Code	R	This nibble denotes the generation of the device. For the ADM1026 this nibble will read 4h.

Table XXXI. Register 18h, Mask Register 1 (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
0	Ext1 Temp Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the Ext1 Temp channel are masked out.
1	Ext 2 Temp	R/$\overline{W}$	When this bit is set, interrupts generated on the Ext2/A_{IN9} channel are masked out.
2	3.3 V STBY Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the 3.3 V STBY Voltage channel are masked out.
3	3.3 V MAIN Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the 3.3 V MAIN Voltage channel are masked out.
4	+5 V Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the +5 V Voltage channel are masked out.
5	V_{CCP} Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the V_{CCP} Voltage channel are masked out.
6	+12 V Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the +12 V Voltage channel are masked out.
7	–12 V Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the –12 V Voltage channel are masked out.

Table XXXII. Register 19h, Mask Register 2 (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
0	A_{IN0} Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the A_{IN0} Voltage channel are masked out.
1	A_{IN1} Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the A_{IN1} Voltage channel are masked out.
2	A_{IN2} Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the A_{IN2} Voltage channel are masked out.
3	A_{IN3} Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the A_{IN3} Voltage channel are masked out.
4	A_{IN4} Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the A_{IN4} Voltage channel are masked out.
5	A_{IN5} Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the A_{IN5} Voltage channel are masked out.
6	A_{IN6} Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the A_{IN6} Voltage channel are masked out.
7	A_{IN7} Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the A_{IN7} Voltage channel are masked out.

Table XXXIII. Register 1Ah, Mask Register 3 (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
0	FAN0 Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the FAN0 Tach channel are masked out.
1	FAN1 Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the FAN1 Tach channel are masked out.
2	FAN2 Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the FAN2 Tach channel are masked out.
3	FAN3 Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the FAN3 Tach channel are masked out.
4	FAN4 Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the FAN4 Tach channel are masked out.
5	FAN5 Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the FAN5 Tach channel are masked out.
6	FAN6 Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the FAN6 Tach channel are masked out.
7	FAN7 Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the FAN7 Tach channel are masked out.

Table XXXIV. Register 1Bh, Mask Register 4 (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
0	Int Temp Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the Int Temp channel are masked out.
1	V_{BAT} Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the V_{BAT} Voltage channel are masked out.
2	A_{IN8} Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the A_{IN8} Voltage channel are masked out.
3	$\overline{THERM}$ Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated from $\overline{THERM}$ events are masked out.
4	AFC Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated from Automatic Fan Control events are masked out.
5	Unused	R	Unused. Will read back 0.
6	CI Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated by the Chassis Intrusion input are masked out.
7	GPIO16 Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the GPIO16 channel are masked out.

Table XXXV. Register 1Ch, Mask Register 5 (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
0	GPIO0 Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the GPIO0 channel are masked out.
1	GPIO1 Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the GPIO1 channel are masked out.
2	GPIO2 Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the GPIO2 channel are masked out.
3	GPIO3 Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the GPIO3 channel are masked out.
4	GPIO4 Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the GPIO4 channel are masked out.
5	GPIO5 Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the GPIO5 channel are masked out.
6	GPIO6 Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the GPIO6 channel are masked out.
7	GPIO7 Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the GPIO7 channel are masked out.

Table XXXVI. Register 1Dh, Mask Register 6 (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
0	GPIO8 Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the GPIO8 channel are masked out.
1	GPIO9 Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the GPIO9 channel are masked out.
2	GPIO10 Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the GPIO10 channel are masked out.
3	GPIO11Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the GPIO11 channel are masked out.
4	GPIO12 Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the GPIO12 channel are masked out.
5	GPIO13 Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the GPIO13 channel are masked out.
6	GPIO14 Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the GPIO14 channel are masked out.
7	GPIO15 Mask = 0	R/$\overline{W}$	When this bit is set, interrupts generated on the GPIO15 channel are masked out.

Table XXXVII. Register 1Eh, INT Temp Offset (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	Int Temp Offset	R/$\overline{W}$	This register contains the Offset Value for the Internal Temperature Channel. A two's complement number can be written to this register which is then 'added' to the measured result before it is stored or compared to limits. In this way, a sort of one–point calibration can be done whereby the whole transfer function of the channel can be moved up or down. From a software point of view, this may be a very simple method to vary the characteristics of the measurement channel if the thermal characteristics change, for whatever reason, for instance from one chassis to another, if the measurement point is moved, if a plug–in card is inserted or removed, and so on.

Table XXXVIII. Register 1Fh, INT Temp Measured Value (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	Int Temp Value	R	This register contains the measured value of the Internal Temperature Channel.

Table XXXIX. Register 20h, Status Register 1 (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
0	Ext1 Temp Status = 0	R	1, if Ext1 Value is above the High Limit or below the Low Limit on the previous conversion cycle, 0 otherwise. This bit is set (once only) if a $\overline{THERM}$ mode is engaged as a result of Ext1 temp readings exceeding the Ext1 $\overline{THERM}$ limit. This bit is also set (once only) if $\overline{THERM}$ mode is disengaged as a result of Ext1 temp readings going 5°C below Ext1 $\overline{THERM}$ limit.
1	Ext 2 Temp	R	1, if Ext 2 Value (or A_{IN9} if in voltage measurement mode) is above the /A_{IN9} Status = 0 High Limit or below the Low Limit on the previous conversion cycle, 0 otherwise. This bit is set (once only) if a $\overline{THERM}$ mode is engaged as a result of Ext2 temp readings exceeding the Ext2 $\overline{THERM}$ limit. This bit is also set (once only) if $\overline{THERM}$ mode is disengaged as a result of Ext2 temp readings going 5°C below Ext2 $\overline{THERM}$ limit.
2	3.3 V STBY Status = 0	R	1, if 3.3 V STBY Value is above the High Limit or below the Low Limit on the previous conversion cycle, 0 otherwise.
3	3.3 V MAIN Status = 0	R	1, if 3.3 V MAIN Value is above the High Limit or below the Low Limit on the previous conversion cycle, 0 otherwise.
4	+5 V Status = 0	R	1, if +5 V Value is above the High Limit or below the Low Limit on the previous conversion cycle, 0 otherwise.
5	V_{CCP} Status = 0	R	1, if V_{CCP} Value is above the High Limit or below the Low Limit on the previous conversion cycle, 0 otherwise.
6	+12 V Status = 0	R	1, if +12 V Value is above the High Limit or below the Low Limit on the previous conversion cycle, 0 otherwise.
7	–12 V Status = 0	R	1, if –12 V Value is above the High Limit or below the Low Limit on the previous conversion cycle, 0 otherwise.

Table XL. Register 21h, Status Register 2 (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
0	A_{IN0} Status = 0	R	1, if A_{IN0} Value is above the High Limit or below the Low Limit on the previous conversion cycle, 0 otherwise.
1	A_{IN1} Status = 0	R	1, if A_{IN1} Value is above the High Limit or below the Low Limit on the previous conversion cycle, 0 otherwise.
2	A_{IN2} Status = 0	R	1, if A_{IN2} Value is above the High Limit or below the Low Limit on the previous conversion cycle, 0 otherwise.
3	A_{IN3} Status = 0	R	1, if A_{IN3} Value is above the High Limit or below the Low Limit on the previous conversion cycle, 0 otherwise.
4	A_{IN4} Status = 0	R	1, if A_{IN4} Value is above the High Limit or below the Low Limit on the previous conversion cycle, 0 otherwise.
5	A_{IN5} Status = 0	R	1, if A_{IN5} Value is above the High Limit or below the Low Limit on the previous conversion cycle, 0 otherwise.
6	A_{IN6} Status = 0	R	1, if A_{IN6} Value is above the High Limit or below the Low Limit on the previous conversion cycle, 0 otherwise.
7	A_{IN7} Status = 0	R	1, if A_{IN7} Value is above the High Limit or below the Low Limit on the previous conversion cycle, 0 otherwise.

Table XLI. Register 22h, Status Register 3 (Power–On Default 00h)

Bit	Name	R/$\overline{W}$	Description
0	FAN0 Status 1 = 0	R	1, if FAN0 Value is above the High Limit on the previous conversion cycle, 0 otherwise.
1	FAN1 Status 1 = 0	R	1, if FAN1 Value is above the High Limit on the previous conversion cycle, 0 otherwise.
2	FAN2 Status 1 = 0	R	1, if FAN2 Value is above the High Limit on the previous conversion cycle, 0 otherwise.
3	FAN3 Status 1 = 0	R	1, if FAN3 Value is above the High Limit on the previous conversion cycle, 0 otherwise.
4	FAN4 Status 1 = 0	R	1, if FAN4 Value is above the High Limit on the previous conversion cycle, 0 otherwise.
5	FAN5 Status 1 = 0	R	1, if FAN5 Value is above the High Limit on the previous conversion cycle, 0 otherwise.
6	FAN6 Status 1 = 0	R	1, if FAN6 Value is above the High Limit on the previous conversion cycle, 0 otherwise.
7	FAN7 Status 1 = 0	R	1, if FAN7 Value is above the High Limit on the previous conversion cycle, 0 otherwise.

Table XLII. Register 23h, Status Register 4 (Power–On Default 00h)

Bit	Name	R/$\overline{W}$	Description
0	Int Temp Status = 0	R	1, if Int value is above the High Limit or below the Low Limit on the previous conversion cycle, 0 otherwise. This bit is set (once only) if a $\overline{THERM}$ mode is engaged as a result of Int temp readings exceeding the Int $\overline{THERM}$ limit. This bit is also set (once only) if $\overline{THERM}$ mode is disengaged as a result of Int temp readings going 5°C below Int $\overline{THERM}$ limit.
1	V_{BAT} Status = 0	R	1, if V_{BAT} Value is above the High Limit or below the Low Limit on the previous conversion cycle, 0 otherwise.
2	A_{IN8} Status = 0	R	1, if A_{IN8} Value is above the High Limit or below the Low Limit on the previous conversion cycle, 0 otherwise.
3	$\overline{THERM}$ Status = 0	R	This bit is set (once only) if a $\overline{THERM}$ mode is engaged as a result of temperature readings exceeding the $\overline{THERM}$ limits on any channel. This bit is also set (once only) if THERM mode is disengaged as a result of temperature readings going 5°C below $\overline{THERM}$ limits on any channel.
4	AFC Status = 0	R	This bit is set (once only) if the fan turns on when in automatic fan speed control (AFC) mode as a result of a temperature reading exceeding T_{MIN} on any channel. This bit is also set (once only) if the fan turns off when in automatic fan speed control mode.
5	Unused	R	Unused. Will read back 0.
6	CI Status = 0	R	This bit latches a Chassis Intrusion event.
7	GPIO16 Status = 0	R	When GPIO16 is configured as an input, this bit is set when GPIO16 is asserted. (“asserted” may be active high or active low depending on the setting in GPIO Configuration Register).
		R/$\overline{W}$	When GPIO16 is configured as an output, setting this bit asserts GPIO16. (“asserted” may be active high or active low depending on setting in GPIO Configuration Register).

Table XLIII. Register 24h, Status Register 5 (Power–On Default 00h)

Bit	Name	R/$\overline{W}$	Description
0	GPIO0 Status = 0	R	When GPIO0 is configured as an input, this bit is set when GPIO0 is asserted. (“asserted” may be active high or active low depending on setting of Bit 1 in GPIO Configuration Register 1).
		R/$\overline{W}$*	When GPIO0 is configured as an output, setting this bit asserts GPIO0. (“asserted” may be active high or active low depending on setting of Bit 1 in GPIO Configuration Register 1).
1	GPIO1 Status = 0	R	When GPIO1 is configured as an input, this bit is set when GPIO1 is asserted. (“asserted” may be active high or active low depending on setting of Bit 3 in GPIO Configuration Register 1).
		R/$\overline{W}$*	When GPIO1 is configured as an output, setting this bit asserts GPIO1. (“asserted” may be active high or active low depending on setting of Bit 3 in GPIO Configuration Register 1).
2	GPIO2 Status = 0	R	When GPIO2 is configured as an input, this bit is set when GPIO2 is asserted. (“asserted” may be active high or active low depending on setting of Bit 5 in GPIO Configuration Register 1).
		R/$\overline{W}$*	When GPIO2 is configured as an output, setting this bit asserts GPIO2. (“asserted” may be active high or active low depending on setting of Bit 5 in GPIO Configuration Register 1).
3	GPIO3 Status = 0	R	When GPIO3 is configured as an input, this bit is set when GPIO3 is asserted. (“asserted” may be active high or active low depending on setting of Bit 7 in GPIO Configuration Register 1).
		R/$\overline{W}$*	When GPIO3 is configured as an output, setting this bit asserts GPIO3. (“asserted” may be active high or active low depending on setting of Bit 7 in GPIO Configuration Register 1).
4	GPIO4 Status = 0	R	When GPIO4 is configured as an input, this bit is set when GPIO4 is asserted. (“asserted” may be active high or active low depending on setting of Bit 1 in GPIO Configuration Register 2).
		R/$\overline{W}$*	When GPIO4 is configured as an output, setting this bit asserts GPIO4. (“asserted” may be active high or active low depending on setting of Bit 1 in GPIO Configuration Register 2).

Table XLIII. Register 24h, Status Register 5 (Power–On Default 00h) (Continued)

Bit	Name	R/$\overline{W}$	Description
5	GPIO5 Status = 0	R	When GPIO5 is configured as an input, this bit is set when GPIO5 is asserted. (“asserted” may be active high or active low depending on setting of Bit 3 in GPIO Configuration Register 2).
		R/$\overline{W}$*	When GPIO5 is configured as an output, setting this bit asserts GPIO5. (“asserted” may be active high or active low depending on setting of Bit 3 in GPIO Configuration Register 2).
6	GPIO6 Status = 0	R	When GPIO6 is configured as an input, this bit is set when GPIO6 is asserted. (“asserted” may be active high or active low depending on setting of Bit 5 in GPIO Configuration Register 2).
		R/$\overline{W}$*	When GPIO6 is configured as an output, setting this bit asserts GPIO6. (“asserted” may be active high or active low depending on setting of Bit 5 in GPIO Configuration Register 2).
7	GPIO7 Status = 0	R	When GPIO7 is configured as an input, this bit is set when GPIO7 is asserted. (“asserted” may be active high or active low depending on setting of Bit 7 in GPIO Configuration Register 2).
		R/$\overline{W}$*	When GPIO7 is configured as an output, setting this bit asserts GPIO7. (“asserted” may be active high or active low depending on setting of Bit 7 in GPIO Configuration Register 2).

*GPIO status bits can be written only when a GPIO pin is configured as output. Read-only otherwise.

Table XLIV. Register 25h, Status Register 6 (Power–On Default 00h)

Bit	Name	R/$\overline{W}$	Description
0	GPIO8 Status = 0	R	When GPIO8 is configured as an input, this bit is set when GPIO8 is asserted. (“asserted” may be active high or active low depending on setting of Bit 1 in GPIO Configuration Register 3).
		R/$\overline{W}$*	When GPIO8 is configured as an output, setting this bit asserts GPIO8. (“asserted” may be active high or active low depending on setting of Bit 1 in GPIO Configuration Register 3).
1	GPIO9 Status = 0	R	When GPIO9 is configured as an input, this bit is set when GPIO9 is asserted. (“asserted” may be active high or active low depending on setting of Bit 3 in GPIO Configuration Register 3).
		R/$\overline{W}$*	When GPIO9 is configured as an output, setting this bit asserts GPIO9. (“asserted” may be active high or active low depending on setting of Bit 3 in GPIO Configuration Register 3).
2	GPIO10 Status = 0	R	When GPIO10 is configured as an input, this bit is set when GPIO10 is asserted. (“asserted” may be active high or active low depending on setting of Bit 5 in GPIO Configuration Register 3).
		R/$\overline{W}$*	When GPIO10 is configured as an output, setting this bit asserts GPIO10. (“asserted” may be active high or active low depending on setting of Bit 5 in GPIO Configuration Register 3).
3	GPIO11 Status = 0	R	When GPIO11 is configured as an input, this bit is set when GPIO11 is asserted. (“asserted” may be active high or active low depending on setting of Bit 7 in GPIO Configuration Register 3).
		R/$\overline{W}$*	When GPIO11 is configured as an output, setting this bit asserts GPIO11. (“asserted” may be active high or active low depending on setting of Bit 7 in GPIO Configuration Register 3).
4	GPIO12 Status = 0	R	When GPIO12 is configured as an input, this bit is set when GPIO12 is asserted. (“asserted” may be active high or active low depending on setting of Bit 1 in GPIO Configuration Register 4).
		R/$\overline{W}$*	When GPIO12 is configured as an output, setting this bit asserts GPIO12. (“asserted” may be active high or active low depending on setting of Bit 1 in GPIO Configuration Register 4).
5	GPIO13 Status = 0	R	When GPIO13 is configured as an input , this bit is set when GPIO13 is asserted. (“asserted” may be active high or active low depending on setting of Bit 3 in GPIO Configuration Register 4).
		R/$\overline{W}$*	When GPIO13 is configured as an output, setting this bit asserts GPIO13. (“asserted” may be active high or active low depending on setting of Bit 3 in GPIO Configuration Register 4).
6	GPIO14 Status = 0	R	When GPIO14 is configured as an input , this bit is set when GPIO14 is asserted. (“asserted” may be active high or active low depending on setting of Bit 5 in GPIO Configuration Register 4).
		R/$\overline{W}$*	When GPIO14 is configured as an output, setting this bit asserts GPIO14. (“asserted” may be active high or active low depending on setting of Bit 5 in GPIO Configuration Register 4).
7	GPIO15 Status = 0	R	When GPIO15 is configured as an input, this bit is set when GPIO15 is asserted. (“asserted” may be active high or active low depending on setting of Bit 7 in GPIO Configuration Register 4).
		R/$\overline{W}$*	When GPIO15 is configured as an output, setting this bit asserts GPIO15. (“asserted” may be active high or active low depending on setting of Bit 7 in GPIO Configuration Register 4).

*GPIO status bits can be written only when a GPIO pin is configured as output. Read-only otherwise.

Table XLV. Register 26h, V_{BAT} Measured Value (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	V_{BAT} Value	R	This register contains the measured value of the V_{BAT} analog input channel.

Table XLVI. Register 27h, A_{IN8} Measured Value (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	A_{IN8} Value	R	This register contains the measured value of the A_{IN8} analog input channel.

Table XLVII. Register 28h, EXT1 Measured Value (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	Ext1 Value	R	This register contains the measured value of the Ext1 Temp channel.

Table XLVIII. Register 29h, EXT2/A_{IN9} Measured Value (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	Ext2 Temp/ A_{IN9} Low Limit	R	This register contains the measured value of the Ext2 Temp/A_{IN9} channel depending on which one is configured.

Table XLIX. Register 2Ah, 3.3 V STBY Measured Value (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	3.3 V STBY Value	R	This register contains the measured value of the 3.3 V STBY voltage.

Table L. Register 2Bh, 3.3 V MAIN Measured Value (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	3.3 V MAIN Value	R	This register contains the measured value of the 3.3 V MAIN voltage.

Table LI. Register 2Ch, +5 V Measured Value (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	+5 V Value	R	This register contains the measured value of the +5 V analog input channel.

Table LII. Register 2Dh, VCCP Measured Value (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	V_{CCP} Value	R	This register contains the measured value of the V_{CCP} analog input channel.

Table LIII. Register 2Eh, +12V Measured Value (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	+12 V Value	R	This register contains the measured value of the +12 V analog input channel.

Table LIV. Register 2Fh, –12V Measured Value (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	–12 V Value	R	This register contains the measured value of the –12 V analog input channel.

Table LV. Register 30h, A_{IN0} Measured Value (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	A_{IN0} Value	R	This register contains the measured value of the A_{IN0} analog input channel.

Table LVI. Register 31h, A_{IN1} Measured Value (Power–On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	A_{IN1} Value	R	This register contains the measured value of the A_{IN1} analog input channel.

Table LVII. Register 32h, A_{IN2} Measured Value (Power–On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	A_{IN2} Value	R	This register contains the measured value of the A_{IN2} analog input channel.

Table LVIII. Register 33h, A_{IN3} Measured Value (Power–On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	A_{IN3} Value	R	This register contains the measured value of the A_{IN3} analog input channel.

Table LIX. Register 34h, A_{IN4} Measured Value (Power–On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	A_{IN4} Value	R	This register contains the measured value of the A_{IN4} analog input channel.

Table LX. Register 35h, A_{IN5} Measured Value (Power–On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	A_{IN5} Value	R	This register contains the measured value of the A_{IN5} analog input channel.

Table LXI. Register 36h, A_{IN6} Measured Value (Power–On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	A_{IN6} Value	R	This register contains the measured value of the A_{IN6} analog input channel.

Table LXII. Register 37h, A_{IN7} Measured Value (Power–On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	A_{IN7} Value	R	This register contains the measured value of the A_{IN7} analog input channel.

Table LXIII. Register 38h, FAN0 Measured Value (Power–On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	FAN0 Value	R	This register contains the measured value of the FAN0 tach input channel.

Table LXIV. Register 39h, FAN1 Measured Value (Power–On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	FAN1 Value	R	This register contains the measured value of the FAN1 tach input channel.

Table LXV. Register 3Ah, FAN2 Measured Value (Power–On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	FAN2 Value	R	This register contains the measured value of the FAN2 tach input channel.

Table LXVI. Register 3Bh, FAN3 Measured Value (Power–On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	FAN3 Value	R	This register contains the measured value of the FAN3 tach input channel.

Table LXVII. Register 3Ch, FAN4 Measured Value (Power–On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	FAN4 Value	R	This register contains the measured value of the FAN4 tach input channel.

Table LXVIII. Register 3Dh, FAN5 Measured Value (Power–On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	FAN5 Value	R	This register contains the measured value of the FAN5 tach input channel.

Table LXIX. Register 3Eh, FAN6 Measured Value (Power–On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	FAN6 Value	R	This register contains the measured value of the FAN6 tach input channel.

Table LXX. Register 3Fh, FAN7 Measured Value (Power–On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	FAN7 Value	R	This register contains the measured value of the FAN7 tach input channel.

Table LXXI. Register 40h, EXT1 High Limit (Power–On Default 64h/100°C)

Bit	Name	R/$\overline{W}$	Description
7–0	Ext1 High Limit	R/$\overline{W}$	This register contains the high limit of the Ext1 Temp channel.

Table LXXII. Register 41h, EXT2/A_{IN9} High Limit (Power-On Default 64h/100°C)

Bit	Name	R/$\overline{W}$	Description
7–0	Ext2 Temp/ A_{IN9} High Limit	R/$\overline{W}$	This register contains the high limit of the Ext2 Temp/A_{IN9} channel depending on which one is configured.

Table LXXIII. Register 42h, 3.3 V STBY High Limit (Power-On Default FFh)

Bit	Name	R/$\overline{W}$	Description
7–0	3.3 V STBY High Limit	R/$\overline{W}$	This register contains the high limit of the 3.3 V STBY analog input channel.

Table LXXIV. Register 43h, 3.3 V MAIN High Limit (Power-On Default FFh)

Bit	Name	R/$\overline{W}$	Description
7–0	3.3 V MAIN High Limit	R/$\overline{W}$	This register contains the high limit of the 3.3 V MAIN analog input channel.

Table LXXV. Register 44h, +5 V High Limit (Power-On Default FFh)

Bit	Name	R/$\overline{W}$	Description
7–0	+5 V High Limit	R/$\overline{W}$	This register contains the high limit of the +5 V analog input channel.

Table LXXVI. Register 45h, V_{CCP} High Limit (Power-On Default FFh)

Bit	Name	R/$\overline{W}$	Description
7–0	V_{CCP} High Limit	R/$\overline{W}$	This register contains the high limit of the V_{CCP} analog input channel.

Table LXXVII. Register 46h, +12 V High Limit (Power-On Default FFh)

Bit	Name	R/$\overline{W}$	Description
7–0	+12 V High Limit	R/$\overline{W}$	This register contains the high limit of the +12 V analog input channel.

Table LXXVIII. Register 47h, -12 V High Limit (Power-On Default FFh)

Bit	Name	R/W	Description
7–0	–12V High Limit	R/$\overline{W}$	This register contains the high limit of the –12 V analog input channel.

Table LXXIX. Register 48h, EXT1 Low Limit (Power-On Default 80h)

Bit	Name R/$\overline{W}$	Description	
7–0	Ext1 Low Limit	R/$\overline{W}$	This register contains the low limit of the Ext1 Temp channel.

Table LXXX. Register 49h, EXT2 / A_{IN9} Low Limit (Power-On Default 80h)

Bit	Name /$\overline{W}$	Description	
7–0	Ext2 Temp /A_{IN9} Low Limit	R/$\overline{W}$	This register contains the low limit of the Ext2 Temp/A_{IN9} channel depending on which one is configured.

Table LXXXI. Register 4Ah, 3.3 V STBY Low Limit (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	3.3 V STBY Low Limit	R/$\overline{W}$	This register contains the low limit of the 3.3 V STBY analog input channel.

Table LXXXII. Register 4Bh, 3.3 V MAIN Low Limit (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	3.3 V MAIN Low Limit	R/$\overline{W}$	This register contains the low limit of the 3.3 V MAIN analog input channel.

Table LXXXIII. Register 4Ch, +5V Low Limit (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	+5 V Low Limit	R/$\overline{W}$	This register contains the low limit of the +5 V analog input channel.

Table LXXXIV. Register 4Dh, V_{CCP} Low Limit (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	V_{CCP} Low Limit	R/$\overline{W}$	This register contains the low limit of the V_{CCP} analog input channel.

Table LXXXV. Register 4Eh, +12V Low Limit (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	+12 V Low Limit	R/$\overline{W}$	This register contains the low limit of the +12 V analog input channel.

Table LXXXVI. Register 4Fh, –12V Low Limit (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	–12 V Low Limit	R/$\overline{W}$	This register contains the low limit of the –12 V analog input channel.

Table LXXXVII. Register 50h, A_{IN0} High Limit (Power-On Default FFh)

Bit	Name	R/$\overline{W}$	Description
7–0	A_{IN0} High Limit	R/$\overline{W}$	This register contains the high limit of the A_{IN0} analog input channel.

Table LXXXVIII. Register 51h, A_{IN1} High Limit (Power-On Default FFh)

Bit	Name	R/$\overline{W}$	Description
7–0	A_{IN1} High Limit	R/$\overline{W}$	This register contains the high limit of the A_{IN1} analog input channel.

Table LXXXIX. Register 52h, A_{IN2} High Limit (Power-On Default FFh)

Bit	Name	R/W	Description
7–0	A_{IN2} High Limit	R/$\overline{W}$	This register contains the high limit of the A_{IN2} analog input channel.

Table XC. Register 53h, A_{IN3} High Limit (Power-On Default FFh)

Bit	Name	R/W	Description
7–0	A_{IN3} High Limit	R/$\overline{W}$	This register contains the high limit of the A_{IN3} analog input channel.

Table XCI. Register 54h, A_{IN4} High Limit (Power-On Default FFh)

Bit	Name	R/$\overline{W}$	Description
7–0	A_{IN4} High Limit	R/$\overline{W}$	This register contains the high limit of the A_{IN4} analog input channel.

Table XCII. Register 55h, A_{IN5} High Limit (Power-On Default FFh)

Bit	Name	R/$\overline{W}$	Description
7–0	A_{IN5} High Limit	R/W	This register contains the high limit of the A_{IN5} analog input channel.

Table XCIII. Register 56h, A_{IN6} High Limit (Power-On Default FFh)

Bit	Name	R/$\overline{W}$	Description
7–0	A_{IN6} High Limit	R/W	This register contains the high limit of the A_{IN6} analog input channel.

Table XCIV. Register 57h, A_{IN7} High Limit (Power-On Default FFh)

Bit	Name	R/$\overline{W}$	Description
7–0	A_{IN7} High Limit	R/$\overline{W}$	This register contains the high limit of the A_{IN7} analog input channel.

Table XCV. Register 58h, A_{IN0} Low Limit (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	A_{IN0} Low Limit	R/$\overline{W}$	This register contains the low limit of the A_{IN0} analog input channel.

Table XCVI. Register 59h, A_{IN1} Low Limit (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	A_{IN1} Low Limit	R/$\overline{W}$	This register contains the low limit of the A_{IN1} analog input channel.

Table XCVII. Register 5Ah, A_{IN2} Low Limit (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	A_{IN2} Low Limit	R/$\overline{W}$	This register contains the low limit of the A_{IN2} analog input channel.

Table XCVIII. Register 5Bh, A_{IN3} Low Limit (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	A_{IN3} Low Limit	R/$\overline{W}$	This register contains the low limit of the A_{IN3} analog input channel.

Table XCIX. Register 5Ch, A_{IN4} Low Limit (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	A_{IN4} Low Limit	R/$\overline{W}$	This register contains the low limit of the A_{IN4} analog input channel.

Table C. Register 5Dh, A_{IN5} Low Limit (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	A_{IN5} Low Limit	R/$\overline{W}$	This register contains the low limit of the A_{IN5} analog input channel.

Table CI. Register 5Eh, A_{IN6} Low Limit (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	A_{IN6} Low Limit	R/$\overline{W}$	This register contains the low limit of the A_{IN6} analog input channel.

Table CII. Register 5Fh, A_{IN7} Low Limit (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	A_{IN7} Low Limit	R/$\overline{W}$	This register contains the low limit of the A_{IN7} analog input channel.

Table CIII. Register 60h, FAN0 High Limit (Power-On Default FFh)

Bit	Name	R/$\overline{W}$	Description
7–0	FAN0 High Limit	R/W	This register contains the high limit of the FAN0 tach channel.

Table CIV. Register 61h, FAN1 High Limit (Power-On Default FFh)

Bit	Name	R/$\overline{W}$	Description
7–0	FAN1 High Limit	R/W	This register contains the high limit of the FAN1 tach channel.

Table CV. Register 62h, FAN2 High Limit (Power-On Default FFh)

Bit	Name	R/$\overline{W}$	Description
7–0	FAN2 High Limit	R/$\overline{W}$	This register contains the high limit of the FAN2 tach channel.

Table CVI. Register 63h, FAN3 High Limit (Power-On Default FFh)

Bit	Name	R/$\overline{W}$	Description
7–0	FAN3 High Limit	R/$\overline{W}$	This register contains the high limit of the FAN3 tach channel.

Table CVII. Register 64h, FAN4 High Limit (Power-On Default FFh)

Bit	Name	R/$\overline{W}$	Description
7–0	FAN4 High Limit	R/$\overline{W}$	This register contains the high limit of the FAN4 tach channel.

Table CVIII. Register 65h, FAN5 High Limit (Power-On Default FFh)

Bit	Name	R/$\overline{W}$	Description
7–0	FAN5 High Limit	R/$\overline{W}$	This register contains the high limit of the FAN5 tach channel.

Table CIX. Register 66h, FAN6 High Limit (Power-On Default FFh)

Bit	Name	R/$\overline{W}$	Description
7–0	FAN6 High Limit	R/$\overline{W}$	This register contains the high limit of the FAN6 tach channel.

Table CX. Register 67h, FAN7 High Limit (Power-On Default FFh)

Bit	Name	R/$\overline{W}$	Description
7–0	FAN7 High Limit	R/$\overline{W}$	This register contains the high limit of the FAN7 tach channel.

Table CXI. Register 68h, Int Temp High Limit (Power-On Default 50h (80°C))

Bit	Name	R/$\overline{W}$	Description
7–0	Int Temp High Limit	R/$\overline{W}$	This register contains the high limit of the internal temperature channel.

Table CXII. Register 69h, Int Temp Low Limit (Power-On Default 80h)

Bit	Name	R/$\overline{W}$	Description
7–0	Int Temp Low Limit	R/$\overline{W}$	This register contains the low limit of the internal temperature channel.

Table CXIII. Register 6Ah, V_{BAT} High Limit (Power-On Default FFh)

Bit	Name	R/$\overline{W}$	Description
7–0	V_{BAT} High Limit	R/W	This register contains the high limit of the V_{BAT} analog input channel.

Table CXIV. Register 6Bh, V_{BAT} Low Limit (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	V_{BAT} Low Limit	R/$\overline{W}$	This register contains the low limit of the V_{BAT} analog input channel.

Table CXV. Register 6Ch, A_{IN8} High Limit (Power-On Default FFh)

Bit	Name	R/$\overline{W}$	Description
7–0	A_{IN8} High Limit	R/$\overline{W}$	This register contains the high limit of the A_{IN8} analog input channel.

Table CXVI. Register 6Dh, A_{IN8} Low Limit (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	A_{IN8} Low Limit	R/$\overline{W}$	This register contains the low limit of the A_{IN8} analog input channel.

Table CXVII. Register 6Eh, EXT1 Temp Offset (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	Ext1 Temp Offset	R/$\overline{W}$	This register contains the Offset Value for the External 1 Temperature Channel. A two's complement number can be written to this register, which is then 'added' to the measured result before it is stored or compared to limits. In this way, a sort of one-point calibration can be done whereby the whole transfer function of the channel can be moved up or down. From a software point of view, this may be a very simple method to vary the characteristics of the measurement channel if the thermal characteristics change, for whatever reason, for instance from one chassis to another, if the measurement point is moved, if a plug-in card is inserted or removed, and so on.

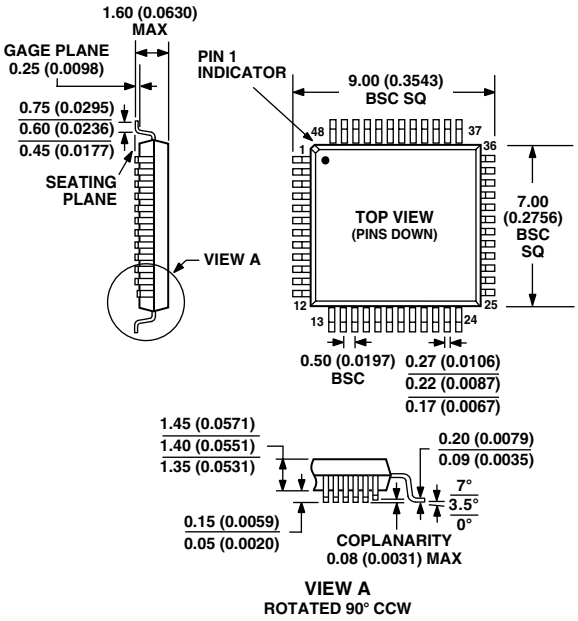
Table CXVIII. Register 6Fh, EXT2 Temp Offset (Power-On Default 00h)

Bit	Name	R/$\overline{W}$	Description
7–0	Ext2 Temp Offset	R/$\overline{W}$	This register contains the Offset Value for the External 2 Temperature Channel. A two's complement number can be written to this register, which is then 'added' to the measured result before it is stored or compared to limits. In this way, a sort of one-point calibration can be done whereby the whole transfer function of the channel can be moved up or down. From a software point of view, this may be a very simple method to vary the characteristics of the measurement channel if the thermal characteristics change, for whatever reason, for instance from one chassis to another, if the measurement point is moved, if a plug-in card is inserted or removed, and so on.

OUTLINE DIMENSIONS

48-Lead Thin Plastic Quad Flatpack [LQFP]
7 mm x 7 mm x 1.4 mm Thick
(ST-48)

Dimensions shown in millimeters and (inches)



CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

COMPLIANT TO JEDEC STANDARDS MS-026-BBC

C02657–0–5/02(0)

PRINTED IN U.S.A.