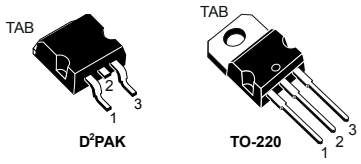
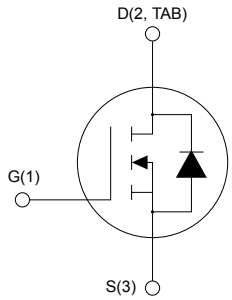
STB34NM60N, STP34NM60N

Datasheet

N-channel 600 V, 92 mΩ typ., 31.5 A MDmesh II Power MOSFETs in D²PAK and TO-220 packages





Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STB34NM60N	600 V	105 mΩ	31.5 A
STP34NM60N			

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using the second generation of MDmesh technology. These revolutionary Power MOSFETs associate a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. They are therefore suitable for the most demanding high-efficiency converters.

STPOWER

Product status links
STB34NM60N
STP34NM60N

Product summary	
Order code	**STB34NM60N**
Marking	34NM60N
Package	D²PAK
Packing	Tape and reel
Order code	**STP34NM60N**
Marking	34NM60N
Package	TO-220
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	31.5	A
	Drain current (continuous) at T_C = 100 °C	20	
I_{DM}(1)	Drain current (pulsed)	126	A
P_{TOT}	Total power dissipation at T_C = 25 °C	250	W
dv/dt(2)	Peak diode recovery voltage slope	15	V/ns
dv/dt(3)	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 31.5 A, di/dt ≤ 400 A/µs, V_{DS}(peak) ≤ $V_{(BR)DSS}$, V_{DD} = 480 V.*
3. *V_{DS} ≤ 480 V*

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		D²PAK	TO-220	
R_{thJC}	Thermal resistance, junction-to-case	0.5		°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	30(1)	62.5	°C/W

1. *When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max.)	7	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	345	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C(1)			100	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 14.5 A		92	105	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	2722	-	pF
C_{oss}	Output capacitance		-	173	-	pF
C_{rss}	Reverse transfer capacitance		-	1.75	-	pF
$C_{oss\ eq.}$(1)	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	458	-	pF
R_g	Gate input resistance	f = 1 MHz, open drain	-	2.9	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 31.5 A, V_{GS} = 0 to 10 V (see the Figure 14. Test circuit for gate charge behavior)	-	84	-	nC
Q_{gs}	Gate-source charge		-	14	-	nC
Q_{gd}	Gate-drain charge		-	45	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 15.75 A, R_G = 4.7 Ω, V_{GS} = 10 V (see the Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	18	-	ns
t_r	Rise time		-	36	-	ns
$t_{d(off)}$	Turn-off delay time		-	104	-	ns
t_f	Fall time		-	73	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	31.5	A
I_{SDM}(1)	Source-drain current (pulsed)		-	-	126	A
V_{SD}(2)	Forward on voltage	I_{SD} = 31.5 A, V_{GS} = 0 V	-	-	1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 31.5 A, di/dt = 100 V, V_{DD} = 60 V (see the Figure 15. Test circuit for inductive load switching and diode recovery times)	-	412		ns
Q_{rr}	Reverse recovery charge		-	8		µC
I_{RRM}	Reverse recovery current		-	39		A
t_{rr}	Reverse recovery time	I_{SD} = 31.5 A, di/dt = 100 A/µs, V_{DD} = 60 V T_J = 150 °C (see the Figure 15. Test circuit for inductive load switching and diode recovery times)	-	490		ns
Q_{rr}	Reverse recovery charge		-	10		µC
I_{RRM}	Reverse recovery current		-	43		A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

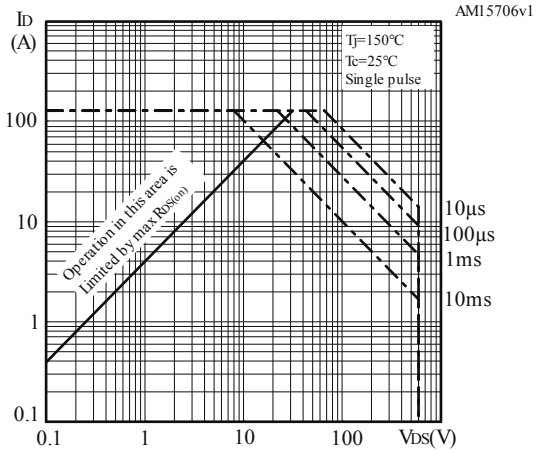


Figure 2. Normalized transient thermal impedance

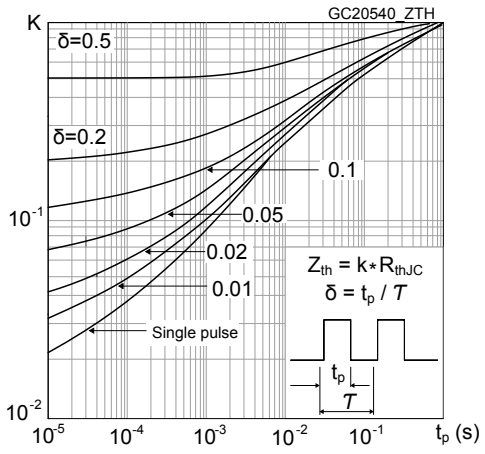


Figure 3. Typical output characteristics

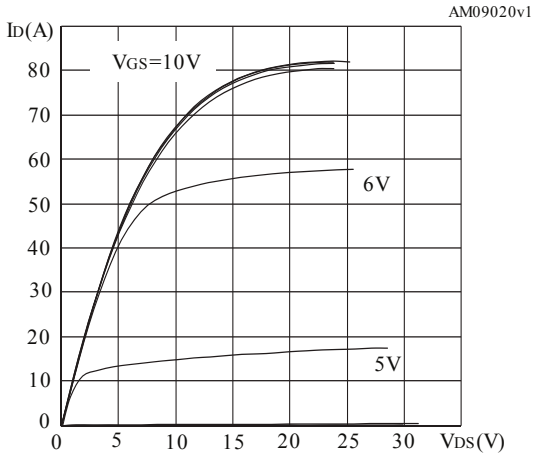


Figure 4. Typical transfer characteristics

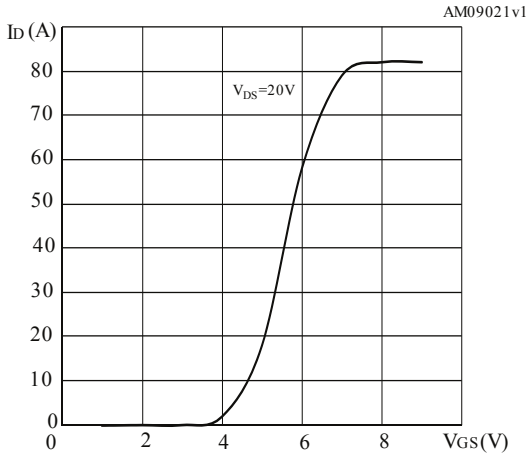


Figure 5. Typical gate charge vs gate-source voltage

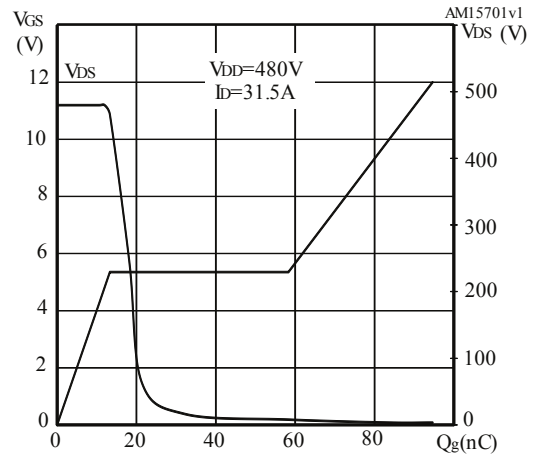


Figure 6. Typical drain-source on-resistance

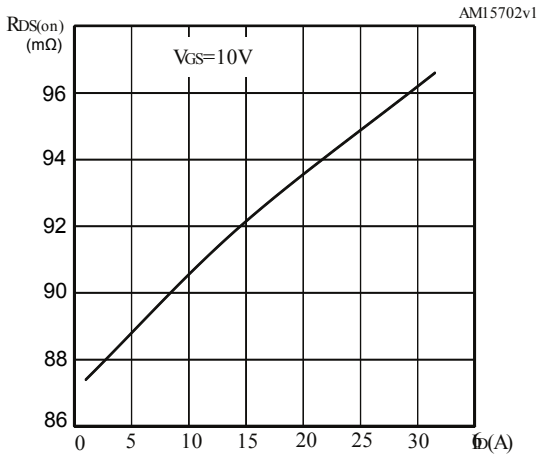


Figure 7. Typical capacitance characteristics

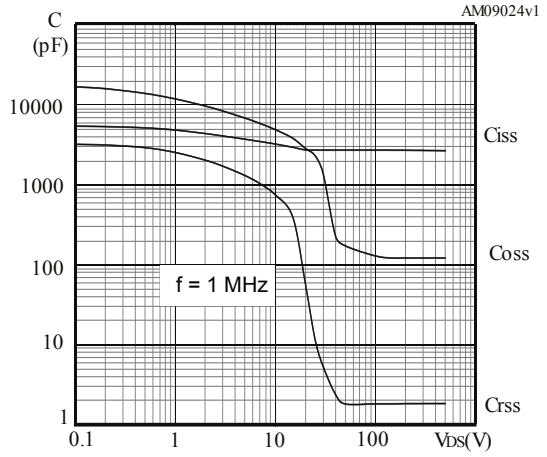


Figure 8. Typical output capacitance stored energy

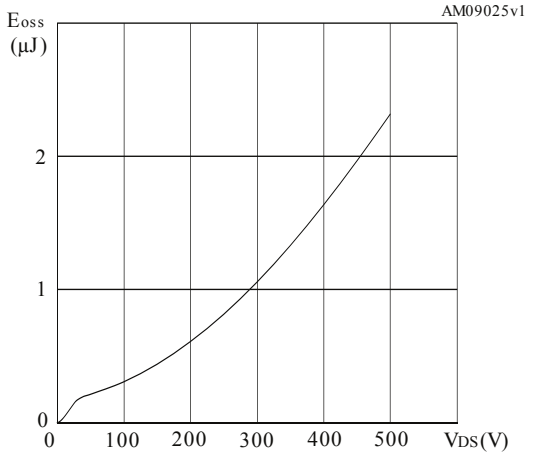


Figure 9. Normalized gate threshold vs temperature

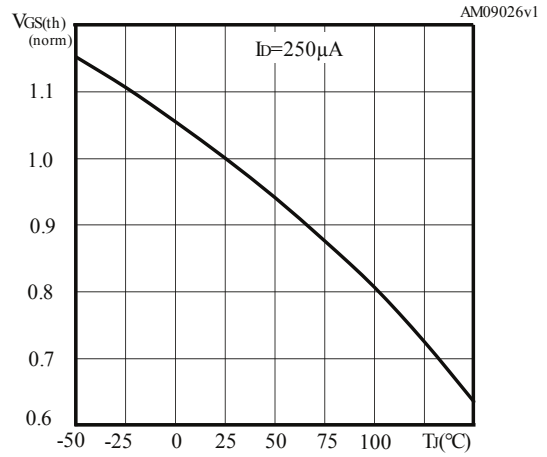


Figure 10. Normalized on-resistance vs temperature

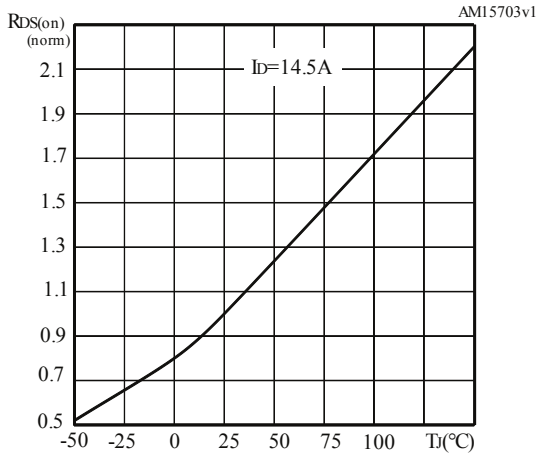


Figure 11. Normalized breakdown voltage vs temperature

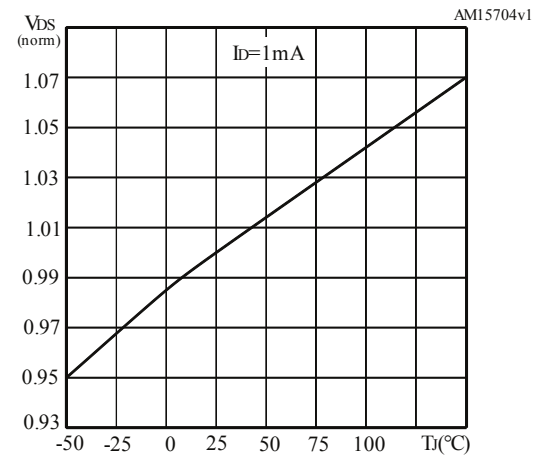
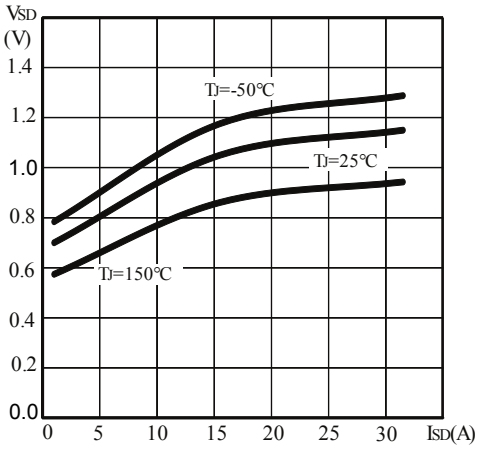


Figure 12. Typical reverse diode forward characteristics



3 Test circuits

Figure 13. Test circuit for resistive load switching times

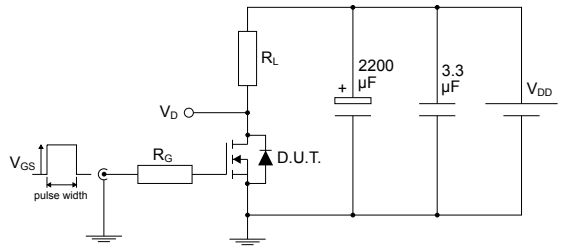


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Figure 14. Test circuit for gate charge behavior

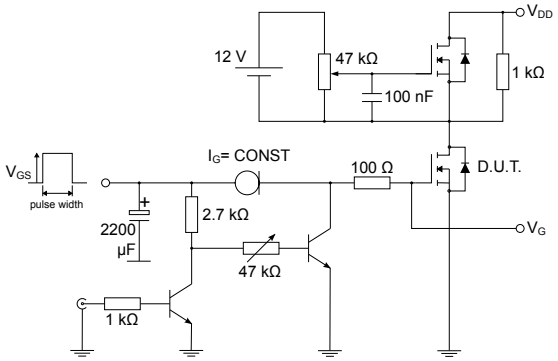

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Figure 15. Test circuit for inductive load switching and diode recovery times

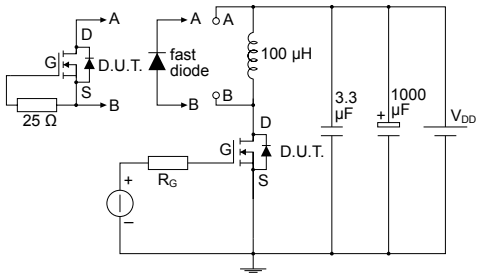

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Figure 16. Unclamped inductive load test circuit

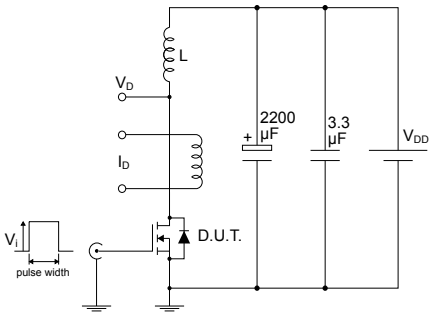

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Figure 17. Unclamped inductive waveform

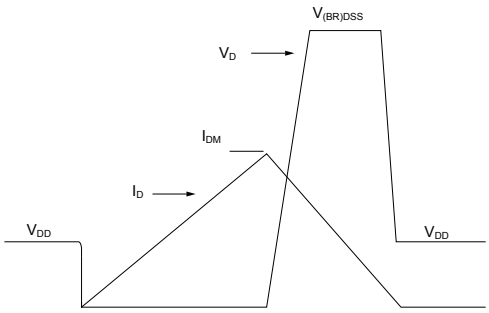

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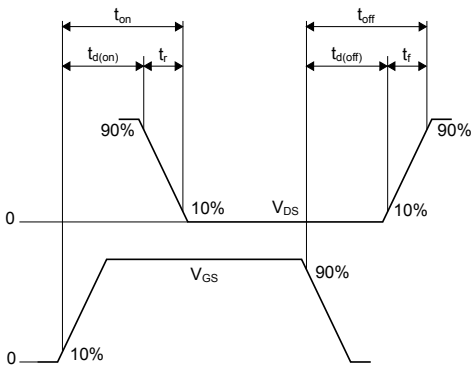
Figure 18. Switching time waveform



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4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A2 package information

Figure 19. D²PAK (TO-263) type A2 package outline

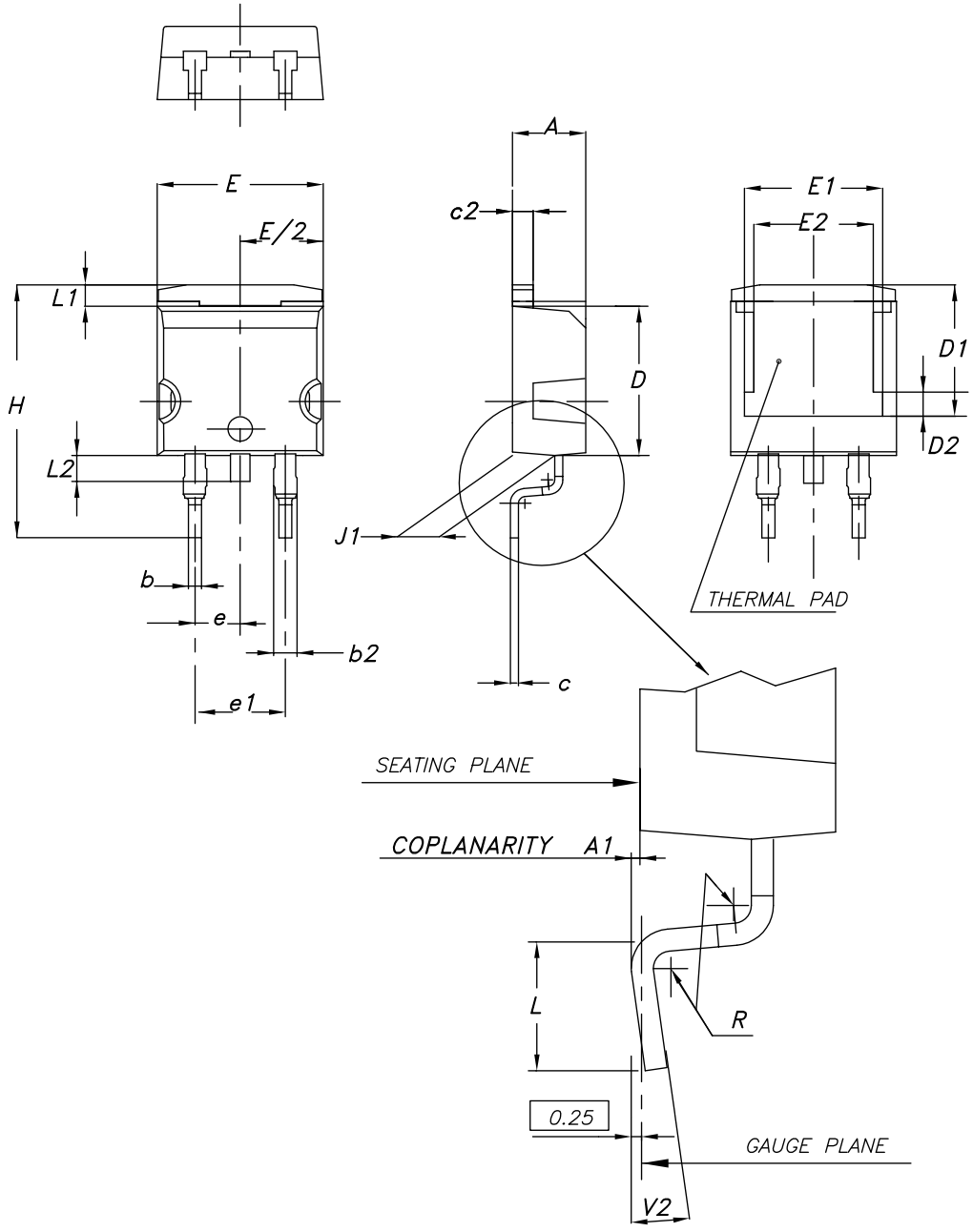
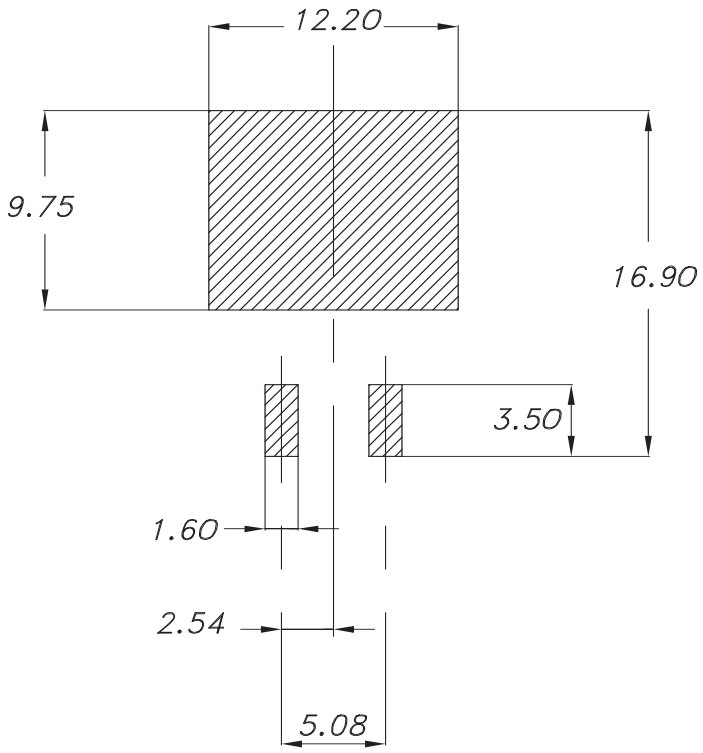


Table 8. **D²PAK (TO-263) type A2 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.70	8.90	9.10
E2	7.30	7.50	7.70
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

Figure 20. D²PAK (TO-263) recommended footprint (dimensions are in mm)



4.2 TO-220 type A package information

Figure 21. **TO-220 type A package outline**

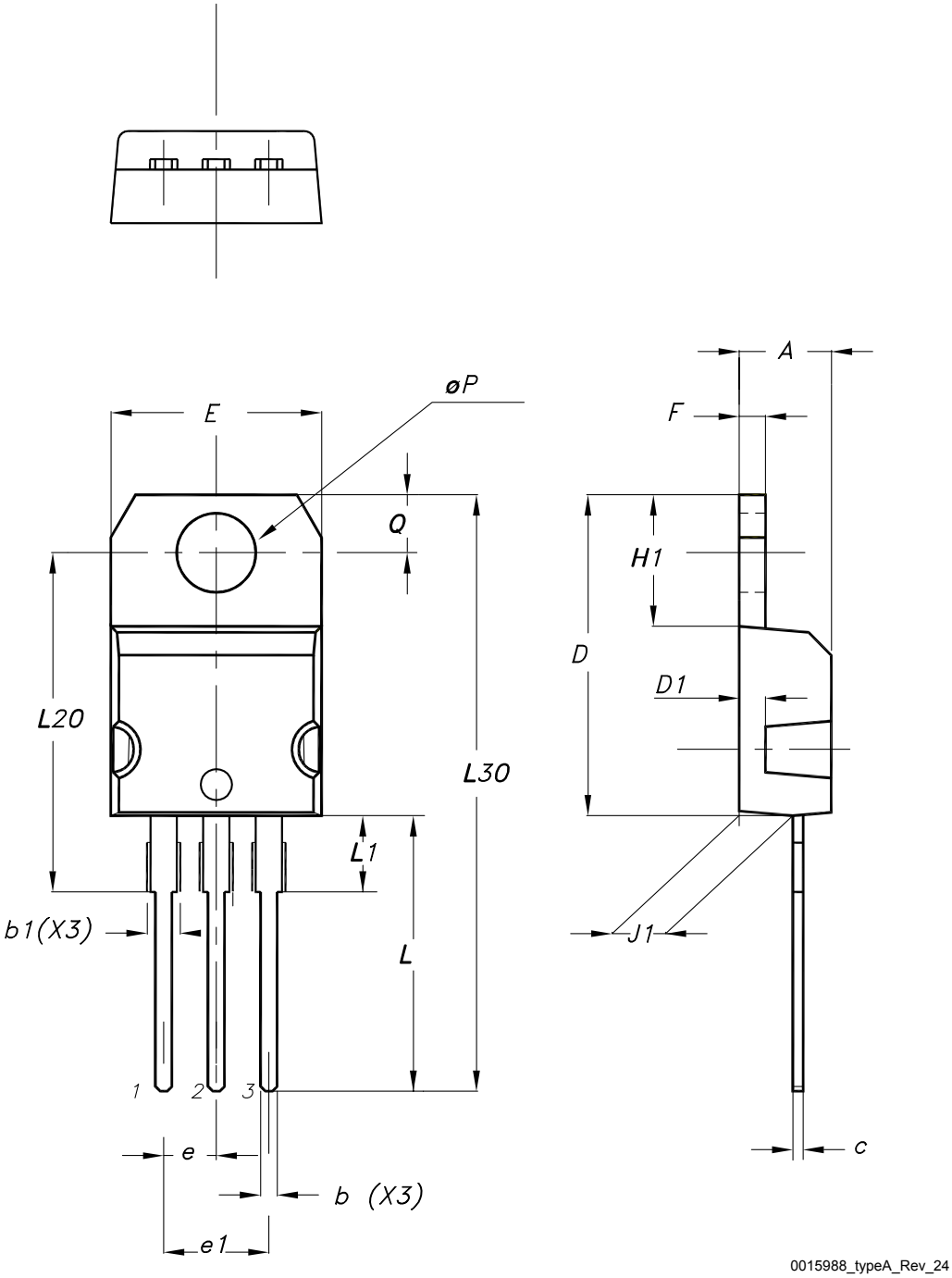
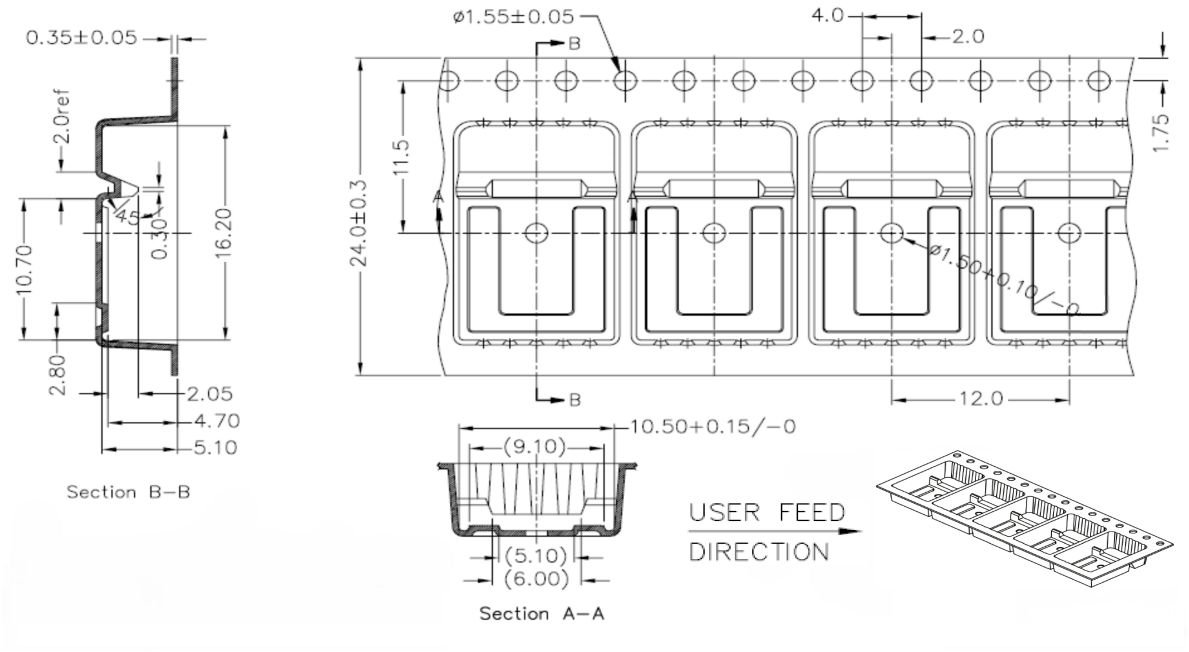


Table 9. **TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

4.3 D²PAK packing information

Figure 22. **D²PAK tape drawing (dimensions are in mm)**



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Revision history

Table 10. **Document revision history**

Date	Version	Changes
05-Aug-2010	1	Initial release.
02-Sep-2010	2	Updated title on cover page and Table 4: On/off states.
07-Apr-2011	3	Document status promoted from preliminary data to datasheet.
10-Oct-2011	4	Inserted new device in D2PAK: Updated: *Table 2: Absolute maximum ratings*, *Table 3: Thermal data* and *Section 4: Package information* with the new device. Inserted *Section 5: Packing information*. Minor text changes.
12-Dec-2011	5	– *Figure 9: Output capacitance stored energy* has been updated. – *Figure 10: Normalized gate threshold voltage vs temperature* has been updated. – *Figure 11: Normalized on-resistance vs temperature has been updated*. – *Figure 12: Normalized B_{VDSS} vs temperature* has been updated.
21-Dec-2011	6	Updated: *Table 2: Absolute maximum ratings* (V_{ISO} value for TO-220FP)
10-May-2012	7	*Figure 6: Gate charge vs gate-source voltage* has been updated.
01-Jul-2013	8	– The part number STF34NM60N has been moved to a separate datasheet. – Added: MOSFET ruggedness parameter and *3* on *Table 2* – Modified: ID value on *Table 5* and typical values for $t_{d(on)}$, t_r, $t_{d(off)}$ and t_f, max values for I_{SD} and I_{SDM}, I_{SD} for V_{SD}, typical value and I_{SD} for t_{rr} – Modified: *Figure 6*, *7*, *12* and *13* – Minor text changes
20-Mar-2015	9	– The part number STW34NM60N has been moved to a separate datasheet. – Updated *Section 4: Package information*. – Minor text changes.
22-Sep-2025	10	Updated Section 4: Package information. Minor text changes.

Contents

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