FAIRCHILD SEMICONDUCTOR®

April 2008

FIN12AC
Low-Voltage 12-Bit Bi-Directional Serializer/Deserializer with Multiple Frequency Ranges

Features

- Low power consumption
- Fairchild proprietary low-power CTL™ interface
- LVCMOS parallel I/O interface:
  – 2mA source / sink current
  – Over-voltage tolerant control signals
- Parallel I/O power supply (V_{DDP}) range between 1.65V and 3.6V
- Analog power supply range of 2.5V to 3.3V
- Multi-mode operation allows for a single device to operate as Serializer or Deserializer
- Internal PLL with no external components
- Standby power-down mode support
- Small footprint packaging:
  – 32-terminal MLP and 42-ball BGA
- Built-in differential termination
- Supports external CKREF frequencies; 5MHz to 40MHz
- Serialized data rate up to 560Mb/s
- Voltage translation from 1.65V to 3.6V

Applications

- Microcontroller or pixel interfaces
- Image sensors
- Small displays: LCD, cell phone, digital camera, portable gaming, printer, PDA, video camera, automotive

Description

The FIN12AC is a 12-bit serializer / deserializer capable of running a parallel frequency range between 5MHz and 40MHz, selected by the S1 and S2 control signals. The bi-directional data flow is controlled through use of a direction (DIRI) control pin. The devices can be configured to operate in a unidirectional mode only by hardwiring the DIRI pin. An internal Phase-Locked Loop (PLL) generates the required bit clock frequency for transfer across the serial link. Options exist for dual or single PLL operation, dependent upon system operational parameters. The device has been designed for low power operation and utilizes Fairchild proprietary low-power control Current Transistor Logic (CTL™) interface. The device also supports an ultra low power power-down mode for conserving power in battery-operated applications.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FIN12ACGFX	-30 to +70°C	42-Ball Ultra Small Scale Ball Grid Array (USS-BGA), JEDEC MO-195, 3.5mm Wide	Tape and Reel
FIN12ACMLX	-30 to +70°C	32-Terminal Molded Leadless Package (MLP), Quad, JEDEC MO-220, 5mm Square	Tape and Reel

Pb-free package per JEDEC J-STD-020B.

µSerDes™ is a trademark of Fairchild Semiconductor Corporation.

Functional Block Diagram

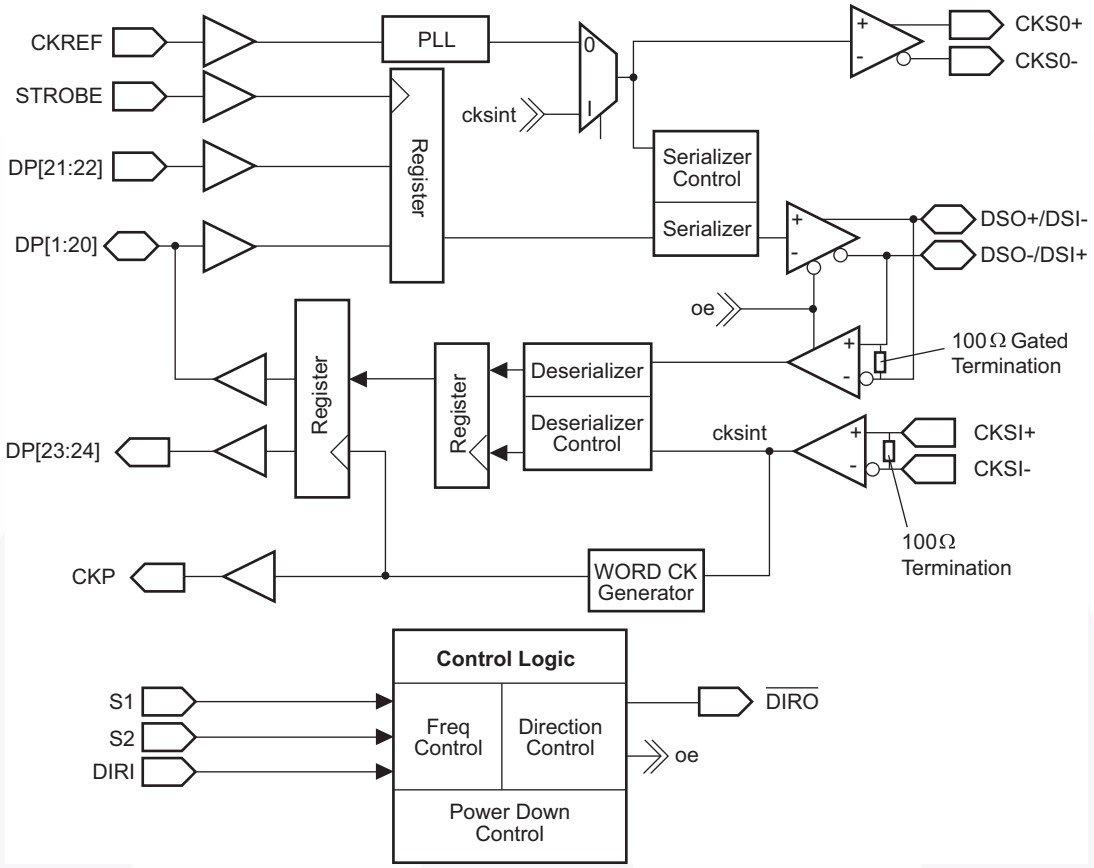


Figure 1. Block Diagram

Terminal Descriptions

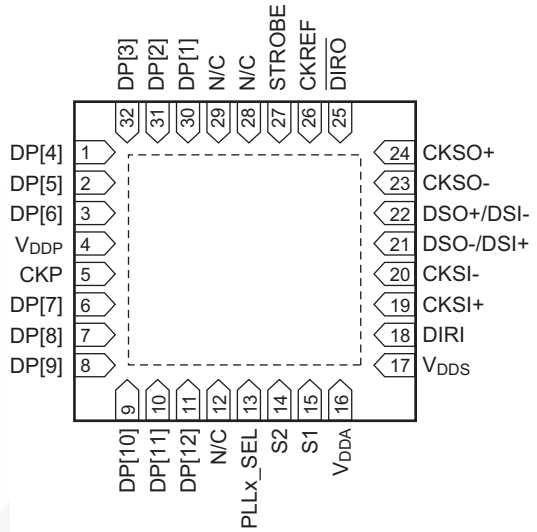
Pin Name	I/O Type	Number of Terminals	Description of Signals
DP[1:12]	I/O	12	LVCMOS parallel I/O, Direction controlled by DIRI pin
CKREF	IN	1	LVCMOS clock input and PLL reference
STROBE	IN	1	LVCMOS strobe signal for latching data into the serializer
CKP	OUT	1	LVCMOS word clock output. This signal is the regenerated STROBE signal
DSO+ / DSI- DSO- / DSI+	DIFF-I/O	2	CTL differential serial I/O data signals(1) DSO: Refers to output signal pair DSI: Refers to input signal pair DSO(I)+: Positive signal of DSO(I) pair DSO(I)-: Negative signal of DSO(I) pair
CKSI+ / CKSI-	DIFF-IN	2	CTL differential deserializer input bit clock CKSI: Refers to signal pair CKSI+: Positive signal of CKSI pair CKSI-: Negative signal of CKSI pair
CKSO+ / CKSO-	DIFF-OUT	2	CTL differential deserializer output bit clock CKSO: Refers to signal pair CKSO+: Positive signal of CKSO pair CKSO-: Negative signal of CKSO pair
S1	IN	1	Used to define frequency range for the RefClock, CKREF.
S2	IN	1	
PLLx_SEL	IN	1	Used to define PLL multiplication mode. PLLX_SEL = 0 multiplication factor 7-1/3x PLLX_SEL = 1 multiplication factor 7x
DIRI	IN	1	LVCMOS control input. Used to control direction of data flow: DIRI = “1” Serializer DIRI = “0” Deserializer
$\overline{\text{DIRO}}$	OUT	1	LVCMOS output, inversion of DIRI
V_{DDP}	Supply	1	Power supply for parallel I/O and translation circuitry
V_{DDS}	Supply	1	Power supply for core and serial I/O
V_{DDA}	Supply	1	Power supply for analog PLL circuitry
GND	Supply	0	Use bottom ground plane for ground signals

Note:

1 The DSO/DSI serial port pins have been arranged such that if one device is rotated 180° with respect to the other device, the serial connections properly aligns without the need for any traces or cable signals to cross. Other layout orientations may require that traces or cables cross.

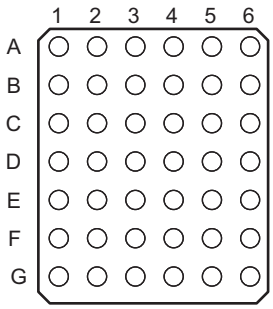
Pin Assignments

Terminal Assignments for MLP



(Top View)

Pin Assignments for BGA



(Top View)

Figure 2. Terminal and Pin Assignments

BGA Pin Assignments

	1	2	3	4	5	6
A	DP4	DP2	N/C	N/C	N/C	CKREF
B	DP6	DP5	DP1	N/C	STROBE	$\overline{\text{DIRO}}$
C	CKP	N/C	DP3	N/C	CKSO+	CKSO-
D	N/C	DP7	V_{DDP}	GND	DSO-/DSI+	DSO+/DSI-
E	DP8	DP9	GND	V_{DDS}	CKSI+	CKSI-
F	DP10	DP11	N/C	V_{DDA}	N/C	DIRI
G	DP12	N/C	N/C	PLLx_SEL	S2	S1

N/C = No Connect

Control Logic Circuitry

The FIN12AC can be used as a 12-bit serializer or a 12-bit deserializer. Terminals S1 and S2 must be set to accommodate the clock reference input frequency range of the serializer. Table 1 shows the terminal programming of these options based on the S1 and S2 control terminals. When DIRI is asserted LOW, the device is configured as a deserializer. When the DIRI terminal is asserted HIGH, the device is configured as a serializer. Changing the state on the DIRI signal reverses the direction of the I/O signals and generates the opposite state signal on $\overline{\text{DIRO}}$. For unidirectional operation, the DIRI terminal should be hardwired to the HIGH or LOW state and the $\overline{\text{DIRO}}$ terminal should be left floating. For bi-directional operation, the DIRI of the master device is driven by the system and the $\overline{\text{DIRO}}$ signal of the master is used to drive the DIRI of the slave device.

PLL Multiplier

The multiply select pin PLLx_SEL determines whether the PLL multiplication factor is 7 times the CKREF frequency or 7-1/3 times the CKREF frequency. Overclocking the PLL increases the range of spread spectrum on the CKREF input clock that can be tolerated.

Both of the PLL multiplier modes can work with a non-spread spectrum clock. When operating with the standard 7x multiplier and operating in a CKREF = STROBE mode, the serialized word is 14 data bits long. Each deserializer output period has the same period of the STROBE signal.

In the overclocking mode, the average deserializer period is the same as the STROBE signal. The individual periods vary between 14 and 16 data bits long. The pattern repeats every three cycles with two 14-bit cycles, followed by a third 16-bit cycle. The last two bits in the 16-bit cycle are zero. The deserializer output clock period has the same variation as the serializer outputs.

Turn-Around Functionality

The device passes and inverts the DIRI signal through the device asynchronously to the $\overline{\text{DIRO}}$ signal. Care must be taken by the system designer to ensure that no contention occurs between the deserializer outputs and the other devices on this port. Optimally the peripheral device driving the serializer should be put into a HIGH-impedance state prior to the DIRI signal being asserted.

When a device with dedicated data outputs turns from a deserializer to a serializer, the dedicated outputs remain at the last logical value asserted. This value only changes if the device is once again turned into a deserializer and the values are overwritten.

Power-Down Mode

Mode 0 is used for powering down and resetting the device. When both of the mode signals are driven to a LOW state, the PLL and references are disabled, differential input buffers are shut off, differential output buffers are placed into a HIGH-impedance state, LVCMOS outputs are placed into a HIGH-impedance state, LVCMOS inputs are driven to a valid level internally, and all internal circuitry are reset. The loss of CKREF state is also enabled to ensure that the PLL only powers up if there is a valid CKREF signal.

In a typical application mode, signals of the device do not change other than between the desired frequency range and the power-down mode. This allows for system-level power-down functionality to be implemented via a single wire for a SerDes pair. The S1 and S2 selection signals that have their operating mode driven to a “logic 0” should be hardwired to GND. The S1 and S2 signals that have their operating mode driven to a “logic 1” should be connected to a system-level power-down signal.

Table 1. Control Logic Circuitry

Mode Number	PLLx_SEL	S2	S1	DIRI	Description
0	X	0	0	X	Power-Down Mode
1	1	0	1	1	12-Bit Serializer, Standard Clocking, 20MHz to 40MHz CKREF
	0	0	1	1	12-Bit Serializer, Over-Clocked PLL, 19MHz to 38.2MHz CKREF
	X	0	1	0	12-Bit Deserializer
2	1	1	0	1	12-Bit Serializer, Standard Clocking, 5MHz to 14MHz CKREF
	0	1	0	1	12-Bit Serializer, Over-Clocked PLL, 4.7MHz to 13.3MHz CKREF
	X	1	0	0	12-Bit Deserializer
3	1	1	1	1	12-Bit Serializer, Standard Clocking, 8MHz to 28MHz CKREF
	0	1	1	1	12-Bit Serializer, Over-Clocked PLL, 9.5MHz to 26.7MHz CKREF
	X	1	1	0	12-Bit Deserializer

Serializer Operation Mode

The serializer configurations are described in the following sections. The basic serialization circuitry works similarly in these modes, but the actual data and clock streams differ, dependent on whether CKREF is the same as the STROBE signal. When it is stated that CKREF = STROBE, the CKREF and STROBE signals have an identical frequency of operation, but may or may not be phase aligned. When it is stated that CKREF does not equal STROBE, each signal is distinct and CKREF must be running at a frequency high enough to avoid any loss of data condition. CKREF must never be a lower frequency than STROBE.

Serializer Operation: Modes, 1, 2, 3 DIRI = 1, CKREF = STROBE

The PLL must receive a stable CKREF signal to achieve lock prior to valid data being sent. During PLL stabilization phase, STROBE should not be connected to the CKREF signal.

Once the PLL is stable and locked, the device can begin to capture and serialize data. Data is captured on the rising edge of the STROBE signal and serialized. When operating in serializer mode, the internal deserializer circuitry is disabled, including the DS input buffer. The CKSI serial inputs remain active to allow the pass through of the CKSI signal to the CKP output.

Serializer Operation: DIRI=1, CKREF Does Not = STROBE

If this mode is not needed, the CKSI inputs can either be driven to valid levels or left to float. For lowest power operation, let the CKSI inputs float.If the same signal is not used for CKREF and STROBE, the CKREF signal must be run at a higher frequency than the STROBE rate to serialize the data correctly. The actual serial transfer rate remains at 14 times the CKREF frequency. A data value of zero is sent when no valid data is present in the serial bit stream. The operation of the serializer otherwise remains the same.

The exact frequency that the reference clock needs is dependent upon the stability of the CKREF and STROBE signal. If the source of the CKREF signal implements spread spectrum technology, the minimum frequency of this spread spectrum clock should be used in calculating the ratio of STROBE frequency to the CKREF frequency. Similarly if the STROBE signal has significant cycle-to-cycle variation, the maximum cycle-to-cycle time needs to be factored into the selection of the CKREF frequency.

Serializer Operation: DIRI = 1, No CKREF

A third method of serialization uses a free-running bit clock on the CKSI signal. This is enabled by grounding the CKREF signal and driving the DIRI signal HIGH.

At power-up, the device is configured to accept a serialization clock from CKSI. If a CKREF is received, this device enables the CKREF serialization mode. The device remains in this mode even if CKREF is stopped. To re-enable this mode, the device must be powered down and powered back up with “logic 0” on CKREF.

Deserializer Operation Mode

The operation of the deserializer is dependent on the data received on the DSI data signal pair and the CKSI clock signal pair. The following sections describe the operation of the deserializer under distinct serializer source conditions. References to the CKREF and STROBE signals refer to the signals associated with the serializer device generating the serial data and clock signals that are inputs to the deserializer.

When operating in derserializer mode, the internal serializer circuitry is disabled, including the parallel data input buffers. If there is a CKREF signal provided, the CKSO serial clock continues to transmit bit clocks. When S1 and S2 are asserted low, all CMOS outputs are driven low at the output of the deserializer.

Deserializer Operation DIRI = 0 (Serializer Source: CKREF = STROBE

When the DIRI signal is asserted LOW, the device is configured as a deserializer. Data is captured on the serial port and deserializer through use of the bit clock sent with the data.

Deserializer Operation: PwrDwn = 1, $\overline{\text{DIRI}}$ = 0 (Serializer Source: CKREF Does Not = STROBE)

The logical operation of the deserializer remains the same if the CKREF is equal in frequency to the STROBE or at a higher frequency than the STROBE. The actual serial data stream presented to the deserializer differs because it has nonvalid data bits sent between words. The duty cycle of CKP varies based on the ratio of the frequency of the CKREF signal to the STROBE signal. The frequency of the CKP signal is equal to the STROBE frequency. The CKP HIGH time is equal to STROBE period - half of the CKREF period.

LVCMOS Data I/O

The LVCMOS input buffers have a nominal threshold value equal to half V_{DDP}. The input buffers are only operational when the device is operating as a serializer. When the device is operating as a deserializer, the inputs are gated off to conserve power.

The LVCMOS 3-STATE output buffers are rated for a source / sink current of 2mA at 1.8V. The outputs are active when the DIRI signal is asserted LOW. When the DIRI signal is asserted HIGH, the bi-directional LVCMOS I/Os are in HIGH-Z state. Under purely capacitive load conditions, the output swings between GND and V_{DDP}.

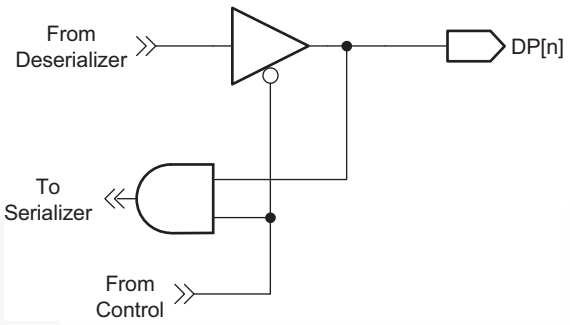


Figure 3. LVCMOS I/O

Application Mode Diagrams

Modes 1, 2, 3: Unidirectional Data Transfer

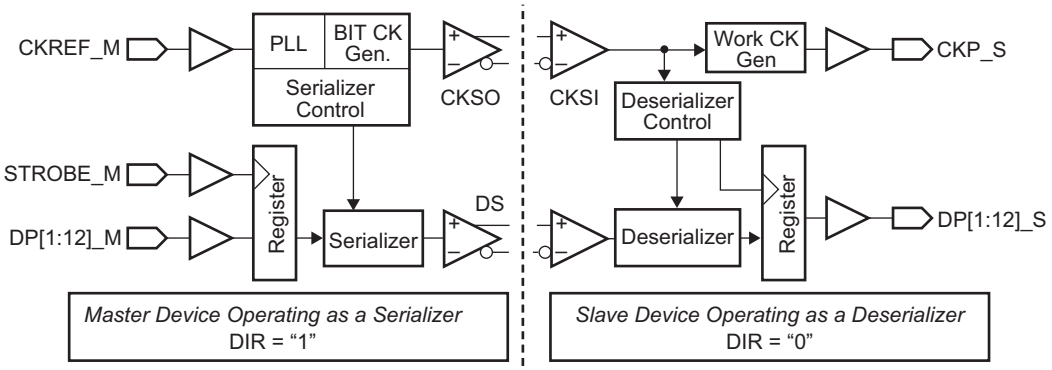


Figure 4. Simplified Block Diagram for Unidirectional Serializer and Deserializer

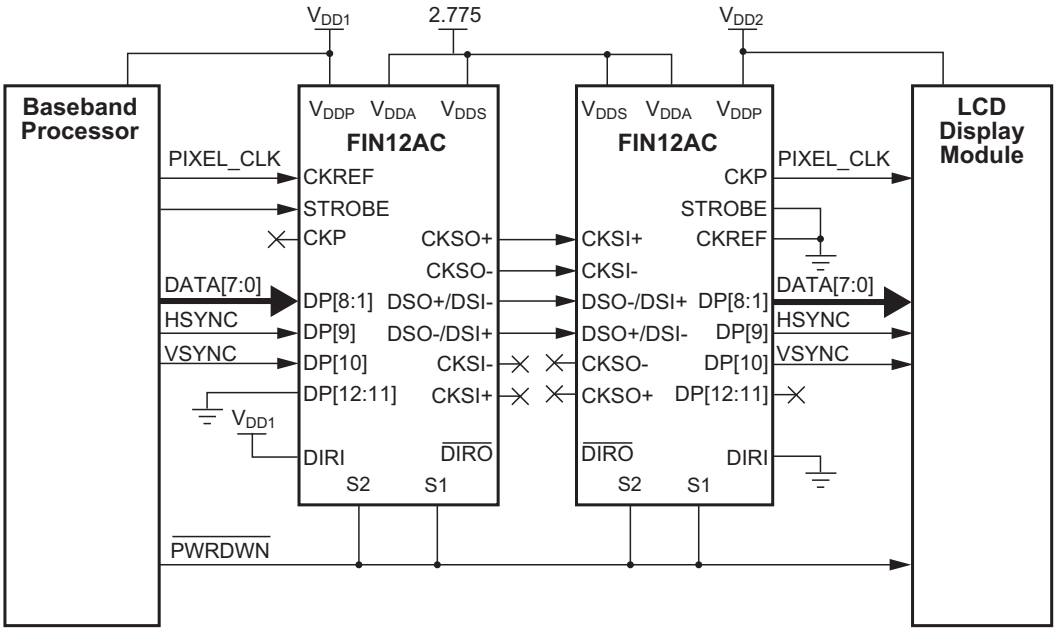
Figure 4. shows basic operation when a pair of µSerDes is configured in an unidirectional operation mode.

Master Operation:

1. During power-up, the device is configured as a serializer based on the value of the DIRI signal.
2. The device accepts CKREF_M word clock and generates a bit clock, which is sent to the slave device through the CKSO port.
3. The device receives parallel data on the rising edge of STROBE_M.
4. The device generates and transmits serialized data on the DS signals, which is source synchronous with CKSO.
5. The device generates an embedded word clock for each strobe signal.

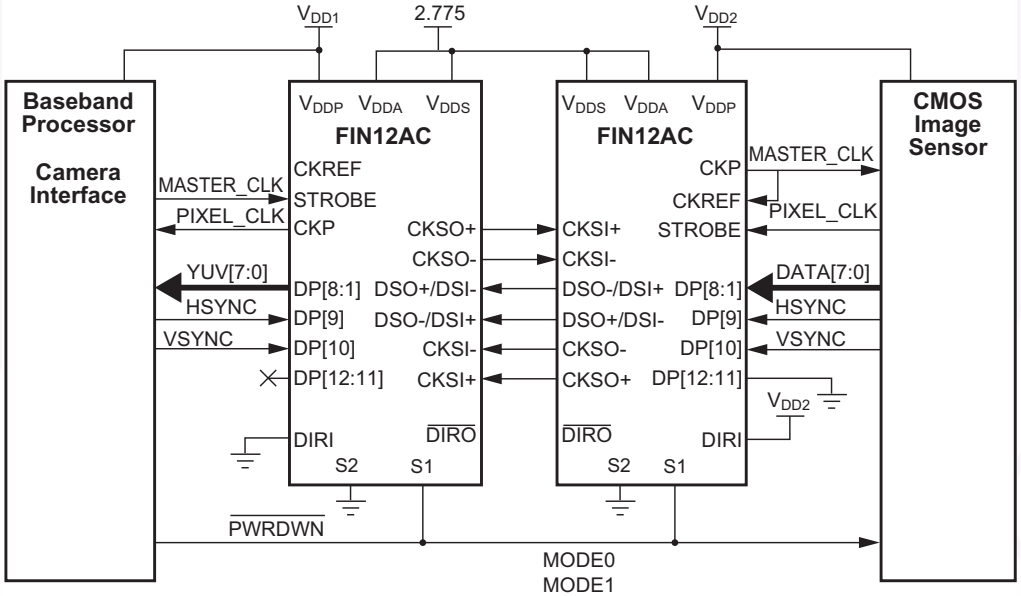
Slave Operation:

1. The device is configured as a deserializer at power-up based on the value of the DIRI signal.
2. The device accepts the bit clock on CKSI.
3. The device deserializes the DS data stream using the CKSI input clock.
4. The device writes parallel data onto the DP_S port and generates the CKP_S only when a valid data word occurs.



Note:
V_{DD1} does not have to equal V_{DD2}.

Figure 5. Unidirectional 8-bit RGB Interface (10MHz to 40MHz Operation)



Note:
V_{DD1} does not have to equal V_{DD2}.

Figure 6. Unidirectional 8-bit YUV Sensor with Master Clock on Base (10MHz to 40MHz Operation)

STROBE Pass-Through Mode

For some applications, it is desirable to pass a word clock across a differential signal pair in the opposite direction of serialization. The FIN12AC supports this mode of operation.

For the deserializer:

1. DIRI = LOW
2. CKREF = LOW
3. Word clock should be connected to the STROBE.

This passes the STROBE signal out the CKSO port.

For the serializer:

1. Connect CKSO of the deserializer to CKSI of the serializer.
2. CKSI passes the signal to CKP.

When PLL-bypass mode is used, the bit clock toggles on the CKP signal.

Table 2. Control I/O

Mode Number	DIRI	$\overline{\text{DIRO}}$	CKSO	CKP	Mode of Operation
0	x	Z	Z	Z	Power Down Mode: S2 = 0, S1 = 0
1, 2, 3	0	1	CKSO = STROBE	Deserializer Output STROBE	Deserializer: Any active mode
1, 2, 3	1	0	Serializer Output Bit Clock	CKSI	Serializer: Any active mode

Flex Circuit Design Guidelines

The serial I/O information is transmitted at a high serial rate. Care must be taken implementing this serial I/O flex cable. The following best practices should be used when developing the flex cabling or Flex PCB:

- Keep all four differential wires the same length.
- Allow no noisy signals over or near differential serial wires. Example: No LVCMOS traces over differential wires.
- Use only one ground plane or wire over the differential serial wires. Do not run ground over top and bottom.
- Do not place test points on differential serial wires.
- Use differential serial wires a minimum of 2cm away from the antenna.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply Voltage	-0.5	+4.6	V
	All Input/Output Voltage	-0.5	+4.6	V
I_{OS}	CTL Output Short-Circuit Duration	Continuous		
T_{STG}	Storage Temperature Range	-65	+150	°C
T_J	Maximum Junction Temperature		+150	°C
T_L	Lead Temperature (Soldering, 4 seconds)		+260	°C
ESD	Human Body Model, JESD22-A114,Serial I/O Pins		8.0	kV
	Human Body Model, JESD22-A114, All Pins		2.5	
	Charged Device Model, JESD22-C101		1.5	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{DDA}, V_{DDS}	Supply Voltage	2.5	3.3	V
V_{DDP}	Supply Voltage	1.65	3.6	V
T_A	Operating Temperature	-30	+70	°C
V_{DDA-PP}	Supply Noise Voltage		100	mV_{PP}

DC Electrical Characteristics

Over-supply voltage and operating temperature ranges, unless otherwise specified. Typical values are given for V_{DD} = 2.775V and T_A = 25°C. Positive current values refer to the current flowing into the device and negative values refer to current flowing out of pins. Voltages are referenced to GROUND unless otherwise specified (except ΔV_{OD} and V_{OD}).

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
LVCMOS I/O							
V_{IH}	Input High Voltage			0.65 x V_{DDP}		V_{DDP}	
V_{IL}	Input Low Voltage			GND		0.35 x V_{DDP}	V
V_{OH}	Output High Voltage	I_{OH} = –2.0mA	V_{DDP} = 3.3 ±0.30	0.75 x V_{DDP}			V
			V_{DDP} = 2.5 ±0.20				
			V_{DDP} = 1.8 ±0.15				
V_{OL}	Output Low Voltage	I_{OL} = 2.0mA	V_{DDP} = 3.3 ±0.30			0.25 x V_{DDP}	V
			V_{DDP} = 2.5 ±0.20				
			V_{DDP} = 1.8 ±0.15				
I_{IN}	Input Current	V_{IN} = 0V to 3.6V		–5.0		5.0	µA
Differential I/O							
I_{ODH}	Output HIGH Source Current	V_{OS} = 1.0V, Figure 7			–1.75		mA
I_{ODL}	Output LOW Sink Current	V_{OS} = 1.0V, Figure 7			0.950		mA
I_{OZ}	Disabled Output Leakage Current	CKSO, DSO = 0V to V_{DDS} S2 = S1 = 0V			±1.0	±5.0	µA
I_{IZ}	Disabled Input Leakage Current	CKSI, DSI = 0V to V_{DDS} S2 = S1 = 0V			±1.0	±5.0	µA
V_{ICM}	Input Common Mode Range	V_{DDS} = 2.775 ±5%			V_{GO} + 0.80		V
V_{GO}	Input Voltage Ground Offset Relative to Driver(2)	Figure 8			0		V
R_{TRM}	CKSI Internal Receiver Termination Resistor	V_{ID} = 50mV, V_{IC} = 925mV, DIRI = 0 $\lvert CKSI^+ - CKSI^- \rvert = V_{ID}$		80.0	100	120	Ω
R_{TRM}	CKSI Internal Receiver Termination Resistor	V_{ID} = 50mV, V_{IC} = 925mV, DIRI = 0 $\lvert DSI^+ - DSI^- \rvert = V_{ID}$		80.0	100	120	Ω

Note:

2 V_{GO} is the difference in device ground levels between the CTL driver and the CTL receiver.

Power Supply Currents

The worst-case test pattern produces a maximum toggling of internal digital circuits, CTL I/O and LVCMOS I/O with the PLL operating at the reference frequency unless otherwise specified. Maximum power is measured at the maximum V_{DD} values. Minimum values are measured at the minimum V_{DD} values. Typical values are measured at V_{DD} = 2.5V.

Symbol	Parameter	Test Conditions			Min.	Typ.	Max.	Unit
I_{DDA1}	V_{DDA} Serializer Static Supply Current	All DP and Control Inputs at 0V or V_{DD} NOCKREF, S2 = 0, S1 = 1, DIR = 1				437		µA
I_{DDA2}	V_{DDA} Deserializer Static Supply Current	All DP and Control Inputs at 0V or V_{DD} NOCKREF, S2 = 0, S1 = 1, DIR = 0				528		µA
I_{DDS1}	V_{DDS} Serializer Static Supply Current	All DP and Control Inputs at 0V or V_{DD} NOCKREF, S2 = 0, S1 = 1, DIR = 1				4.4		mA
I_{DDS2}	V_{DDS} Deserializer Static Supply Current	All DP and Control Inputs at 0V or V_{DD} NOCKREF, S2 = 0, S1 = 1, DIR = 0				5.5		mA
I_{DD_PD}	V_{DD} Power-Down Supply Current $I_{DD\_PD} = I_{DDA} + I_{DDS} + I_{DDP}$	S1 = S2 = 0 All Inputs at GND or V_{DD}				1.0		µA
I_{DD_SER1}	14:1 Dynamic Serializer Power Supply Current $I_{DD\_SER1} = I_{DDA} + I_{DDS} + I_{DDP}$	CKREF = STROBE DIRI = H Figure 10	S2 = H S1 = L	5MHz		8.5		mA
				14MHz		15.0		
			S2 = H S1 = H	10MHz		9.5		
				28MHz		17.0		
			S2 = L S1 = H	20MHz		11.0		
				40MHz		17.0		
I_{DD_DES1}	14:1 Dynamic Deserializer Power Supply Current $I_{DD\_DES1} = I_{DDA} + I_{DDS} + I_{DDP}$	CKREF = STROBE DIRI = L Figure 10	S2 = H S1 = L	5MHz		6.5		mA
				14MHz		7.5		
			S2 = H S1 = H	10MHz		7.0		
				28MHz		10.0		
			S2 = L S1 = H	20MHz		8.5		
				40MHz		11.5		

AC Electrical Characteristics

Characteristics at recommended over-supply voltage and operating temperature ranges, unless otherwise specified. Typical values are given for V_{DD} = 2.775V and T_A = 25°C. Positive current values refer to the current flowing into device and negative values refer to current flowing out of pins. Voltages are referenced to GROUND unless otherwise specified (except ΔV_{OD} and V_{OD}).

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
Serializer Input Operating Conditions							
t_{TCP}	CKREF Clock Period (5MHz – 40MHz)	CKREF = STROBE Figure 13	S2=1 S1=0	71.0		200	ns
			S2=1 S1=1	35.0		100	
			S2=0 S1=1	25.0		50.0	
f_{REF}	CKREF Frequency Relative to STROBE Frequency	CKREF does not = STROBE	S2=1 S1=0	1.1 x f_{STROBE}		40	MHz
			S2=1 S1=0			14	
			S2=0 S1=1			28	
t_{CPWH}	CKREF Clock High Time			0.2	0.5		T
t_{CPWL}	CKREF Clock Low Time			0.2	0.5		T
t_{CLKT}	LVCMOS Input Transition Time	Figure 13				90.0	ns
t_{SPWH}	STROBE Pulse Width HIGH/LOW	Figure 13		(T x 4)/14		(T x 12)/14	ns
f_{MAX}	Maximum Serial Data Rate	CKREF x 14	S2=0 S1=1	280		540	Mb/s
			S2=1 S1=0	70		196	
			S2=1 S1=1	140		392	
t_{STC}	$DP_{(n)}$ Setup to STROBE	DIRI = 1 Figure 3 (f = 5MHz)		2.5			ns
t_{HTC}	$DP_{(n)}$ Hold to STROBE			2.0			ns
Serializer AC Electrical Characteristics							
t_{TCCD}	Transmitter Clock Input to Clock Output Delay	DIRI = 1, a=(1/f)/14 CKREF = STROBE,		23a+1.5		21a+6.5	ns
t_{SPOS}	CKSO Position Relative to DS(3)	Figure 17		-200		200	ps
PLL AC Electrical Characteristics							
t_{TPLLS0}	Serializer Phase-Lock Loop Stabilization Time	Figure 15				200	µs
t_{TPLLD0}	PLL Disable Time Loss of Clock	Figure 18				30.0	µs
t_{TPLLD1}	PLL Power-Down Time(4)	Figure 19				20.0	ns
Deserializer AC Electrical Characteristics							
t_{RCOP}	Deserializer Clock Output (CKP OUT) Period	Figure 14		17.8		200	ns
t_{RCOL}	CKP OUT Low Time	Figure 14 (Rising Edge Strobe) Serializer source STROBE = CKREF where a = (1/f)/14		7a–3		7a+3	ns
t_{RCOH}	CKP OUT High Time(6)			7a–3		7a+3	ns
t_{PDV}	Data Valid to CKP LOW(6)	Figure 14 (Rising Edge Strobe) where a = (1/f)/14		7a–3		7a+3	ns
t_{ROLH}	Output Rise Time (20% to 80%)	C_L = 5pF Figure 11			3.5	7.0	ns
t_{ROHL}	Output Fall Time (80% to 20%)				3.5	7.0	ns

Notes:

3 Skew is measured from either the rising or falling edge of CKSO clock to the rising or falling edge of data (DSO). Signals are edge aligned. Both outputs should have identical load conditions for this test to be valid.

4 The power-down time is a function of the CKREF frequency prior to CKREF being stopped HIGH or LOW and the state of the S1/S2 mode pins. The specific number of clock cycles required for the PLL to be disabled varies dependent upon the operating mode of the device.

5 Signals are transmitted from the serializer source synchronously. Note that, in some cases, data is transmitted when the clock remains at a HIGH state. Skew should only be measured when data and clock are transitioning at the same time. Total measured input skew would be a combination of output skew from the serializer, load variations, and ISI and jitter effects.

6 Rising edge of CKP appears approximately 13 bit times after the falling edge of the CKP output. Falling edge of CKP occurs approximately 8 bit times after a data transition or 6 bit times after the falling edge of CKSO. Variation of the data with respect to the CKP signal is due to internal propagation delay differences of the data and CKP path and propagation delay differences on the various data pins. Note that if the CKREF is not equal to STROBE for the serializer, the CKP signal does not maintain a 50% duty cycle.The low time of CKP remains 13 bit times.

Control Logic Timing Controls

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
t_{PHL_DIR}, t_{PLH_DIR}	Propagation Delay DIRI-to-$\overline{DIRO}$	DIRI LOW-to-HIGH or HIGH-to-LOW			17	ns
t_{PLZ}, t_{PHZ}	Propagation Delay DIRI-to-DP	DIRI LOW-to-HIGH			25	ns
t_{PZL}, t_{PZH}	Propagation Delay DIRI-to-DP	DIRI HIGH-to-LOW			25	ns
t_{PLZ}, t_{PHZ}	Deserializer Disable Time S0 or S1 to DP	DIRI = 0, S1(2) = 0 and S2(1) = LOW-to-HIGH Figure 21			25	ns
t_{PZL}, t_{PZH}	Deserializer Enable Time S0 or S1 to DP(7)	DIRI = 0, S1(2) = 0 and S2(1) = LOW-to-HIGH Figure 21			2	µs
t_{PLZ}, t_{PHZ}	Serializer Disable Time S0 or S1 to CKSO, DS	DIRI = 1, S1(2) = 0 and S2(1) = HIGH-to-LOW Figure 20			25	ns
t_{PZL}, t_{PZH}	Serializer Enable Time S0 or S1 to CKSO, DS	DIRI = 1, S1(2) and S2(1) = LOW-to-HIGH Figure 20			65	ns

Note:

7 Serializer enable time includes the amount of time required for internal voltage and current references to stabilize. This time is significantly less than the PLL lock time and does not limit overall system startup time.

Capacitance

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
C_{IN}	Capacitance of Input Only Signals, CKREF, STROBE, S1, S2, DIRI	DIRI = 1, S1 = 0, S2=0, V_{DD} = 2.5V		2		pF
C_{IO}	Capacitance of Parallel Port Pins DP[1:12]	DIRI = 1, S1 = 0, S2=0, V_{DD} = 2.5V		2		pF
$C_{IO-DIFF}$	Capacitance of Differential I/O Signals	DIRI = 1, S2=0, S1 = 0, V_{DD} = 2.5V		2		pF

AC Loading and Waveforms

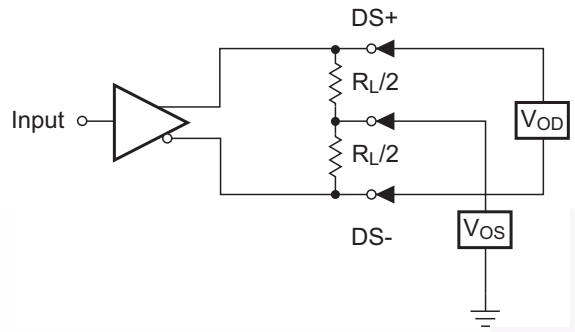


Figure 7. Differential CTL Output DC Test Circuit

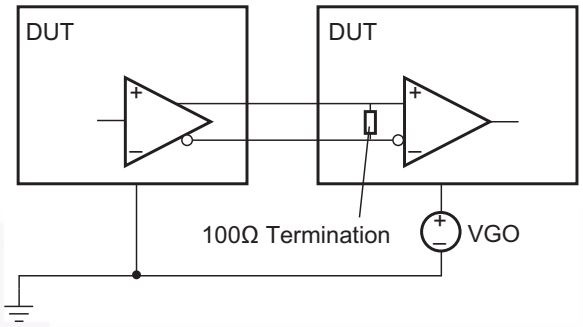
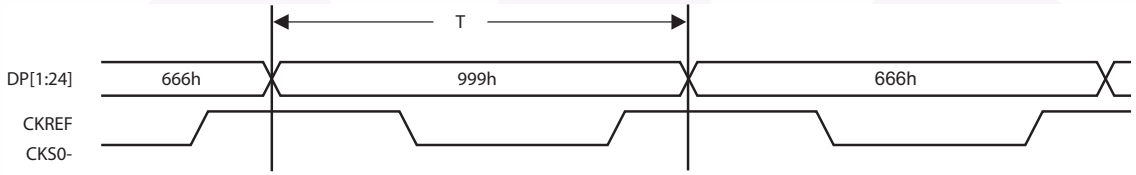
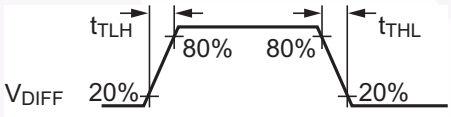


Figure 8. CTL Input Common Mode Test Circuit



Note:
The "worst-case" test pattern produces a maximum toggling of internal digital curcuits, CTL I/O and LVCMOS I/O with PLL operating at the reference frequency, unless otherwise specified. Maximum power is measured at the maximum V_{DD} values. Minimum values are measured at the minimum V_{DD} values. Typical values are measured at V_{DD} = 2.5V.

Figure 9. "Worst Case" Serializer Test Pattern



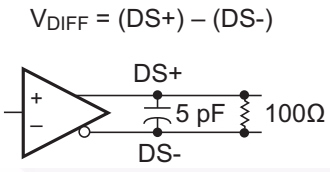
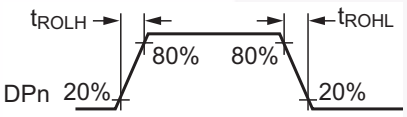


Figure 10. CTL Output Load and Transition Times



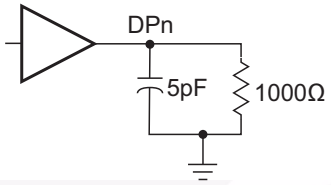
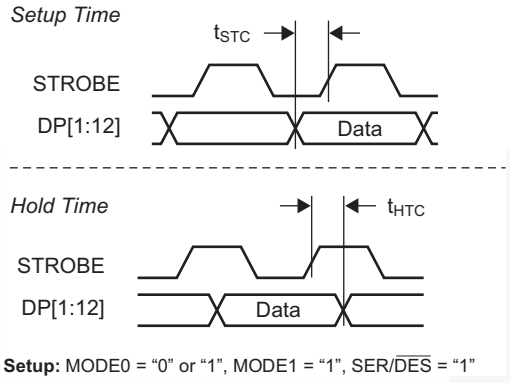


Figure 11. LVCMOS Output Load and Transition Times

AC Loading and Waveforms (Continued)



Setup: MODE0 = "0" or "1", MODE1 = "1", SER/$\overline{DES}$ = "1"

Figure 12. Serial Setup and Hold Time

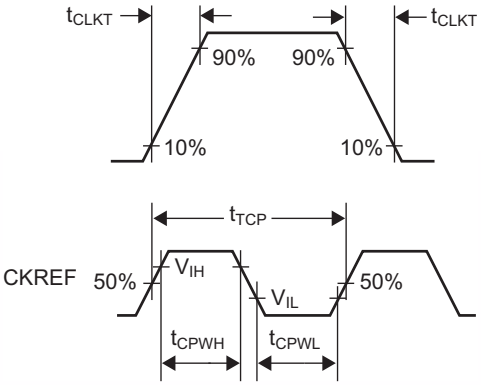
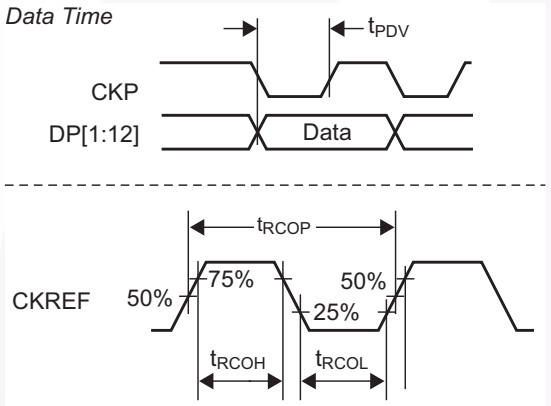
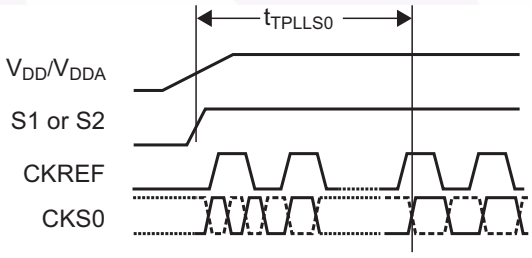


Figure 13. LVCMOS Clock Parameters



Setup: $\overline{DIRI}$ = "0", CKSI and DS are valid signals.

Figure 14. Deserializer Data Valid Window Time and Clock Output Parameters



Note: CKREF Signa is free running.

Figure 15. Serializer PLL Lock Time

AC Loading and Waveforms (Continued)

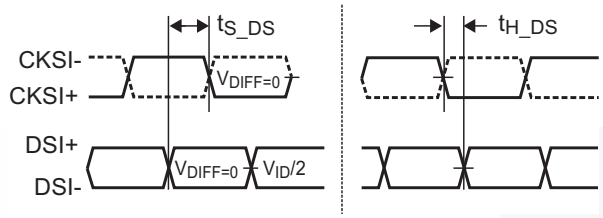


Figure 16. Differential Input Setup and Hold Times

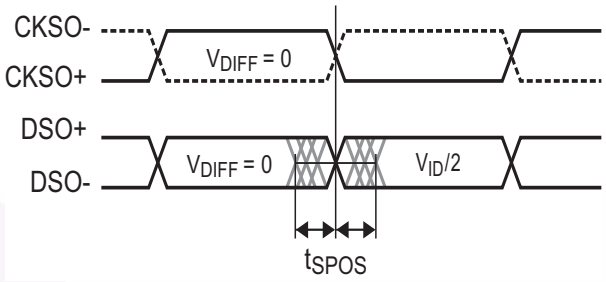
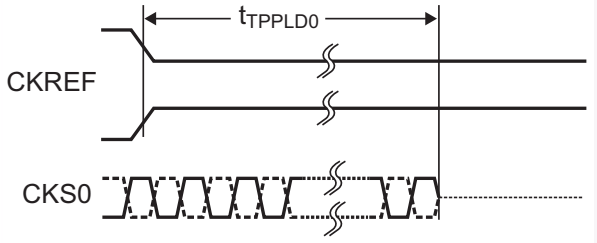


Figure 17. Differential Output Signal Skew



Note: CKREF Signal can be stopped either High or LOW.

Figure 18. PLL Loss of Clock Disable Time

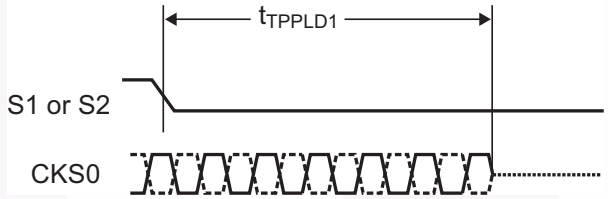
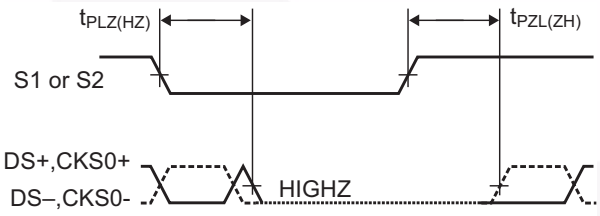
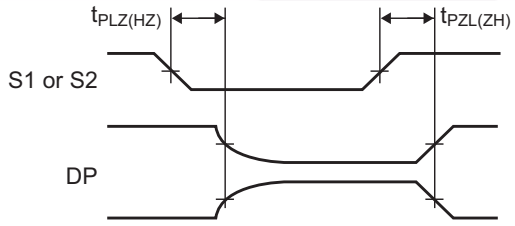


Figure 19. PLL Power-Down Time



Note: CKREF must be active and PLL must be stable.

Figure 20. Serializer Enable and Disable Time



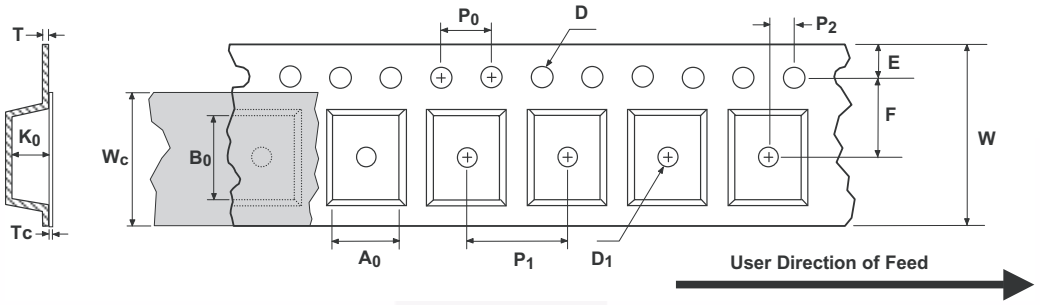
Note: If S1(2) transitioning, then S2(1) must = 0 for test to be valid.

Figure 21. Deserializer Enable and Disable Times

Tape and Reel Specification

MLP Embossed Tape Dimension

Dimensions are in millimeters.



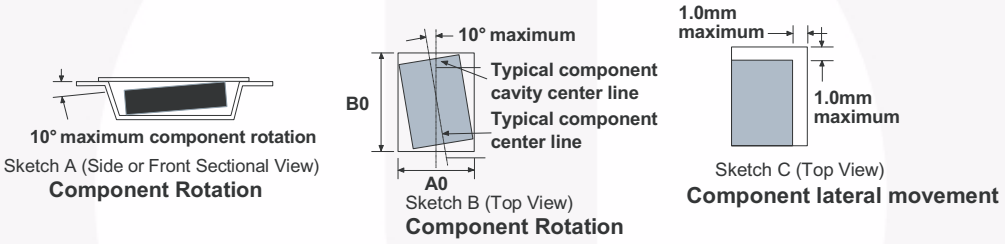
Package	A_0 ±0.1	B_0 ±0.1	D ±0.05	D_1 Min.	E ±0.1	F ±0.1	K_0 ±0.1	P_1 Typ.	P_0 Typ.	P_2 ±0/05	T Typ.	T_C ±0.005	W ±0.3	W_C Typ.
5 x 5	5.35	5.35	1.55	1.50	1.75	5.50	1.40	8.00	4.00	2.00	0.30	0.07	12.00	9.30
6 x 6	6.30	6.30	1.55	1.50	1.75	5.50	1.40	8.00	4.00	2.00	0.30	0.07	12.00	9.30

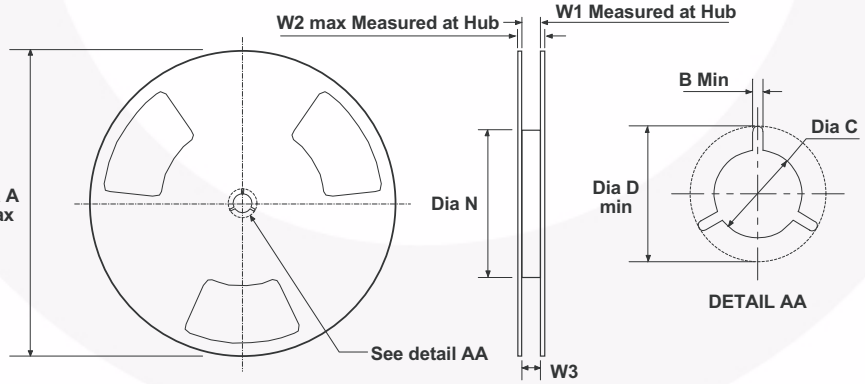
Notes:

Ao, Bo, and Ko dimensions are determined with respect to the EIA/JEDEC RS-481 rotational and lateral movement requirements (see sketches A, B, and C).

Shipping Reel Dimensions

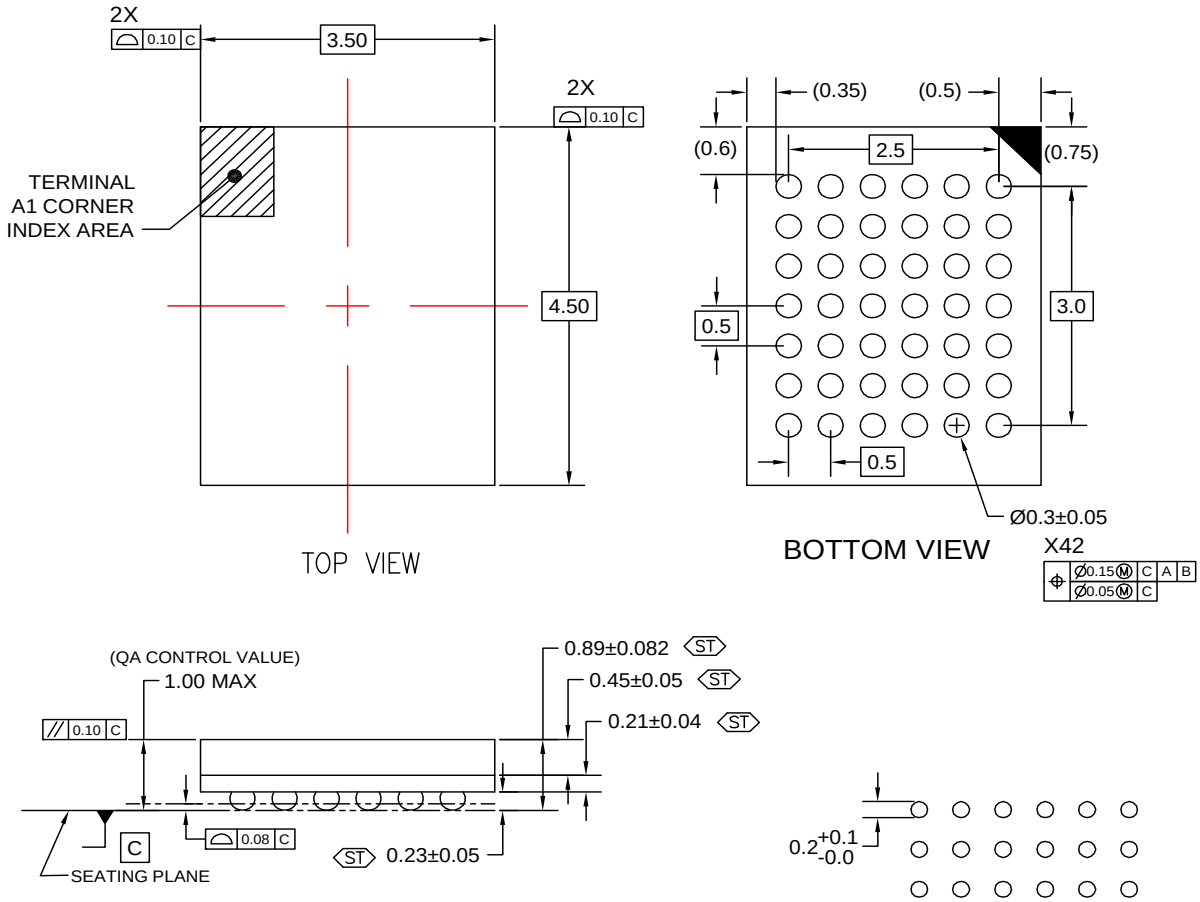
Dimensions are in millimeters.





Tape Width	Dia A Max.	Dim B Min.	Dia C +0.5/–0.2	Dia D Min.	Dim N Min.	Dim W1 +2.0/–0	Dim W2 Max.	Dim W3 (LSL–USL)
8	330.0	1.5	13.0	20.2	178.0	8.4	14.4	7.9 ~ 10.4
12	330.0	1.5	13.0	20.2	178.0	12.4	18.4	11.9 ~ 15.4
16	330.0	1.5	13.0	20.2	178.0	16.4	22.4	15.9 ~ 19.4

Physical Dimensions



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO−195,

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

D. STATISTICAL TOLERANCING FOR REFERENCE REFER TO MAX DIMENSION FOR QA INSPECTION

E. LAND PATTERN RECOMENDATION PER IPC−7351 TABLE14−15 LAND PATTERN NAME PER TABLE 3−15: BGA50P+6X7−42

BGA42ArevB

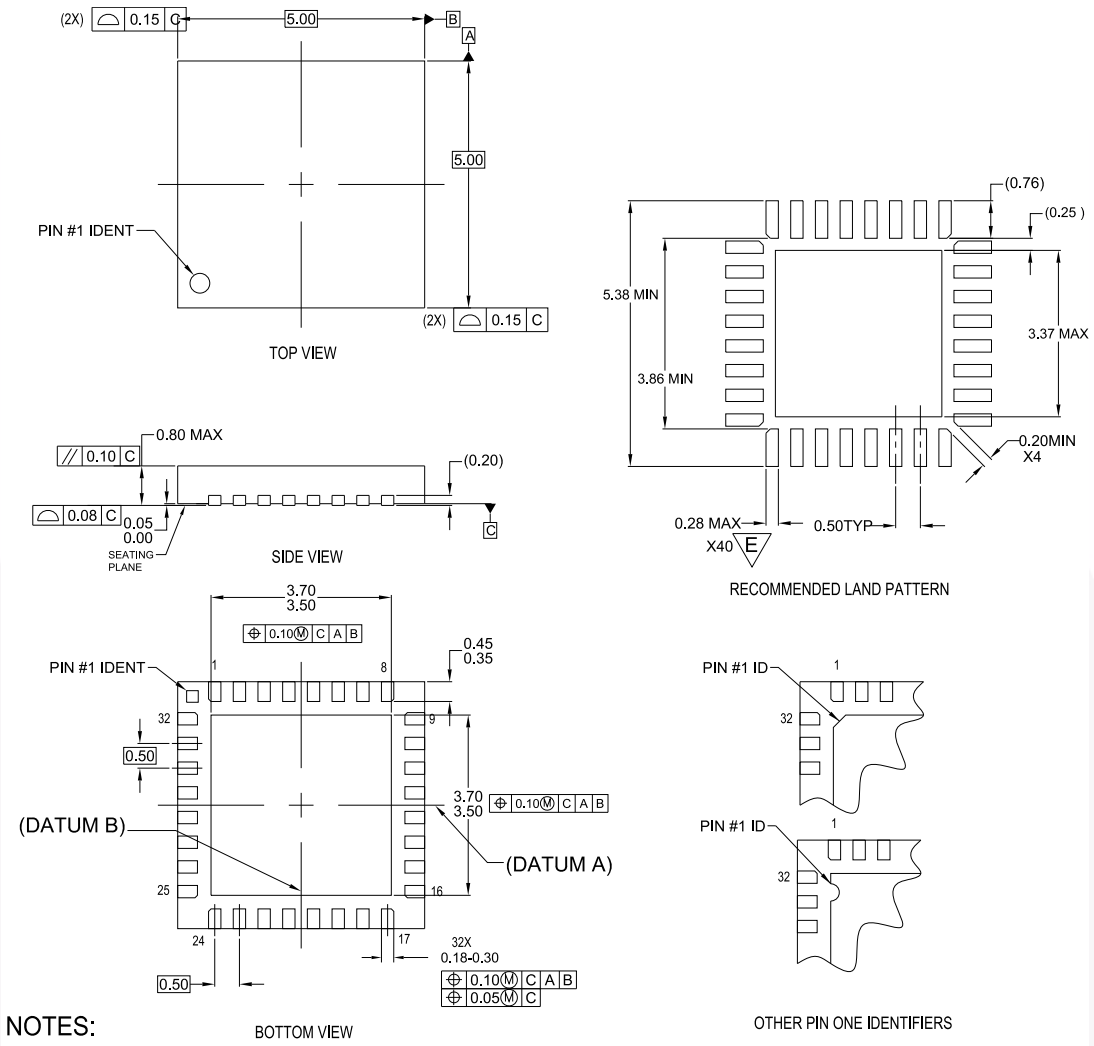
Figure 22. 42-Ball, Ultra Small Scale Ball Grid Array (USS-BGA), JEDEC MO-195, 3.5mm Wide

Note: Click here for tape and reel specifications, available at:
http://www.fairchildsemi.com/products/analog/packaging/bga42.html.

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
http://www.fairchildsemi.com/packaging/

Physical Dimensions (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-220, VARIATION WHHD-4
THIS PACKAGE IS ALSO FOOTPRINT COMPATIBLE WITH WHHD-5

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994

D. LAND PATTERN PER IPC SM-782 FABRICATION AND ASSEMBLY TOLERANCES OF 0.1 MM APPLIED

E. WIDTH REDUCED TO AVOID SOLDER BRIDGING.

G. DIMENSIONS ARE NOT INCLUSIVE OF BURRS,
MOLD FLASH, NOR TIE BAR PROTRUSIONS.

MLP032ArevB

Figure 23. 32-Terminal, Molded Leadless Package (MLP), Quad, JEDEC MO-220, 5mm Square

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
http://www.fairchildsemi.com/packaging/

FAIRCHILD SEMICONDUCTOR®

TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

ACEx®
Build it Now™
CorePLUS™
CorePOWER™
CROSSVOLT™
CTL™
Current Transfer Logic™
EcoSPARK®
EfficentMax™
EZSWITCH™ *
™
®
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FlashWriter®*
FPS™
F-PFS™
FRFET®
Global Power Resource℠
Green FPS™
Green FPS™ e-Series™
GTO™
IntelliMAX™
ISOPLANAR™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MillerDrive™
MotionMax™
Motion-SPM™
OPTOLOGIC®
OPTOPLANAR®
®
PDP SPM™
Power-SPM™
PowerTrench®
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™
Saving our world, 1mW at a time™
SmartMax™
SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS™
SyncFET™
SYSTEM ® GENERAL
The Power Franchise®
the power franchise
TinyBoost™
TinyBuck™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
µSerDes™
SerDes
UHC®
Ultra FRFET™
UniFET™
VCX™
VisualMax™

* EZSWITCH™ and FlashWriter® are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	This datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I34