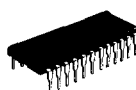
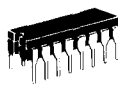
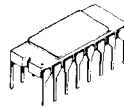


MC10,100/10,200 Series (-30 to +85°C)

MC10,500/10,600 Series (-55 to +125°C)

MECL 10,000 has an excellent speed-power product, has relatively slow rise and fall times, and transmission-line drive capability. The combination of versatile logic functions and the 2.0 ns propagation delay make MECL 10,000 a versatile family for data handling and processing systems.

Circuit design with MECL 10,000 is unusually convenient. The differential amplifier input and emitter-follower output permit high fanout, the wired-OR option, and complementary outputs. MECL III is directly compatible with MECL 10,000, and can be used to extend the speed capability of the MECL 10,000 series.

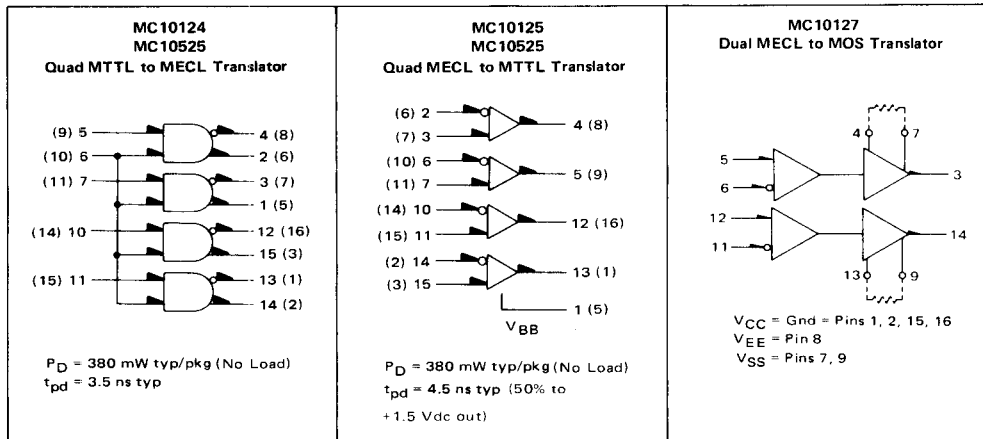
L SUFFIX
CERAMIC PACKAGE
CASE 623P SUFFIX
PLASTIC PACKAGE
CASE 648F SUFFIX
CERAMIC PACKAGE
CASE 650P SUFFIX
PLASTIC PACKAGE
CASE 649L SUFFIX
CERAMIC PACKAGE
CASE 620AL SUFFIX
CERAMIC PACKAGE
CASE 690F SUFFIX
CERAMIC PACKAGE
CASE 692FUNCTIONS AND CHARACTERISTICS ($V_{CC} = 0$, $V_{EE} = -5.2$ V, $T_A = 25^\circ\text{C}$)

Function	Type ①		Propagation Delay ns typ	Power Dissipation mW typ/pkg*	Case
	-30 to +85°C	-55 to +125°C			
Quad 2-Input NOR Gate With Strobe	MC10100	—	2.0	100	620
Quad OR/NOR Gate	MC10101	MC10501	2.0	100	620,648,650
Quad 2-Input NOR Gate	MC10102	MC10502	2.0	100	620,648,650
Quad 2-Input OR Gate	MC10103	—	2.0	100	620
Quad 2-Input AND Gate	MC10104	MC10504	2.7	140	620,648,650
Triple 2-3-2-Input OR/NOR Gate	MC10105	MC10505	2.0	90	620,648,650
Triple 4-3-3-Input NOR Gate	MC10106	MC10506	2.0	90	620,648,650
Triple 2-Input Exclusive OR/Exclusive NOR	MC10107	MC10507	2.5	110	620,648,650
Dual 4-5-Input OR/NOR Gate	MC10109	MC10509	2.0	60	620,648,650
Dual 3-Input 3-Output OR Gate	MC10110	—	2.4	160	620,648
Dual 3-Input 3-Output NOR Gate	MC10111	—	2.4	160	620,648
Quad Exclusive OR Gate	MC10113	—	2.5	175	620
Triple Line Receiver	MC10114	MC10514	2.4	145	620,648,650
Quad Line Receiver	MC10115	MC10515	2.0	110	620,648,650
Triple Line Receiver	MC10116	MC10516	2.0	85	620,648,650
Dual 2-Wide 2-3-Input OR-AND/OR-AND-INVERT Gate	MC10117	MC10517	2.3	100	620,648,650
Dual 2-Wide 3-Input OR-AND Gate	MC10118	MC10518	2.3	100	620,648,650
4-Wide 4-3-3-Input OR-AND Gate	MC10119	MC10519	2.3	100	620,648,650
4-Wide OR-AND/OR-AND-INVERT Gate	MC10121	MC10521	2.3	100	620,648,650
Triple 4-3-3-Input Bus Driver	MC10123	—	3.0	310	620
Quad MTTL to MECL Translator	MC10124	MC10524	3.5	380	620,648,650
Quad MECL to MTTL Translator	MC10125	MC10525	4.5	380	620,648,650
Dual MECL to MOS Translator	MC10127	—	—	—	620
Bus Driver	MC10128	—	12.0	700	620
Quad Bus Receiver	MC10129	—	10.0	750	620
Dual Latch	MC10130	MC10530	2.5	155	620,648,650
Dual Type D Master-Slave Flip-Flop	MC10131	MC10531	$f = 160$ MHz	235	620,648,650
Dual Multiplexer With Latch and Common Reset	MC10132	—	3.0	225	620,648
Quad Latch	MC10133	MC10533	4.0	310	620,648,650
Multiplexer with Latch	MC10134	—	3.0	225	620,648
Dual J-K Master-Slave Flip-Flop	MC10135	MC10535	$f = 140$ MHz	280	620,648,650
Universal Hexadecimal Counter	MC10136	MC10536	$f = 150$ MHz	625	620,650

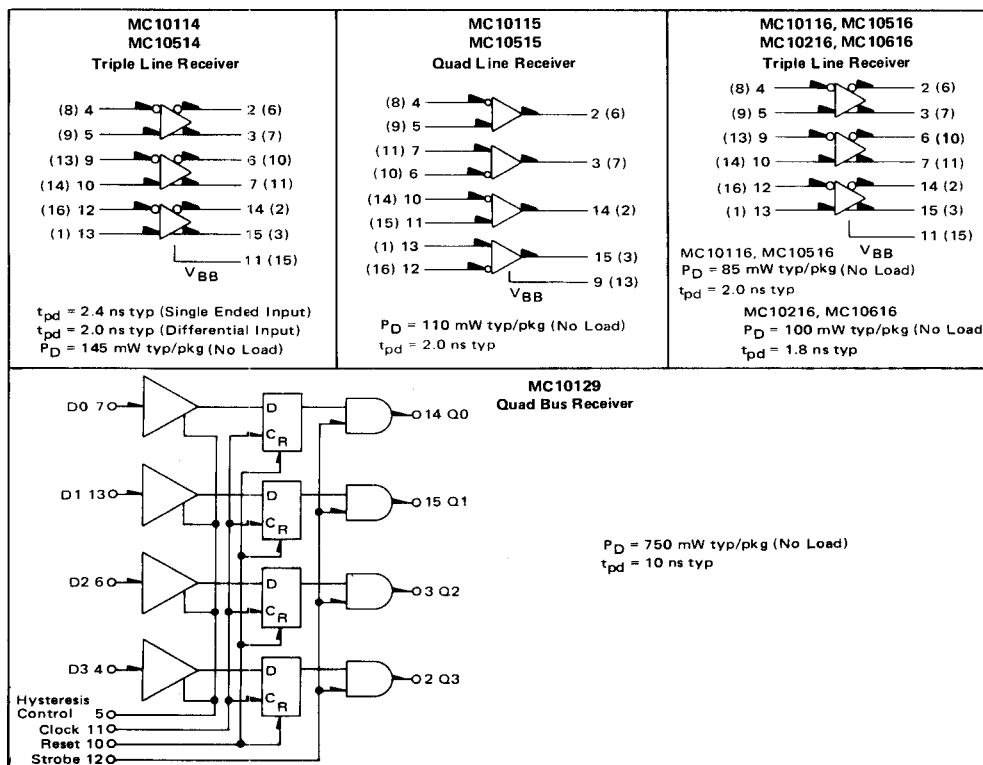
① L suffix denotes Dual In-Line Ceramic Package, P suffix denotes Dual In-Line Plastic Package, F suffix denotes flat package (i.e., MC10100L = Ceramic Dual In-Line Package, MC10100P = Plastic Dual In-Line Package and MC10500F = Ceramic Flat Package.)

*External Load Power not included.

TRANSLATORS



RECEIVERS



MC10129

The MC10129 bus receiver works in conjunction with the MC10128 to allow interfacing of MECL 10,000 to other forms of logic and logic buses. The data inputs are compatible with, and accept MTTL logic levels as well as levels compatible with IBM-type buses. The clock, strobe, and reset inputs accept MECL 10,000 logic levels.

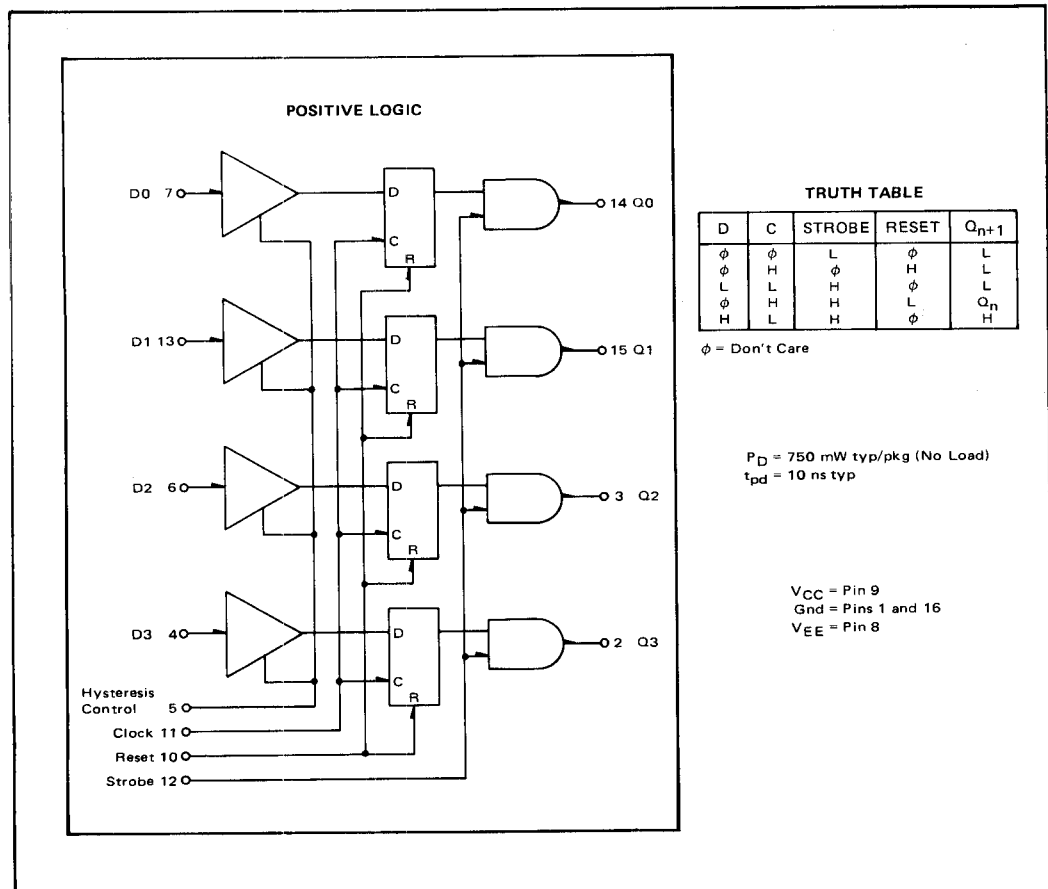
The data inputs accept the bus levels, and storage elements are provided to yield temporary latch storage of the information after receiving it from the bus. The outputs can be strobed to allow accurate synchronization of signals and/or connection to MECL 10,000 level buses. When the clock is low, the outputs will follow the D inputs, and the reset input is disabled. The latches will store the data on the rising edge of the clock. The outputs are enabled when the strobe input is high. Unused D

inputs must be tied to VCC or Gnd. The clock, strobe, and reset inputs each have 50 k ohm pulldown resistors to VEE. They may be left floating, if not used.

The MC10129 will operate in either of two modes. The first mode is obtained by tying the hysteresis control input to VEE. In this mode, the input threshold points of the D inputs are fixed. The second mode is obtained by tying the hysteresis control input to ground. In this mode, input hysteresis is achieved as shown in the test table. This hysteresis is desirable where extra noise margin is required on the D inputs. The other input pins are unaffected by the mode of operation used.

The MC10129 is especially useful in interface applications for central processors, mini-computers, and peripheral equipment.

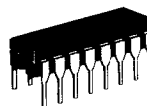
3



See General Information section for packaging and maximum ratings information.



Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input/output combination. Other combinations are tested in the same manner.



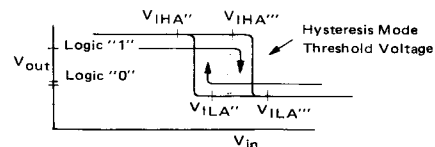
**L SUFFIX
CERAMIC PACKAGE
CASE 620**

[illegible]

*When testing choose either MTTL or IBM Input Levels

- ① Operation and limits shown also apply for $V_{CC} = +5.0\text{ V}$
- ② Input level on data input taken from $+0.4\text{ V}$ up to voltage level given.
- ③ Input level on data input taken from $+4.0\text{ V}$ down to voltage level given.
- ④ Output latched to logic high state prior to test.

V_{IH}^* , V_{IL}^* are standard logic "1" and logic "0" MTTL threshold voltages
 V_{IH}^{**} , V_{IL}^{**} , V_{IH}^{***} and V_{IL}^{***} are logic "1" and logic "0" threshold voltages in the hysteresis mode
as shown in diagram



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

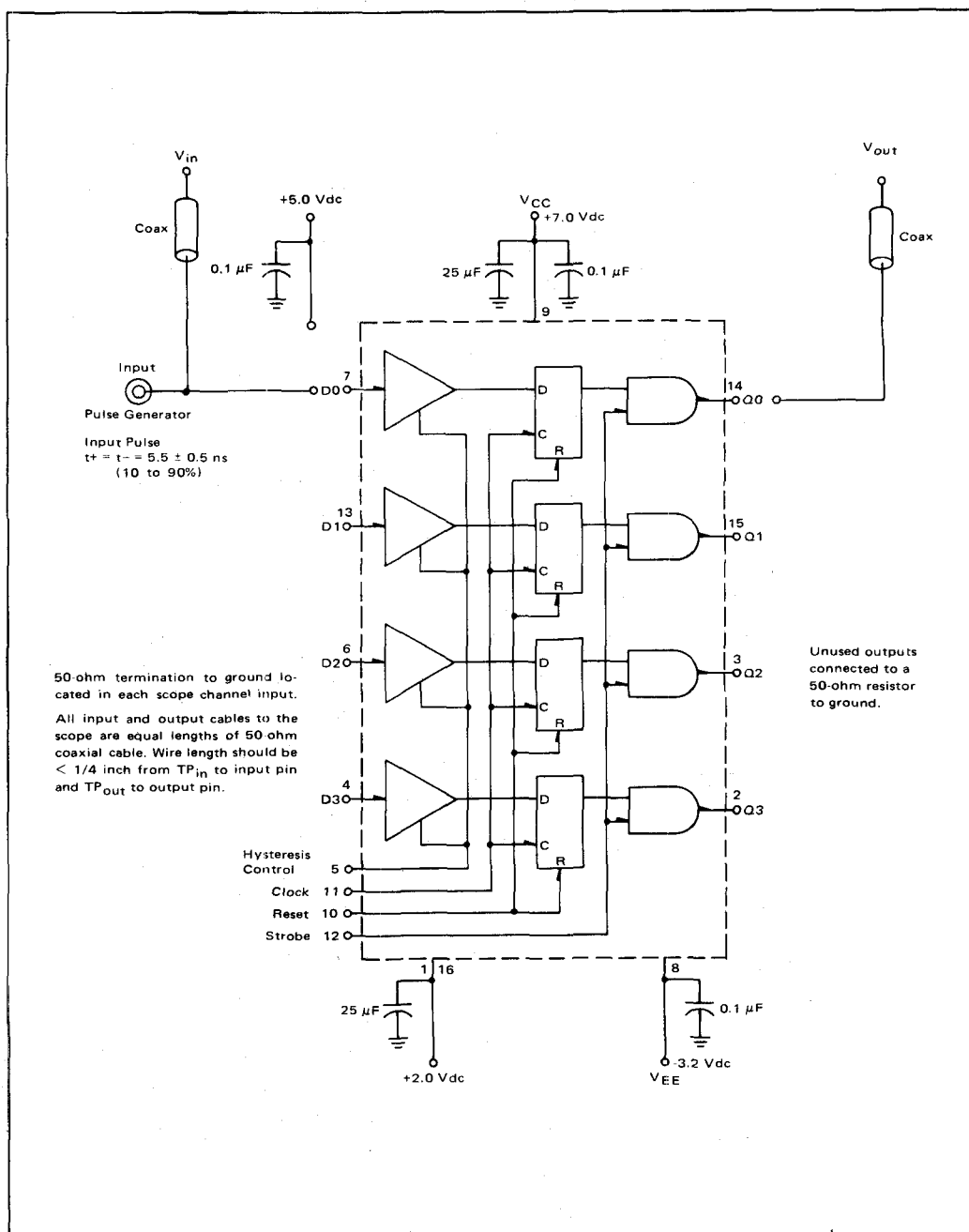


FIGURE 1 – DATA to OUTPUT
(Clock and Reset are low, Strobe is high)

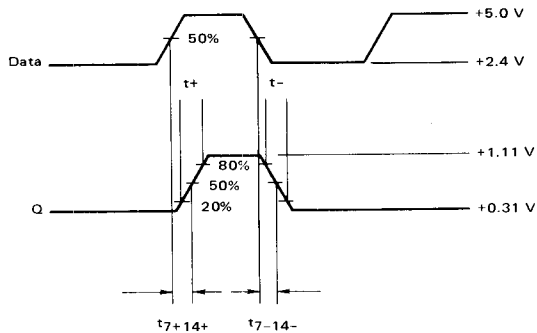


FIGURE 2 – STROBE to OUTPUT
(Data is high, Clock and Reset are low)

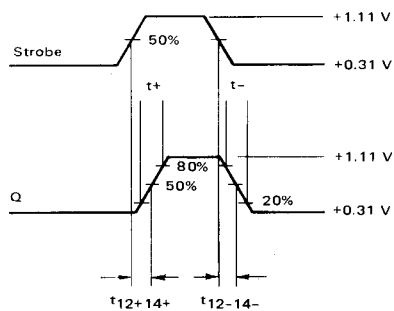


FIGURE 4 – CLOCK to OUTPUT
(Reset is low, Strobe is high)

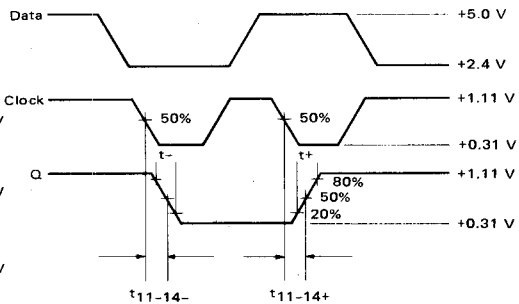


FIGURE 3 – RESET to OUTPUT
(Data and Strobe are high)

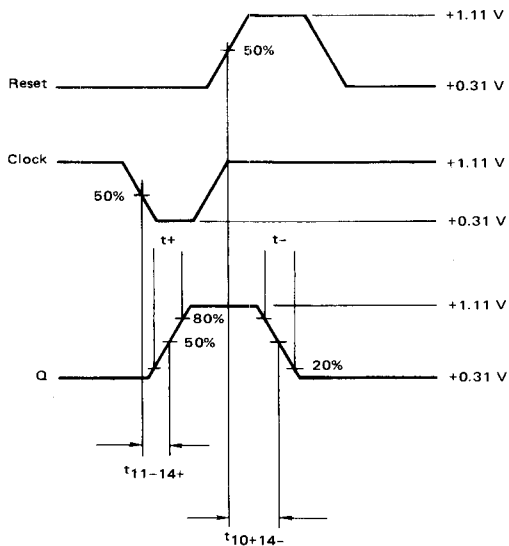


FIGURE 5 – TSET UP AND THOLD WAVEFORMS

