

# **TC74LVX374F,TC74LVX374FT**

## **Octal D-Type Flip-Flop with 3-State Output**

The TC74LVX374F/FT is a high-speed CMOS octal D-flip flop fabricated with silicon gate CMOS technology. Designed for use in 3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

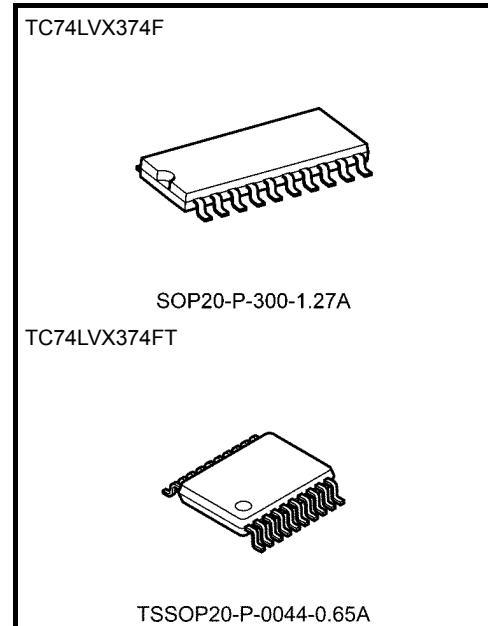
This device is suitable for low-voltage and battery operated systems.

This 8-bit D-type flip-flop is controlled by a clock input (CK) and an output enable input ( $\overline{OE}$ ). When the  $\overline{OE}$  input is high, the eight outputs are in a high-impedance state.

An input protection circuit ensures that 0 to 5.5V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

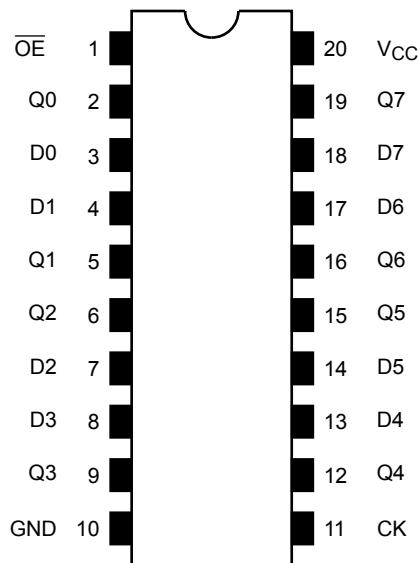
## **Features**

- High-speed:  $f_{max} = 160$  MHz (typ.) ( $V_{CC} = 3.3$  V)
- Low power dissipation:  $I_{CC} = 4$   $\mu$ A (max) ( $T_a = 25^\circ C$ )
- Input voltage level:  $V_{IL} = 0.8$  V (max) ( $V_{CC} = 3$  V)  
 $V_{IH} = 2.0$  V (min) ( $V_{CC} = 3$  V)
- Power-down protection is provided on all inputs
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Low noise:  $V_{OLP} = 0.8$  V (max)
- Pin and function compatible with 74HC374

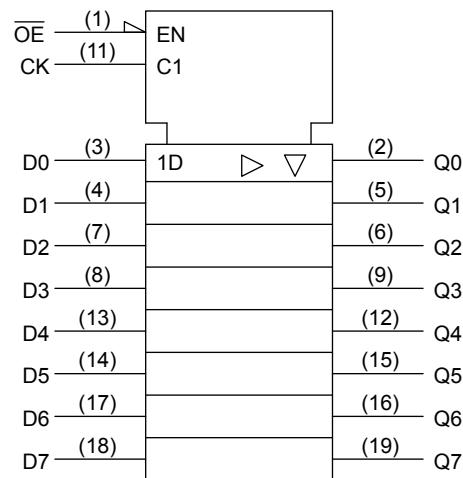


Weight  
SOP20-P-300-1.27A : 0.22 g (typ.)  
TSSOP20-P-0044-0.65A : 0.08 g (typ.)

## Pin Assignment (top view)



## IEC Logic Symbol



## Truth Table

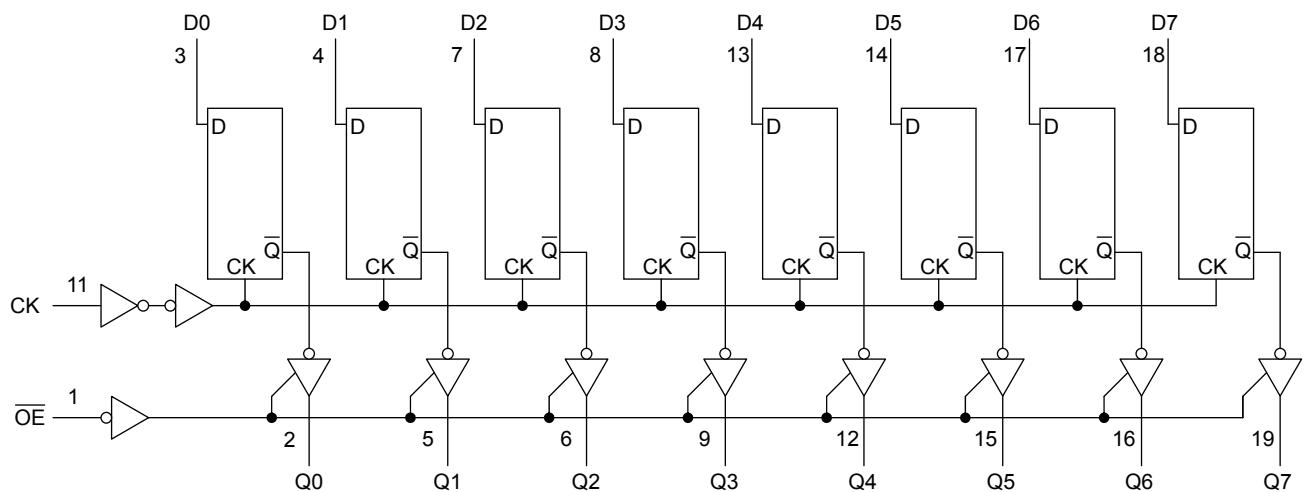
Inputs			Outputs
OE	CK	D	
H	X	X	Z
L	↓	X	Qn
L	↑	L	L
L	↑	H	H

X: Don't care

Z: High impedance

Qn: No change

## System Diagram



**Absolute Maximum Ratings (Note)**

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	–0.5 to 7.0	V
DC input voltage	$V_{IN}$	–0.5 to 7.0	V
DC output voltage	$V_{OUT}$	–0.5 to $V_{CC}$ + 0.5	V
Input diode current	$I_{IK}$	–20	mA
Output diode current	$I_{OK}$	±20	mA
DC output current	$I_{OUT}$	±25	mA
DC $V_{CC}$ /ground current	$I_{CC}$	±75	mA
Power dissipation	$P_D$	180	mW
Storage temperature	$T_{STG}$	–65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

**Operating Ranges (Note)**

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	2.0 to 3.6	V
Input voltage	$V_{IN}$	0 to 5.5	V
Output voltage	$V_{OUT}$	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	–40 to 85	°C
Input rise and fall time	$dt/dv$	0 to 100	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.

Unused inputs must be tied to either VCC or GND.

## Electrical Characteristics

## DC Characteristics

Characteristics		Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit	
				V <sub>CC</sub> (V)	Min	Typ.	Max	Min		
Input voltage	H-level	V <sub>IH</sub>	—	2.0	1.5	—	—	1.5	—	V
				3.0	2.0	—	—	2.0	—	
				3.6	2.4	—	—	2.4	—	
	L-level	V <sub>IL</sub>	—	2.0	—	—	0.5	—	0.5	
				3.0	—	—	0.8	—	0.8	
				3.6	—	—	0.8	—	0.8	
Output voltage	H-level	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50 µA	2.0	1.9	2.0	—	1.9	V
				I <sub>OH</sub> = -50 µA	3.0	2.9	3.0	—	2.9	
				I <sub>OH</sub> = -4 mA	3.0	2.58	—	—	2.48	
	L-level	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 µA	2.0	—	0	0.1	—	
				I <sub>OL</sub> = 50 µA	3.0	—	0	0.1	—	
				I <sub>OL</sub> = 4 mA	3.0	—	—	0.36	—	
3-state output Off-state current	I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND	3.6	—	—	—	±0.25	—	±2.5	µA
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = 5.5 V or GND	3.6	—	—	—	±0.1	—	±1.0	µA
Quiescent supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	3.6	—	—	—	4.0	—	40.0	µA

Timing Requirements (input: t<sub>r</sub> = t<sub>f</sub> = 3 ns)

Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = -40 to 85°C		Unit
			V <sub>CC</sub> (V)	Limit	Limit	Limit	
Minimum pulse width (CK)	t <sub>W</sub> (H) t <sub>W</sub> (L)	—	2.7	7.5	8.0	8.0	ns
			3.3 ± 0.3	5.0	5.5	5.5	
Minimum set-up time	t <sub>s</sub>	—	2.7	6.5	6.5	6.5	ns
			3.3 ± 0.3	4.5	4.5	4.5	
Minimum hold time	t <sub>h</sub>	—	2.7	2.0	2.0	2.0	ns
			3.3 ± 0.3	2.0	2.0	2.0	

AC Characteristics (input:  $t_r = t_f = 3$  ns)

Characteristics	Symbol	Test Condition	$T_a = 25^\circ\text{C}$			$T_a = -40$ to $85^\circ\text{C}$		Unit		
			$V_{CC}$ (V)	$C_L$ (pF)	Min	Typ.	Max			
Propagation delay time (CK-Q)	$t_{pLH}$	—	2.7	15	—	8.5	16.3	1.0	19.5	
				50	—	11.0	19.8	1.0	23.0	
	$t_{pHL}$		$3.3 \pm 0.3$	15	—	6.7	10.6	1.0	12.5	
				50	—	9.2	14.1	1.0	16.0	
Output enable time	$t_{pZL}$	$R_L = 1\text{ k}\Omega$	2.7	15	—	7.6	14.5	1.0	17.5	
				50	—	10.1	18.0	1.0	21.0	
	$t_{pZH}$		$3.3 \pm 0.3$	15	—	5.9	9.3	1.0	11.0	
				50	—	8.4	12.8	1.0	14.5	
Output disable time	$t_{pLZ}$	$R_L = 1\text{ k}\Omega$	2.7	50	—	11.5	18.5	1.0	22.0	
	$t_{pHZ}$		$3.3 \pm 0.3$	50	—	9.6	13.2	1.0	15.0	
Maximum clock frequency	$f_{max}$	—	2.7	15	60	115	—	50	—	
				50	45	60	—	40	—	
			$3.3 \pm 0.3$	15	100	160	—	85	—	
				50	60	95	—	55	—	
Output to output skew	$t_{osLH}$	(Note 1)	2.7	50	—	—	1.5	—	1.5	
	$t_{osHL}$		$3.3 \pm 0.3$	50	—	—	1.5	—	1.5	
Input capacitance	$C_{IN}$	(Note 2)			—	4	10	—	10	
Output capacitance	$C_{OUT}$	—			—	6	—	—	—	
Power dissipation capacitance	$C_{PD}$	(Note 3)			—	32	—	—	—	

Note 1: Parameter guaranteed by design.

 $(tosLH = |t_{pLHm} - t_{pLHn}|, tosHL = |t_{pHLm} - t_{pHLn}|)$ 

Note 2: Parameter guaranteed by design.

Note 3:  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per F/F)}$$

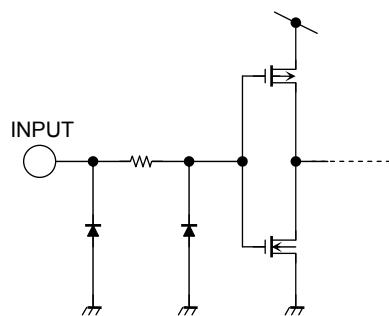
And the total  $C_{PD}$  when  $n$  pcs. of Flip Flop operate can be gained by the following equation:

$$C_{PD}(\text{total}) = 20 + 12 \cdot n$$

Noise Characteristics (Ta = 25°C, input:  $t_r = t_f = 3$  ns,  $C_L = 50$  pF)

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Typ.	Limit	Unit
Quiet output maximum dynamic V <sub>OL</sub>	V <sub>OLP</sub>	—	3.3	0.5	0.8	V
Quiet output minimum dynamic V <sub>OL</sub>	V <sub>OLV</sub>	—	3.3	-0.5	-0.8	V
Minimum high level dynamic input voltage V <sub>IHD</sub>	V <sub>IHD</sub>	—	3.3	—	2.0	V
Maximum low level dynamic input voltage V <sub>ILD</sub>	V <sub>ILD</sub>	—	3.3	—	0.8	V

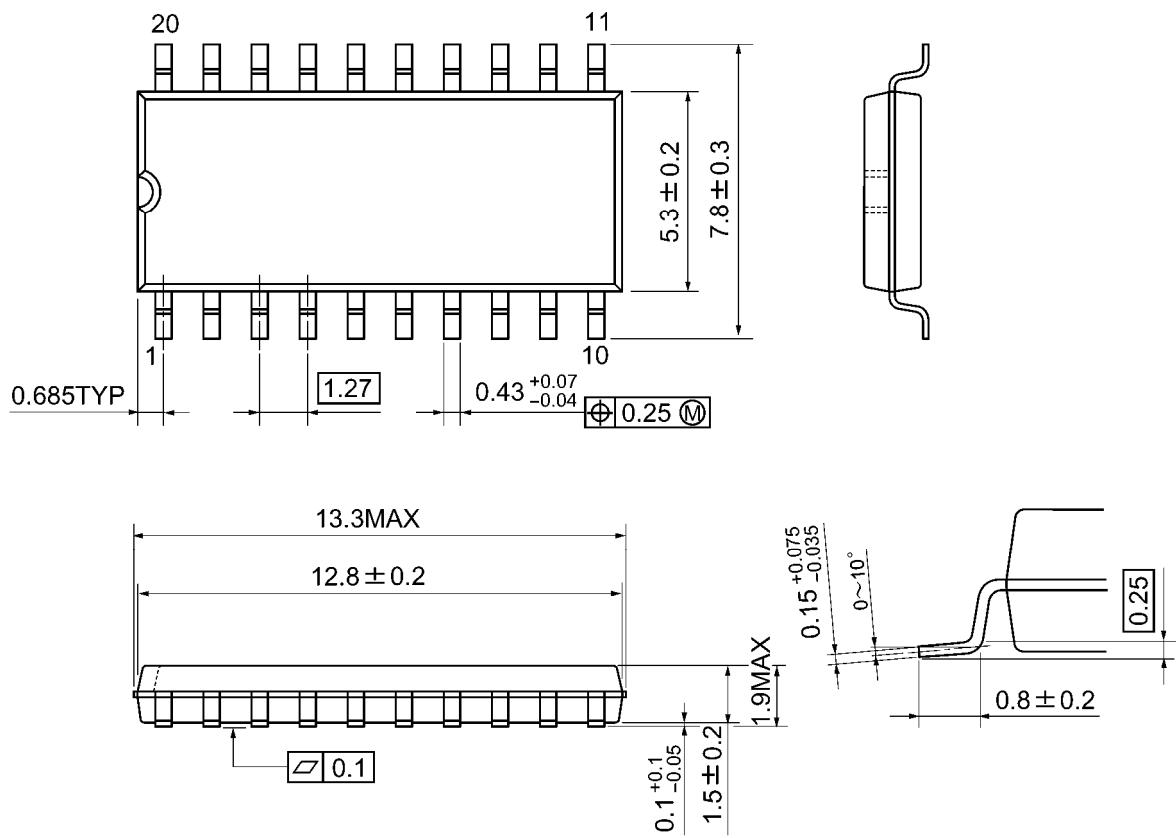
## Input Equivalent Circuit



**Package Dimensions**

SOP20-P-300-1.27A

Unit: mm

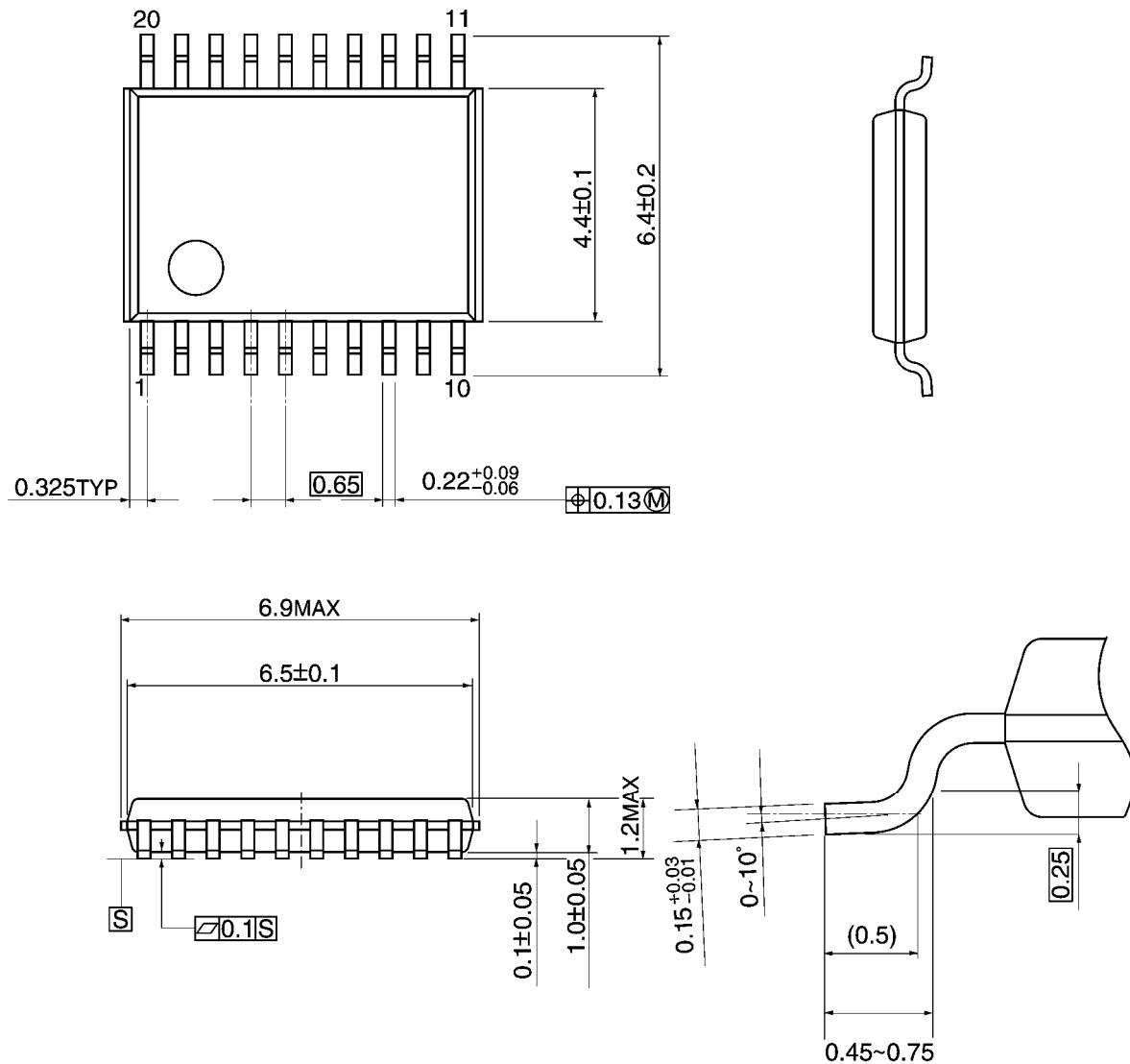


Weight: 0.22 g (typ.)

## Package Dimensions

TSSOP20-P-0044-0.65A

Unit: mm



Weight: 0.08 g (typ.)

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