

# FDT86246

## N-Channel Power Trench® MOSFET

150 V, 2 A, 236 mΩ

### Features

- Max  $r_{DS(on)}$  = 236 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 2\text{ A}$
- Max  $r_{DS(on)}$  = 329 mΩ at  $V_{GS} = 6\text{ V}$ ,  $I_D = 1.7\text{ A}$
- High performance trench technology for extremely low  $r_{DS(on)}$
- High power and current handling capability in a widely used surface mount package
- Fast switching speed
- 100% UIL Tested
- RoHS Compliant

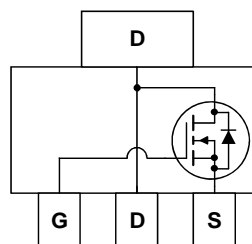
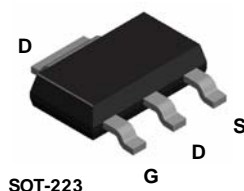


### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process that has been optimized for  $r_{DS(on)}$ , switching performance and ruggedness.

### Applications

- Load Switch
- Primary Switch



### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	150	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current -Continuous (Note 1a)	2	A
	-Pulsed	8	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	8	mJ
$P_D$	Power Dissipation (Note 1a)	2.2	W
	Power Dissipation (Note 1b)	1.0	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	12	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	55	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
86246	FDT86246	SOT-223	13 "	12 mm	2500 units

**Electrical Characteristics**  $T_J = 25\text{ }^{\circ}\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	150			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^{\circ}\text{C}$		104		mV/ $^{\circ}\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 120\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 100$	nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$	2.0	3.1	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^{\circ}\text{C}$		-9		mV/ $^{\circ}\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 2\text{ A}$		194	236	m $\Omega$
		$V_{GS} = 6\text{ V}$ , $I_D = 1.7\text{ A}$		231	329	
		$V_{GS} = 10\text{ V}$ , $I_D = 2\text{ A}$ , $T_J = 125\text{ }^{\circ}\text{C}$		349	425	
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}$ , $I_D = 2\text{ A}$		5		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 75\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		161	215	pF
$C_{oss}$	Output Capacitance			21	30	pF
$C_{rss}$	Reverse Transfer Capacitance			1.6	5	pF
$R_g$	Gate Resistance			0.9		$\Omega$

**Switching Characteristics**

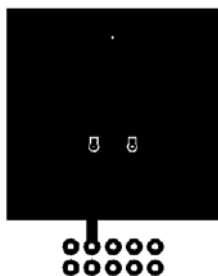
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 75\text{ V}$ , $I_D = 2\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		7.8	16	ns
$t_r$	Rise Time			2.3	10	ns
$t_{d(off)}$	Turn-Off Delay Time			4.6	10	ns
$t_f$	Fall Time			1.2	10	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\text{ V to }10\text{ V}$	$V_{DD} = 75\text{ V}$ , $I_D = 2\text{ A}$	2.9	4	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\text{ V to }5\text{ V}$		1.7	3	
$Q_{gs}$	Total Gate Charge			0.9		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			0.8		nC

**Drain-Source Diode Characteristics**

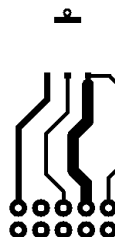
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 2\text{ A}$ (Note 2)		0.84	1.3	V
$t_{rr}$	Reverse Recovery Time	$I_F = 2\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		44	71	ns
$Q_{rr}$	Reverse Recovery Charge			31	49	nC

## NOTES:

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a) 55  $^{\circ}\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b) 118  $^{\circ}\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

3. Starting  $T_J = 25\text{ }^{\circ}\text{C}$ ; N-ch:  $L = 1.0\text{ mH}$ ,  $I_{AS} = 4.0\text{ A}$ ,  $V_{DD} = 135\text{ V}$ ,  $V_{GS} = 10\text{ V}$ .

# Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

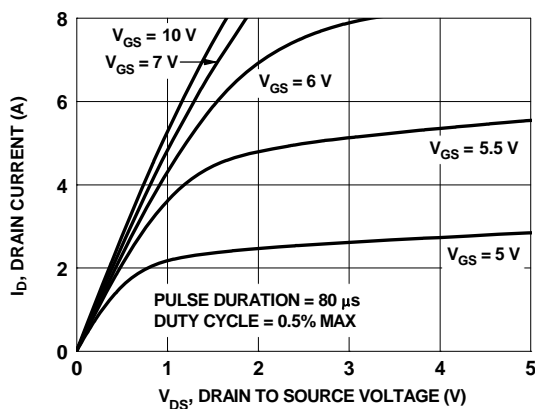


Figure 1. On-Region Characteristics

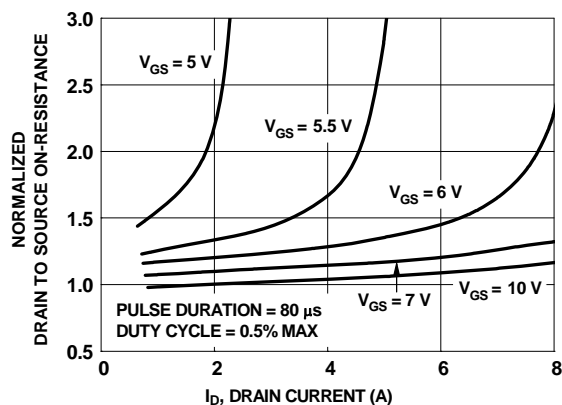


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

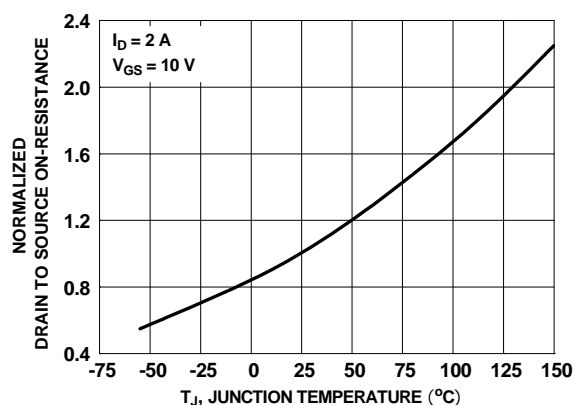


Figure 3. Normalized On-Resistance vs Junction Temperature

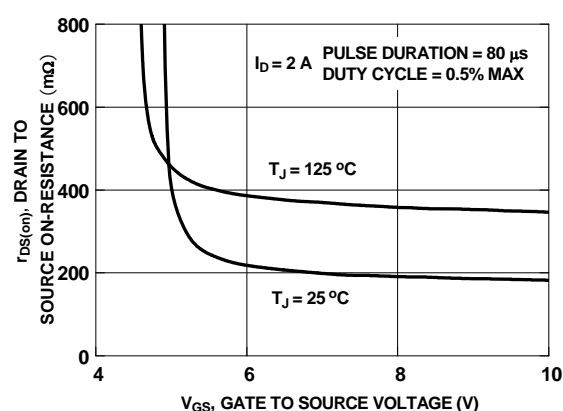


Figure 4. On-Resistance vs Gate to Source Voltage

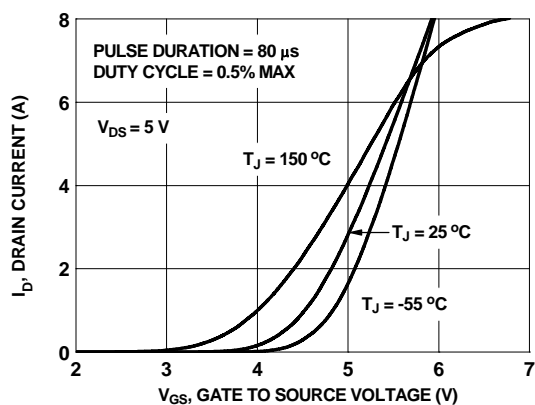


Figure 5. Transfer Characteristics

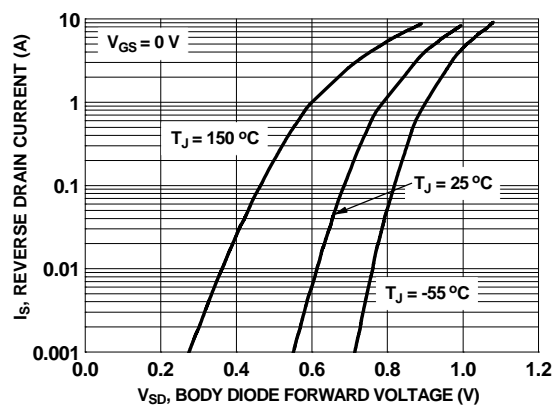
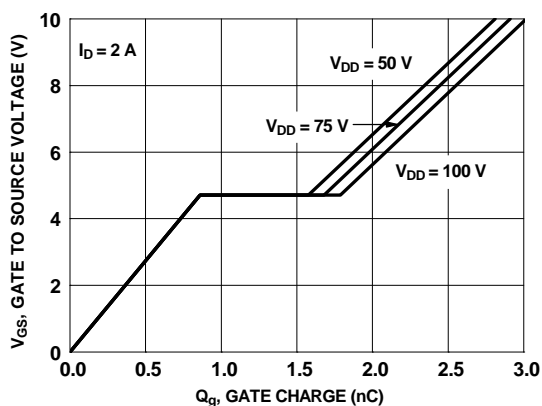
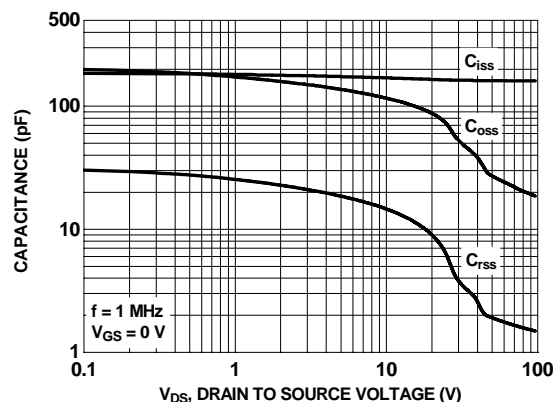


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

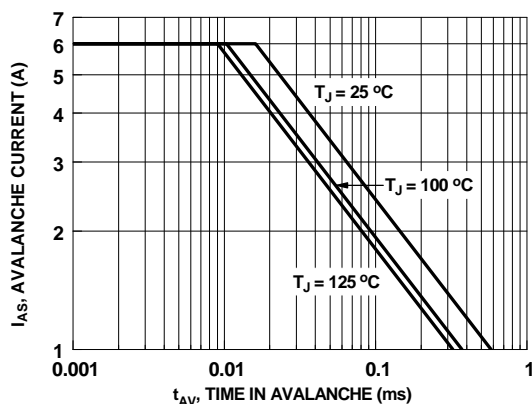
# **Typical Characteristics** $T_J = 25^\circ\text{C}$ unless otherwise noted



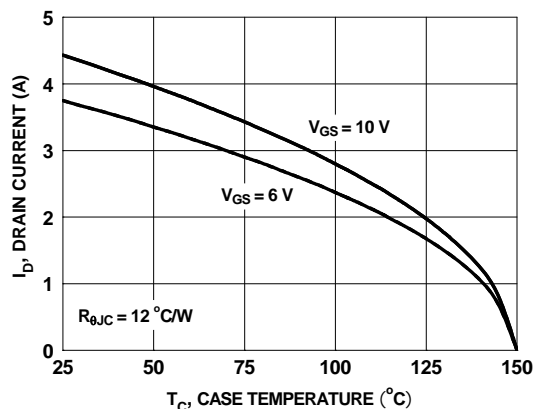
**Figure 7. Gate Charge Characteristics**



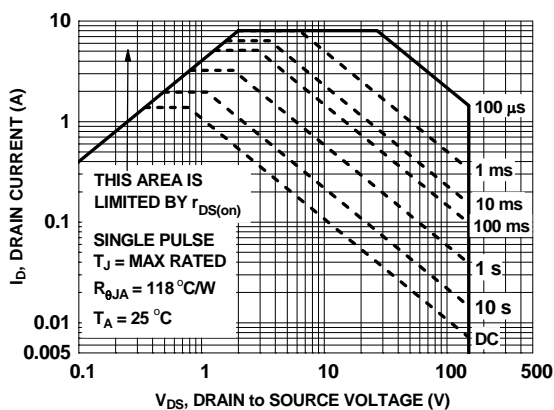
**Figure 8. Capacitance vs Drain to Source Voltage**



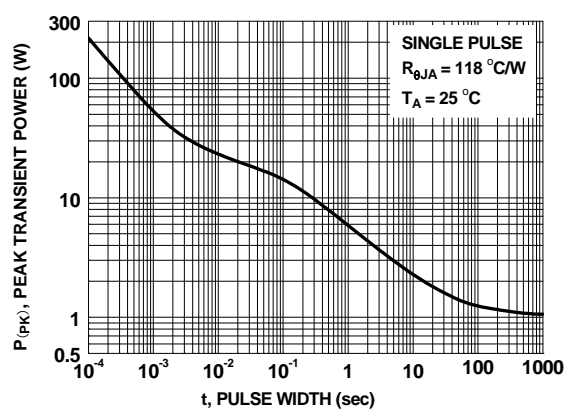
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

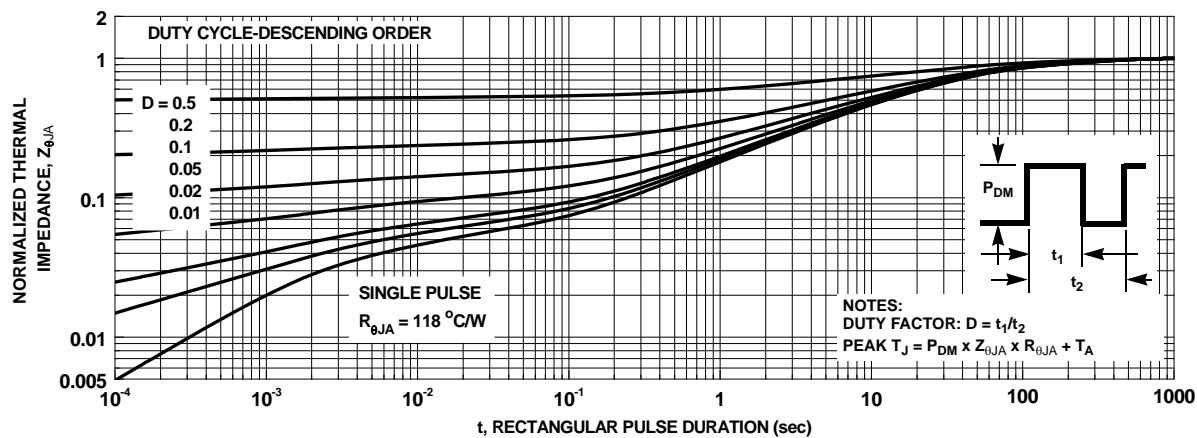


**Figure 11. Forward Bias Safe Operating Area**



**Figure 12. Single Pulse Maximum Power Dissipation**

# Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted



**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**

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