

Resonant Mode Power Supply Controller

FEATURES

- 3MHz VFO Linear over 100:1 Range
- 5MHz Error Amplifier with Controlled Output Swing
- Programmable One Shot Timer—Down to 100ns
- Precision 5V Reference
- Dual 2A Peak Totem Pole Outputs
- Programmable Output Sequence
- Programmable Under Voltage Lockout
- Very Low Start Up Current
- Programmable Fault Management & Restart Delay
- Uncommitted Comparator

DESCRIPTION

The UC1860 family of control ICs is a versatile system for resonant mode power supply control. This device easily implements frequency modulated fixed-on-time control schemes as well as a number of other power supply control schemes with its various dedicated and programmable features.

The UC1860 includes a precision voltage reference, a wide-bandwidth error amplifier, a variable frequency oscillator operable to beyond 3MHz, an oscillator-triggered one-shot, dual high-current totem-pole output drivers, and a programmable toggle flip-flop. The output mode is easily programmed for various sequences such as A, off, B, off; A & B, off; or A, B, off. The error amplifier contains precision output clamps that allow programming of minimum and maximum frequency.

The device also contains an uncommitted comparator, a fast comparator for fault sensing, programmable soft start circuitry, and a programmable restart delay. Hic-up style response to faults is easily achieved. In addition, the UC1860 contains programmable under voltage lockout circuitry that forces the output stages low and minimizes supply current during start-up conditions.

ABSOLUTE MAXIMUM RATINGS

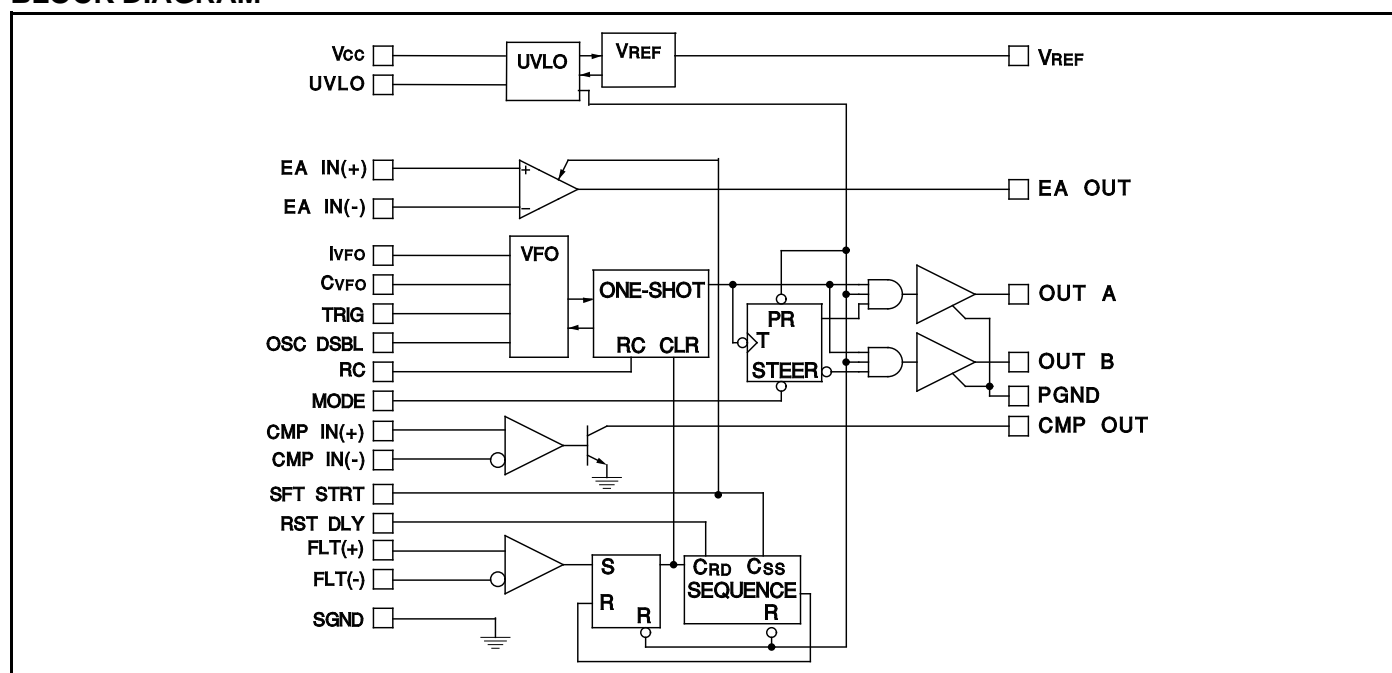
Supply Voltage (pin 19)	20V
Output Current, Source or Sink (pins 17 & 20)	
DC	0.8A
Pulse (0.5μs)	3.0A
Power Ground Voltage	±0.2V
Inputs (pins 1, 2, 3, 4, 8, 9, 11, 12, 13, 14, 21, 22, 23 & 24)	-0.4 to 6V
Error Amp Output Current, Source or Sink (pin 5)	2mA
IvFo Current (pin 7)	2mA
Comparator Output Current (pin 15)	5mA

Comparator Output Voltage (pin 15)	15V
Soft Start or Restart Delay Sink Current (pins 22 & 23)	5mA
Power Dissipation at TA = 50°C (DIP)	1.25W
Power Dissipation at TA = 50°C (PLCC)	1W
Lead Temperature (Soldering, 10 seconds)	300°C

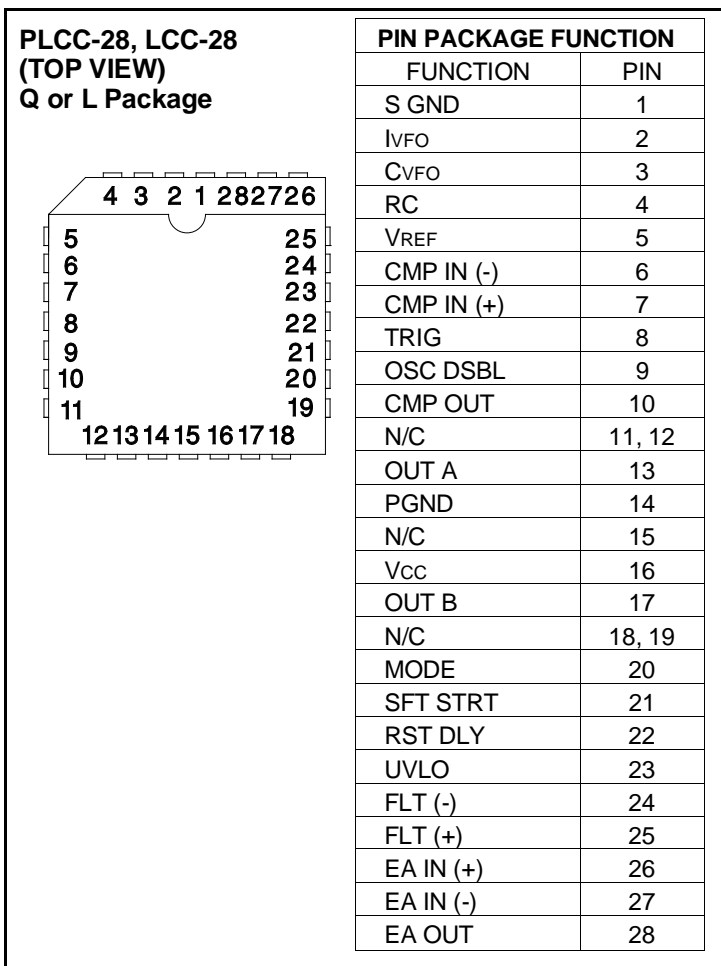
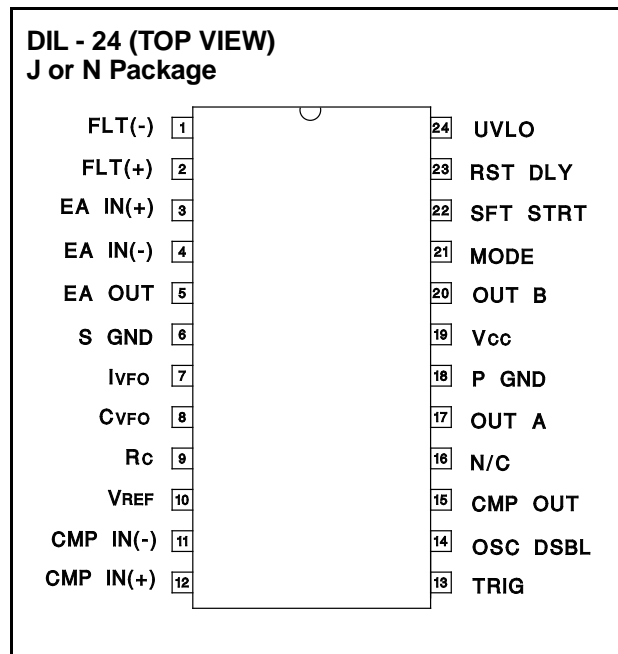
Note: All voltages are with respect to signal ground and all currents are positive into the specified terminal. Pin numbers refer to the DIP.

Refer to Packaging Section of Databook for thermal limitations and considerations of packages.

BLOCK DIAGRAM



CONNECTION DIAGRAM



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, all specifications apply for $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ for the UC1860, $-25^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ for the UC2860, $0 \leq T_A \leq 70^{\circ}\text{C}$ for the UC3860, $V_{CC} = 12\text{V}$, $C_{VFO} = 330\text{pF}$, $I_{VFO} = 0.5\text{mA}$, $C = 330\text{pF}$, and $R = 2.7\text{k}\Omega$, $T_A = T_J$.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
Output Voltage	$T_A = 25^{\circ}\text{C}$, $I_O = 0$	4.95	5.00	5.05	V
	$I_O = 0$, Over Temp	4.93		5.07	V
Line Regulation	$10 \leq V_{CC} \leq 20\text{V}$		2	15	mV
Load Regulation	$0 \leq I_O \leq 10\text{mA}$		2	25	mV
Output Noise Voltage*	$10\text{Hz} \leq f \leq 10\text{kHz}$		50		μVRMS
Short Circuit Current	$V_{REF} = 0\text{V}$	-150		-15	mA
Error Amplifier Section					
Input Offset Voltage	$2.8 \leq V_{CM} \leq 4.5\text{V}$		1	8	mV
Input Bias Current			50	500	nA
Open Loop Gain	$dV_O = 1.5\text{V}$	60	80		dB
PSRR	$10 \leq V_{CC} \leq 20\text{V}$	70	100		dB
Output Low ($V_O - V_{IVFO}$)	$-0.1 \leq I_O \leq 0.1\text{mA}$	-8	0	8	mV
Output High ($V_O - V_{IVFO}$)	$-0.5 \leq I_O \leq 0.5\text{mA}$	1.9	2	2.1	V
Unity Gain Bandwidth*	$R_{IN} = 2\text{k}\Omega$	4	5		MHz
Oscillator Section					
Nominal Frequency*		1.0	1.5	2.0	MHz
dF/dI_{osc} *	$100 \leq I_{VFO} \leq 500\mu\text{A}$	2	3	4	GHz/A

*Guaranteed by design but not 100% tested.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, all specifications apply for $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ for the UC1860, $-25^{\circ} \leq T_A \leq 85^{\circ}\text{C}$ for the UC2860, $0 \leq T_A \leq 70^{\circ}\text{C}$ for the UC3860, $V_{CC} = 12\text{V}$, $C_{VFO} = 330\text{pF}$, $I_{VFO} = 0.5\text{mA}$, $C = 330\text{pF}$, and $R = 2.7\text{k}$, $T_A = T_J$.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Section (cont'd)					
Trig in Threshold		1.0	1.4	1.8	V
Trig in Open Circuit Voltage		0.7	0.9	1.1	V
Trig in Delta ($V_{TH}-V_{OC}$)		0.3	0.5	0.7	V
Trig in Input Resistance	dV TRIG = V_{OC} to V_{TH}	5	12	25	k Ω
Minimum Trig in Pulse Width*			3	10	ns
Osc. Disable Threshold		1.0	1.4	1.8	V
One Shot Timer					
On Time*		150	200	250	ns
Clamp Frequency*	$I_{VFO} = 1.5\text{mA}$	2.8	3.7	4.6	MHz
Dead Time*	$I_{VFO} = 1.5\text{mA}$	35	70	100	ns
Output Stage					
Output Low Saturation	20mA		0.2	0.4	V
	200mA		0.5	2.2	V
Output High Saturation	-20mA		1.5	2.0	V
	-200mA		1.7	2.5	V
Rise/Fall Time*	$C_{LOAD} = 1\text{nF}$		15	30	ns
UVLO Low Saturation	20mA		0.8	1.5	V
Output Mode Low Input				0.4	V
Output Mode High Input		2.0			V
Under Voltage Lockout Section					
Vcc Comparator Threshold	On	16	17.3	18.5	V
	Off	9.5	10.5	12	V
UVLO Comparator Threshold	On	3.6	4.2	4.8	V
	Hysteresis	0.2	0.4	0.6	V
UVLO Input Resistance	$UVLO = 4/V_{CC} = 8$	10	23	50	k Ω
VREF Comparator Threshold	$V_{CC} = UVLO = V_{REF}$		4.5	4.9	V
Supply Current					
ICC	$V_{CC} = 12\text{V}$, $V_{OSC} \text{ DSBL} = 3\text{V}$		30	40	mA
ISTART	UVLO pin open $V_{CC} = V_{CC} \text{ (on)} - 0.3\text{V}$		0.3	0.5	mA
Fault Comparator					
Input Offset Voltage	$-0.3 \leq V_{CM} \leq 3\text{V}$		2	10	mV
Input Bias Current	$V_{CM} = 0\text{V}$		100	200	μA
Input Offset Current	$V_{CM} = 0\text{V}$		10	30	μA
Propagation Delay To Output*	$\pm 50\text{mV}$ input		100	150	ns
Uncommitted Comparator					
Input Offset Voltage	$-0.3 \leq V_{CM} \leq 3\text{V}$		2	10	mV
Input Bias Current	$V_{CM} = 0\text{V}$		100	200	μA
Input Offset Current	$V_{CM} = 0\text{V}$		10	30	μA
Output Low Voltage	$I_O = 2\text{mA}$		0.3	0.5	V
Propagation Delay To Sat*	$\pm 50\text{mV}$ input, 2.5k load to 5V		50	100	ns
Soft Start/Restart Control Section					
Saturation Voltage (2 pins)	$I_{SINK} = 100\mu\text{A}$		0.2	0.5	V
Charge Current (2 pins)		2	5	10	μA
Restart Delay Threshold		2.8	3.0	3.2	V

*Guaranteed by design but not 100% tested.

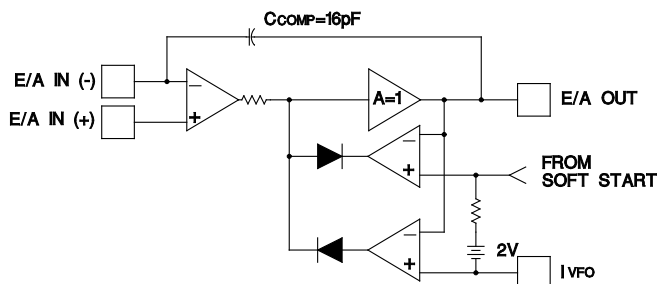
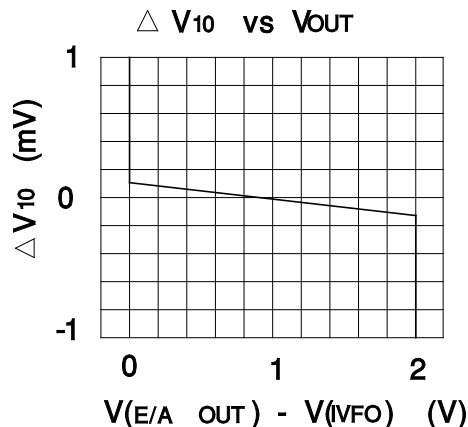
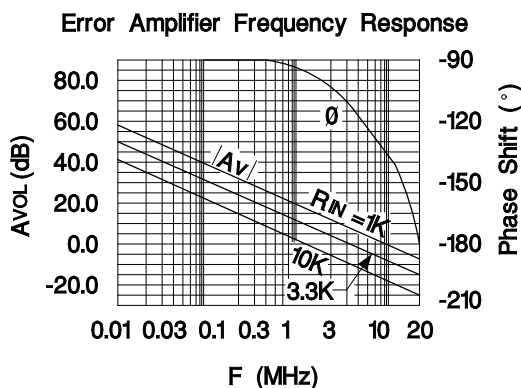
ERROR AMPLIFIER

The error amplifier is a high gain, low offset, high bandwidth design with precise limits on its output swing. The bandwidth of the amplifier is externally determined by the resistance seen at the inverting input. Unity gain bandwidth is approximately:

$$\text{Frequency (0dB)} = 1/(2\pi * R_{IN} * C_{COMP})$$

The input common mode range of the amplifier is from 2.8 to 4.5V. As long as one pin is within this range, the other can go as low as zero.

The output swing with respect to the V_{FO} pin is limited from zero to 2V. Note that pulling $Sft Strt$ (soft start) low will lower the reference of the upper clamp. The lower clamp, however, will dominate should the upper clamp reference drop below the lower reference.

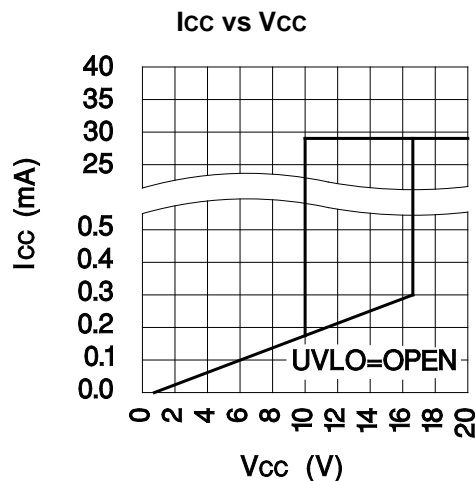
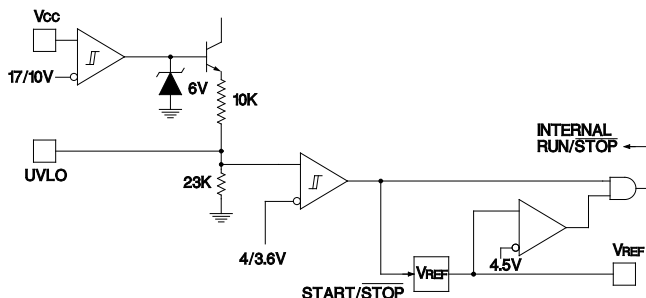


UNDER VOLTAGE LOCKOUT SECTION

The under voltage lockout consists of three comparators that monitor V_{CC} , $UVLO$ and V_{REF} . The V_{REF} comparator makes sure that the reference voltage is sufficiently high before operation begins. When the $UVLO$ comparator is low, the outputs are driven low, the fault latch is reset, the soft start pin is discharged, and the toggle flip-flop is loaded for output A.

The V_{CC} comparator is used for off-line applications by leaving the $UVLO$ pin open. In this application the supply current is typically less than 0.3mA during start-up.

The $UVLO$ comparator is used for DC to DC applications or to gate the chip on and off. To utilize its hysteretic threshold by an external resistive divider, the internal impedance of the pin must be accounted for. To run from a 5V external supply, $UVLO$, V_{CC} , and V_{REF} are tied together.



VARIABLE FREQUENCY OSCILLATOR

The VFO block is controlled through 4 pins: C_{VFO} , I_{VFO} , Osc Dsbl (oscillator disable), and Trig (trigger input). Oscillator frequency is approximately:

$$Frequency = I_{VFO} / (C_{VFO} * 1V)$$

With a fixed capacitor and low voltage applied to Trig and Osc Dsbl, frequency is linearly modulated by varying the current into the I_{VFO} pin.

The Trig and Osc Dsbl inputs are used to modify VFO operation. If Osc Dsbl is held high, the oscillator will complete the current cycle but wait until Osc Dsbl is returned low to initiate a new cycle. If a pulse is applied to Trig during a cycle, the oscillator will immediately initiate a new cycle. Osc Dsbl has priority over Trig, but if a trigger pulse is received while Osc Dsbl is high, the VFO will remember the trigger pulse and start a new cycle as soon as Osc Dsbl goes low.

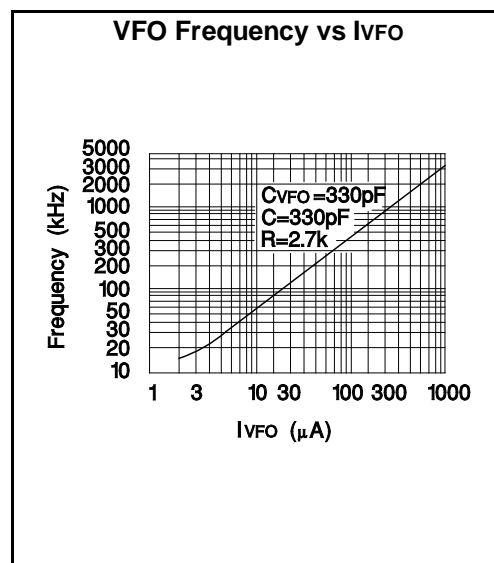
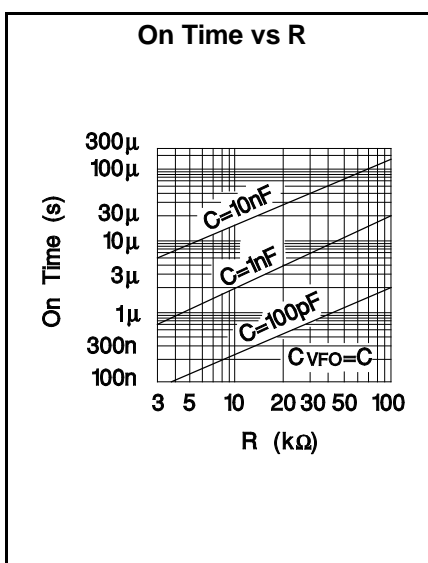
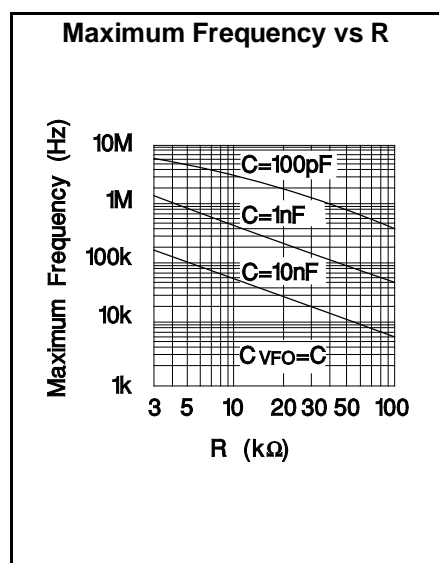
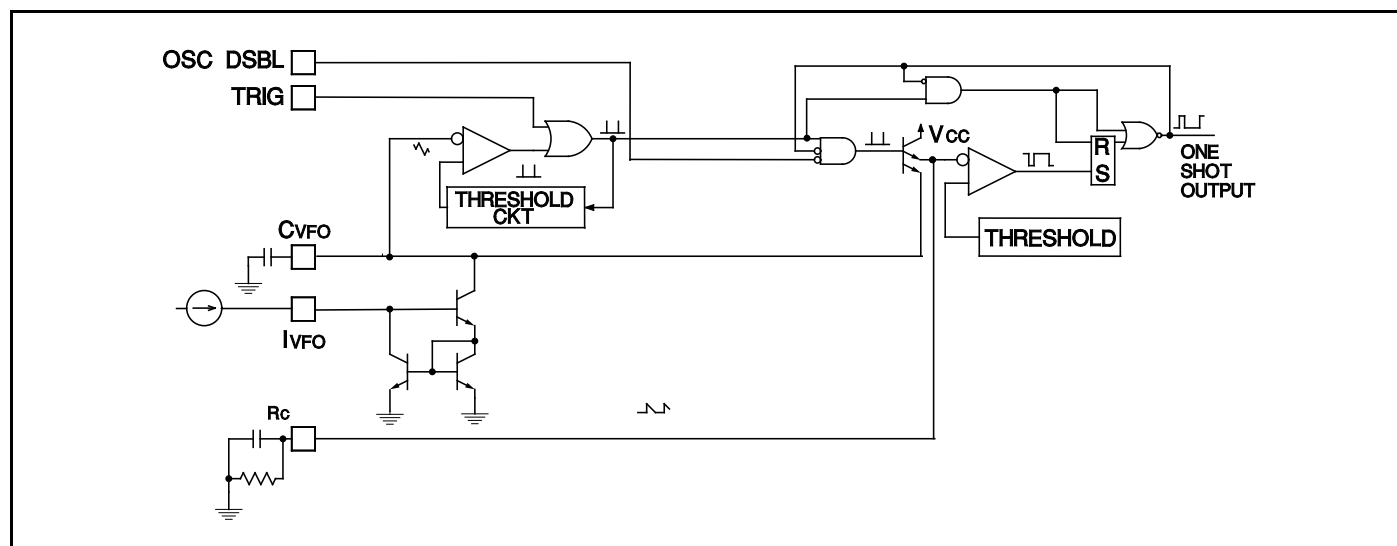
Normally low trigger pulses are used to synchronize the oscillator to a faster clock. Normally high trigger pulses can also be used to synchronize to a slower clock.

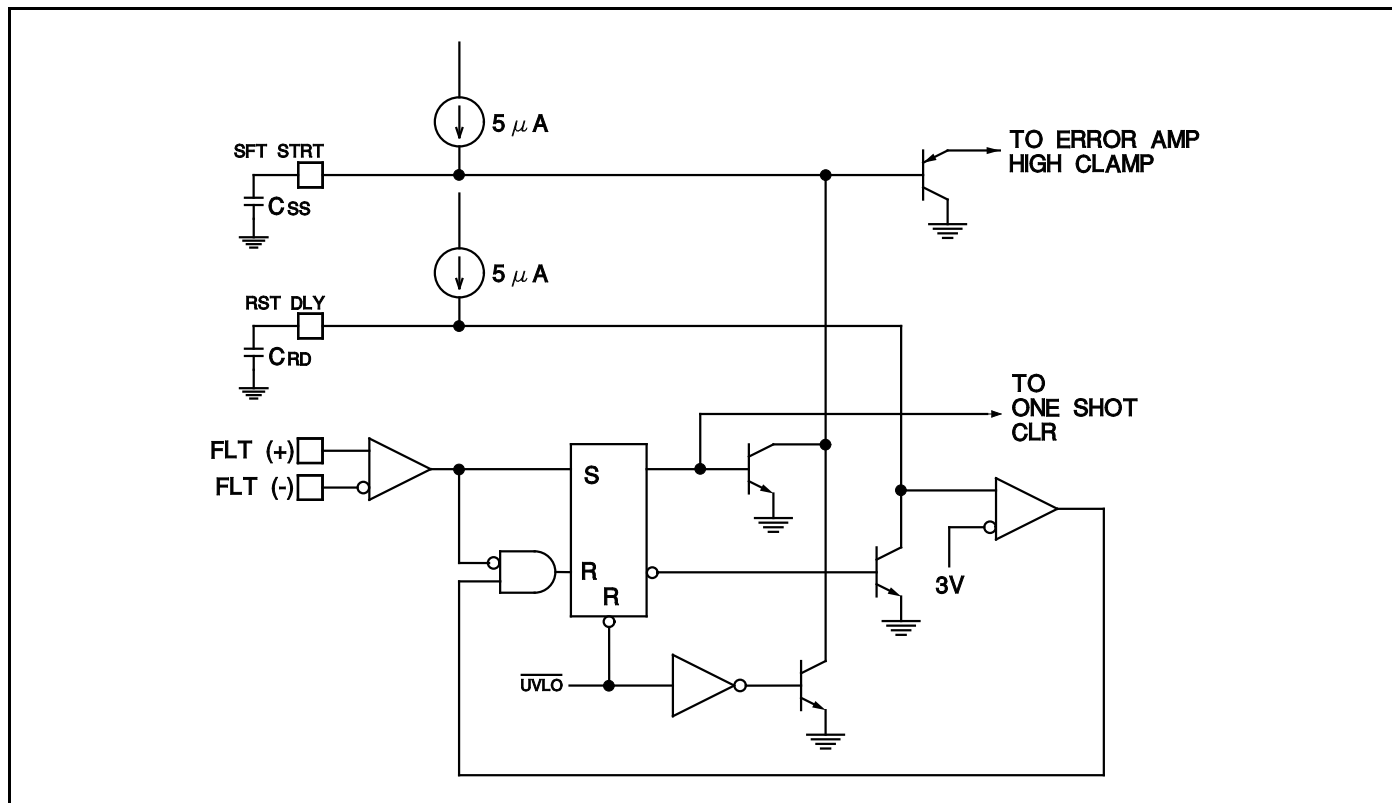
ONE SHOT TIMER

The one shot timer performs three functions and is programmed by the RC pin. The first function is to control output driver pulse width. Secondly, it clocks the toggle flip-flop. Thirdly, it establishes the maximum allowable frequency for the VFO. One shot operation is initiated at the beginning of each oscillator cycle. The RC pin, programmed by an external resistor and capacitor to ground, is charged to approximately 4.3V and then allowed to discharge. The lower threshold is approximately 80% of the peak. On time is approximately:

$$t(on) = 0.2 * R * C.$$

After crossing the lower threshold, the resistor continues to discharge the capacitor to approximately 3V, where it waits for the next oscillator cycle.





FAULT MANAGEMENT SECTION

During UVLO, the fault management section is initialized. The latch is reset, and both Sft Strt (soft start) and Rst Dly (restart delay) are pulled low. When Sft Strt is low, it lowers the upper clamp of the error amplifier. As Sft Strt increases in voltage, the upper clamp increases from a value equal to the lower clamp until it is 2V more positive. A capacitor to ground from the Sft Strt pin will control the start rate.

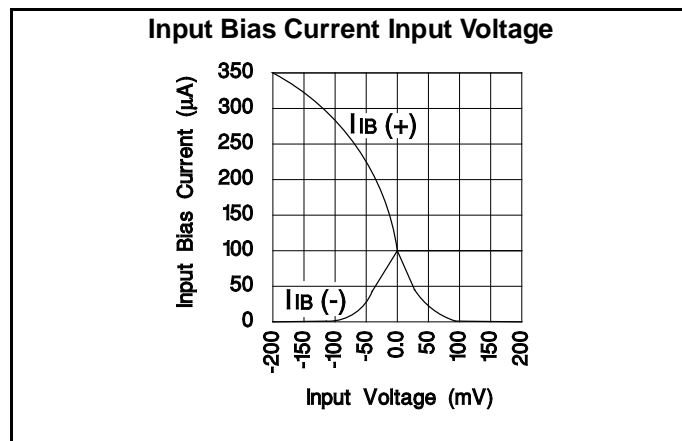
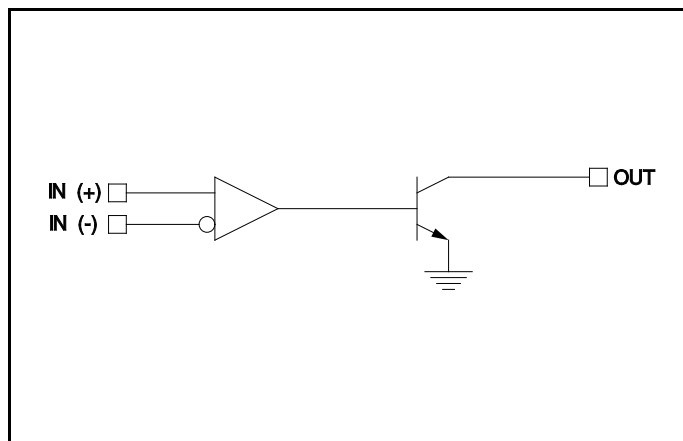
UNCOMMITTED COMPARATOR

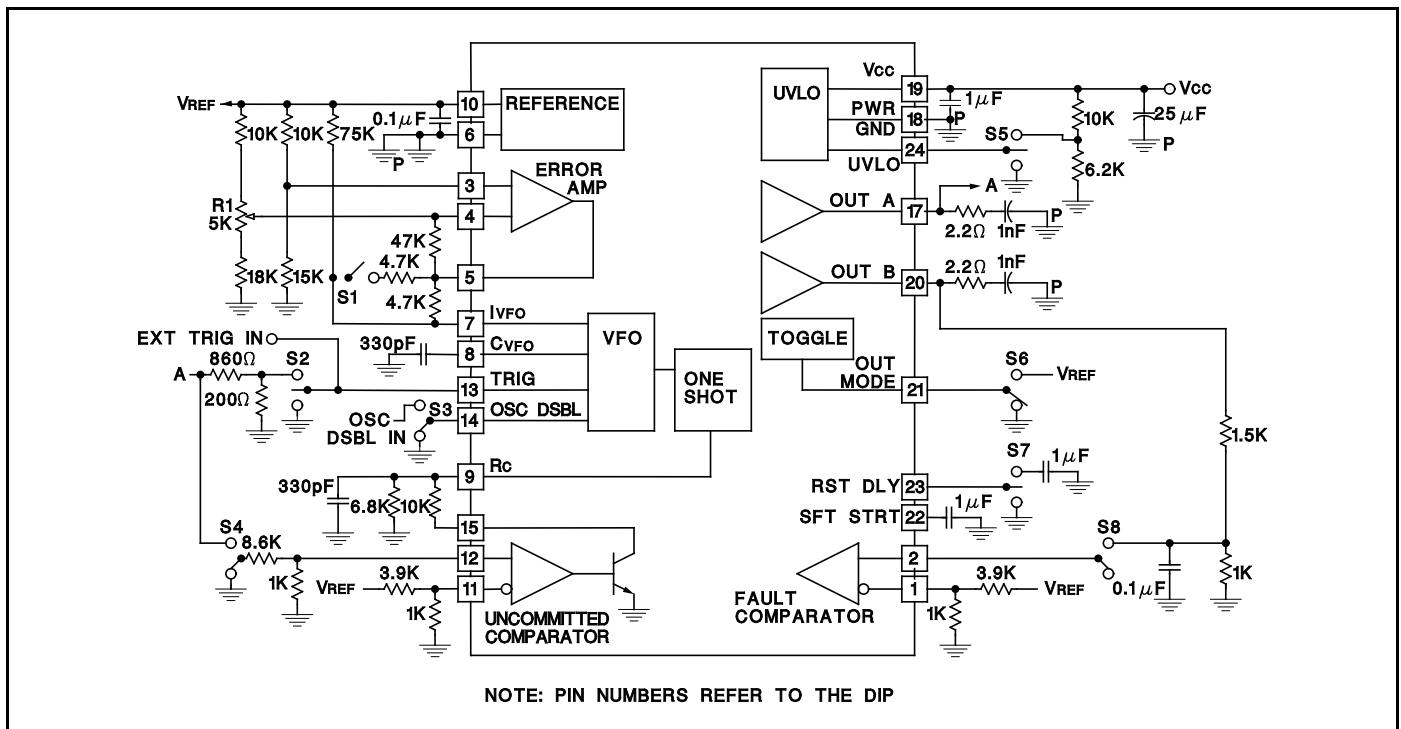
The uncommitted comparator, biased from the reference voltage, operates independently from the rest of the chip. The open collector output is capable of sinking 2mA. The inputs are valid in the common mode range of -0.3 to

3.0V. As long as one of the inputs is within this range, the other can be as high as 5V.

The high speed fault comparator will work over the input common mode range of -0.3 to 3.0V. When a fault is sensed, the one shot is immediately terminated, Sft Strt is pulled low, and Rst Dly is allowed to go high. Three modes of fault disposition can easily be implemented. If Rst Dly is externally held low, then a detected fault will shut the chip down permanently. If the Rst Dly pin is left open, a fault will simply cause an interruption of operation. If a capacitor is connected from Rst Dly to ground, then hic-up operation is implemented. The hic-up time is:

$$t(off) = 600 \text{ kohm} * C(Rst Dly).$$





OPEN LOOP LABORATORY TEST FIXTURE

The open loop laboratory test fixture is designed to allow familiarization with the operating characteristics of the UC3860. Note the pin numbers apply to the DIP.

To get started, preset all the options as follows:

Adjust the error amplifier variable resistor pot (R1) so the wiper is at a high potential.

Open the IvFO resistor switch (S1).

Throw the Trig switch (S2) to ground.

Throw the Osc Dsbl switch (S3) to ground.

Throw the uncommitted comparator switch (S4) to ground.

Throw the UVLO switch (S5) to the resistive divider.

Throw the Out Mode switch (S6) to ground.

Open the restart delay switch (S7).

Throw the fault switch (S8) to ground.

In this configuration, the chip will operate for Vcc greater than 12V. Adjustment of the following controls allows examination of specific features.

R1 adjusts the output of the error amp. Notice the voltage at pin 5 is limited from 0 to 2V above the voltage at pin 7.

S1 changes the error amp output to VFO gain. With S1 open, the maximum frequency is determined by the error amp output. With S1 closed, the one shot will set the maximum frequency.

S2 demonstrates the trigger. An external trigger signal

may be applied. When the switch is set to the resistive divider, the chip will operate in consecutive mode (ie: A,B, off,...)

S3 allows input of an external logic signal to disable the oscillator.

S4 demonstrates the uncommitted comparator. When set to output A, the comparator will accelerate the discharge of pin 9, shortening the output pulse.

S5 shorted to ground will disable the chip and the outputs will be low. If the switch is open, the Vcc start and stop thresholds are 17 and 10V. Switched to the resistive divider, the thresholds are approximately 12 and 10V.

S6 sets the mode of the toggle flip-flop. When grounded, the outputs operate alternately. Switched to 5V, the outputs switch in unison. (Note: If S6 and S2 are set for unison operation and triggered consecutive outputs, the chip will free run at the maximum frequency determined by the one shot.)

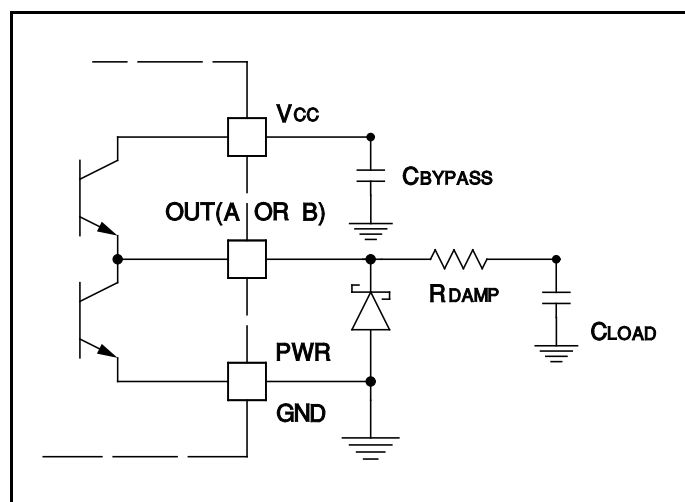
S7 open allows the chip to restart immediately after a fault sense has been removed. When grounded, it causes the chip to latch off indefinitely. This state can be reset by UVLO, Vcc, or opening the switch. Connected to 1μF programs a hic-up delay time of 600 ms.

S8 allows the simulation of a fault state. When flipped to the RC network, the comparator monitors scaled average voltage of output B. Adjusting frequency will cause the comparator to sense a 'fault' and the chip will enter fault sequence.

OUTPUT STAGE

The two totem pole output stages can be programmed by Mode to operate alternately or in unison. When Mode is low the outputs alternate. During UVLO, the outputs are low.

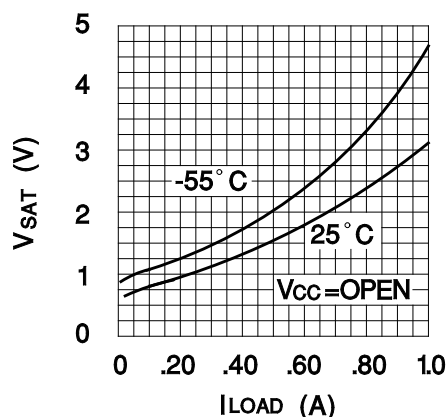
Extreme care needs to be exercised in the application of these outputs. Each output can source and sink transient currents of 2A or more and is designed for high values of di/dt . This dictates the use of a ground plane, shielded interconnect cables, Schottky diode clamps from the output pins to Pwr Gnd (power ground), and some series resistance to provide damping. Pwr Gnd should not exceed $\pm 0.2V$ from signal ground.



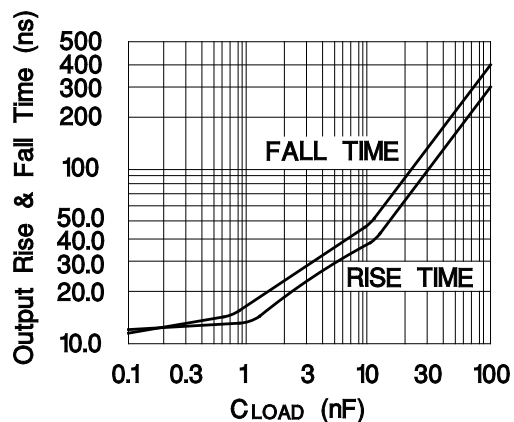
BYPASS NOTE

The reference should be bypassed with a $0.1\mu F$ ceramic capacitor from the VREF pin directly to the ground plane near the Signal Ground pin. The timing capacitors on CVFO and RC should be treated likewise. Vcc, however, should be bypassed with a ceramic capacitor from the Vcc pin to the section of ground plane that is connected to Power Ground. Any required bulk reservoir capacitor should parallel this one. The two ground plane sections can then be joined at a single point to optimize noise rejection and minimize DC drops.

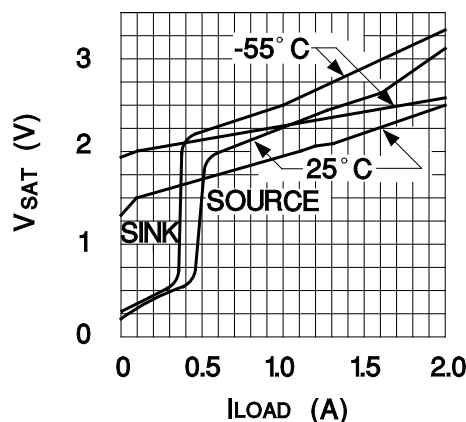
Output Saturation Voltage vs Load Current



Output Rise & Fall Time vs Load Capacitance



Output Saturation Voltage vs Load Current



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
UC1860J	OBSOLETE	CDIP	J	24		TBD	Call TI	Call TI
UC1860J883B	OBSOLETE	CDIP	J	24		TBD	Call TI	Call TI
UC2860DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
UC2860DWTR	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
UC2860N	OBSOLETE	PDIP	N	24		TBD	Call TI	Call TI
UC2860Q	OBSOLETE	PLCC	FN	28		TBD	Call TI	Call TI
UC2860QTR	OBSOLETE	PLCC	FN	28		TBD	Call TI	Call TI
UC3860DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
UC3860DWTR	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
UC3860N	OBSOLETE	PDIP	N	24		TBD	Call TI	Call TI
UC3860Q	OBSOLETE	PLCC	FN	28		TBD	Call TI	Call TI
UC3860QTR	OBSOLETE	PLCC	FN	28		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2008, Texas Instruments Incorporated