DATA SHEET

MOS FIELD EFFECT TRANSISTOR
2SK3458

SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK3458 is N-channel DMOS FET device that features a low gate charge and excellent switching characteristics, designed for high voltage applications such as switching power supply.

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3458	TO-220AB
2SK3458-S	TO-262
2SK3458-ZK	TO-263

FEATURES

- Low gate charge
  Q_G = 25 nC TYP. (V_{DD} = 450 V, V_{GS} = 10 V, I_D = 6.0 A)
- Gate voltage rating ±30 V
- Low on-state resistance
  $R_{DS(on)}$ = 2.2 Ω MAX. (V_{GS} = 10 V, I_D = 3.0 A)
- Avalanche capability ratings
- Surface mount package available

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	800	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±30	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±6.0	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±24	A
Total Power Dissipation (T_A = 25°C)	P_{T1}	1.5	W
Total Power Dissipation (T_C = 25°C)	P_{T2}	100	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current Note2	I_{AS}	6.0	A
Single Avalanche Energy Note2	E_{AS}	66.5	mJ

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

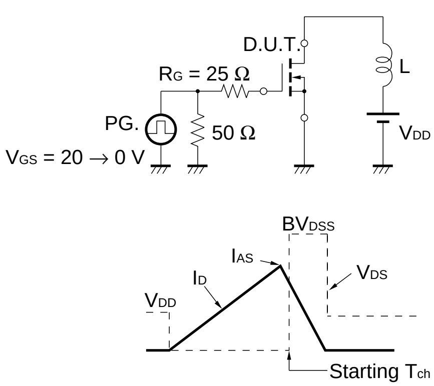
2. Starting T_{ch} = 25°C, V_{DD} = 150 V, R_G = 25 Ω, V_{GS} = 20 → 0 V

Document No. D14755EJ1V0DS00 (1st edition)
Date Published June 2002 NS CP(K)
Printed in Japan

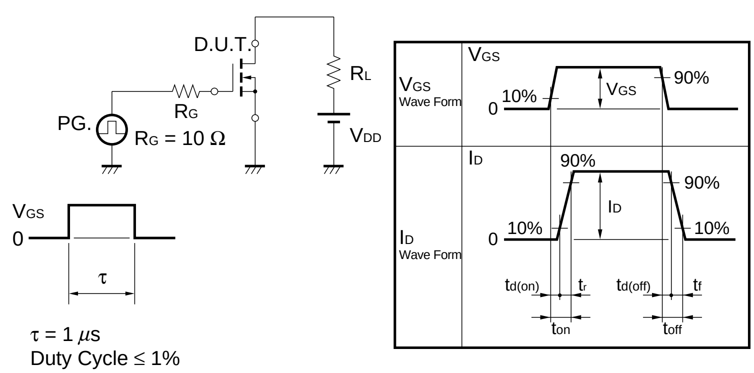
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 800 V, V_{GS} = 0 V			100	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V			±100	nA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	2.5		3.5	V
Forward Transfer Admittance	| y_{fs} |	V_{DS} = 10 V, I_D = 3.0 A	2.0			S
Drain to Source On-state Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 3.0 A		1.8	2.2	Ω
Input Capacitance	C_{iss}	V_{DS} = 10 V		1220		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		170		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		16		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 150 V, I_D = 3.0 A		17		ns
Rise Time	t_r	V_{GS} = 10 V		7		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		43		ns
Fall Time	t_f			11		ns
Total Gate Charge	Q_G	V_{DD} = 450 V		25		nC
Gate to Source Charge	Q_{GS}	V_{GS} = 10 V		6		nC
Gate to Drain Charge	Q_{GD}	I_D = 6.0 A		10		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 6.0 A, V_{GS} = 0 V		1.0		V
Reverse Recovery Time	t_{rr}	I_F = 6.0 A, V_{GS} = 0 V		1490		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 50 A/ μs		7.5		μC

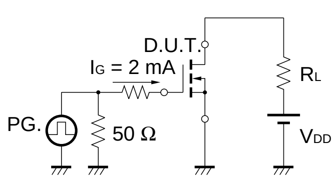
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

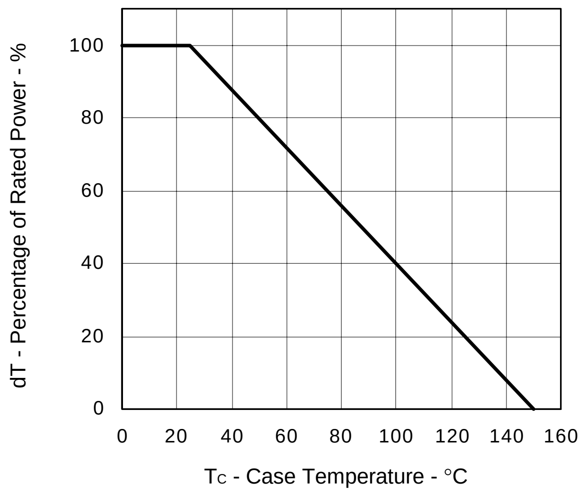


TEST CIRCUIT 3 GATE CHARGE

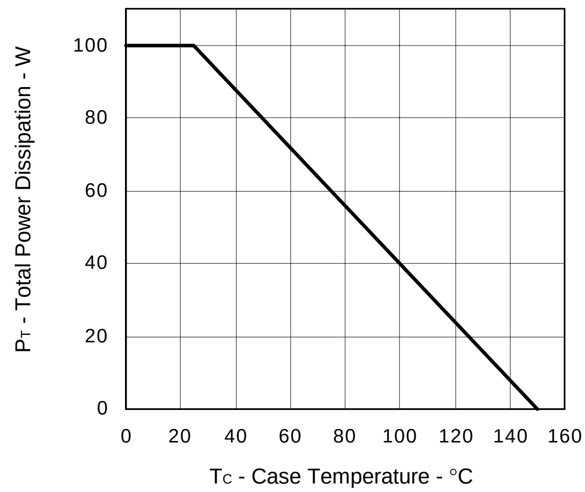


TYPICAL CHARACTERISTICS (T_A = 25°C)

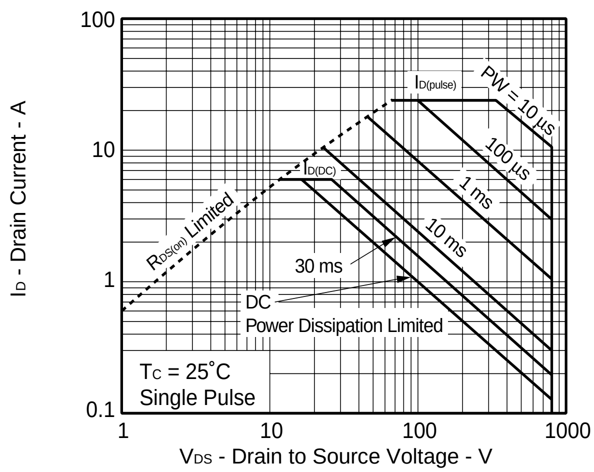
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



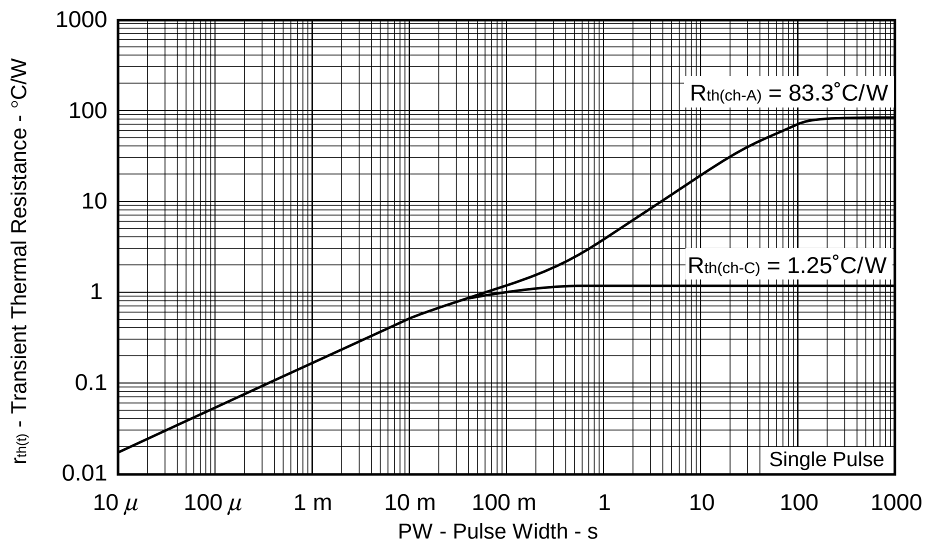
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



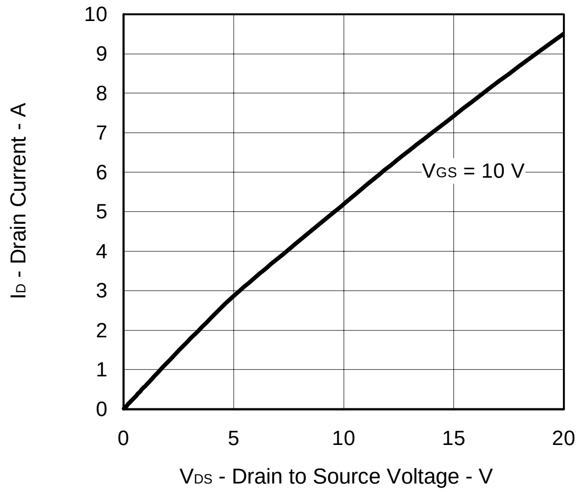
FORWARD BIAS SAFE OPERATING AREA



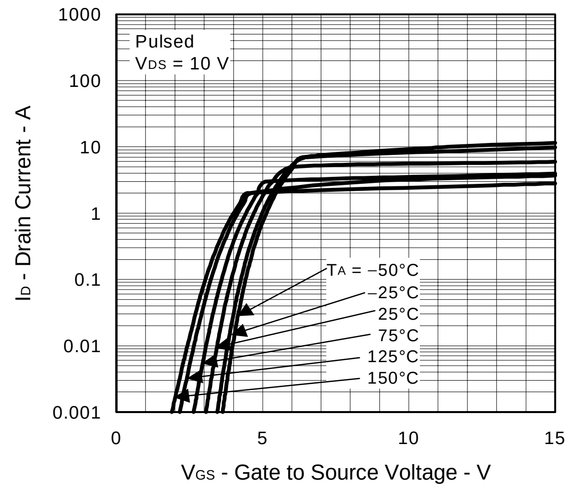
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



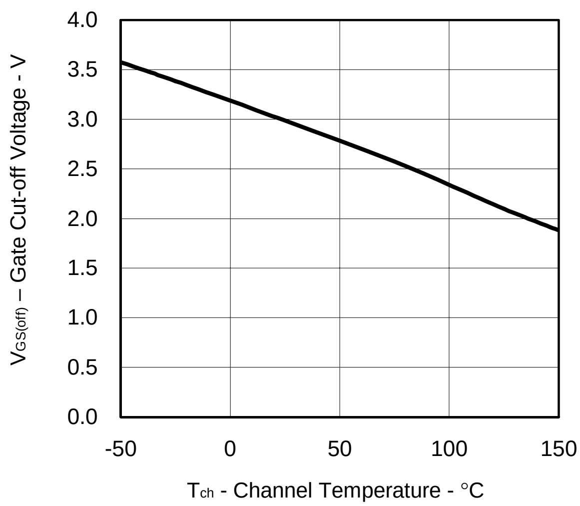
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



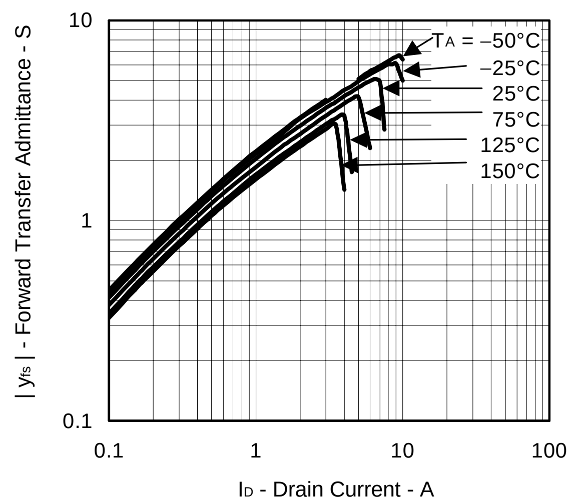
FORWARD TRANSFER CHARACTERISTICS



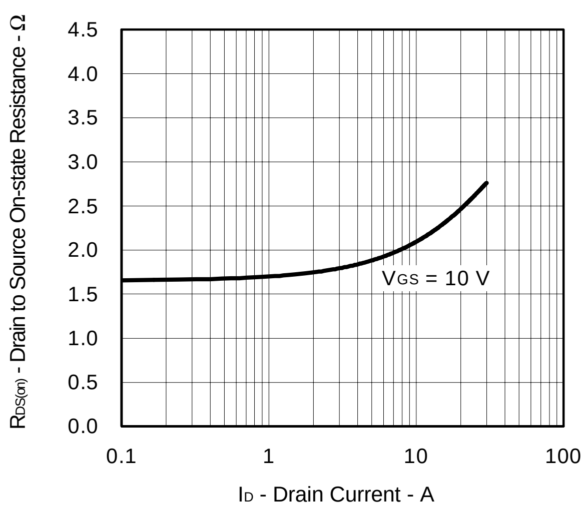
GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



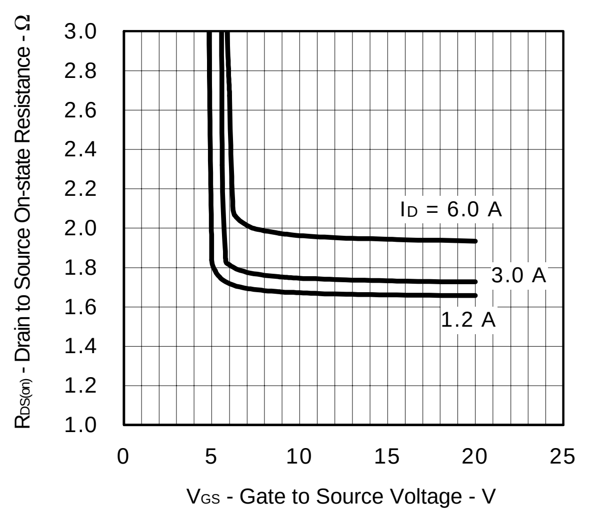
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



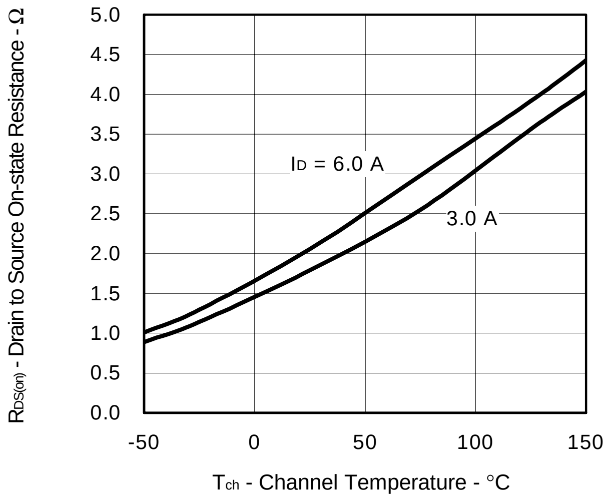
DRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENT



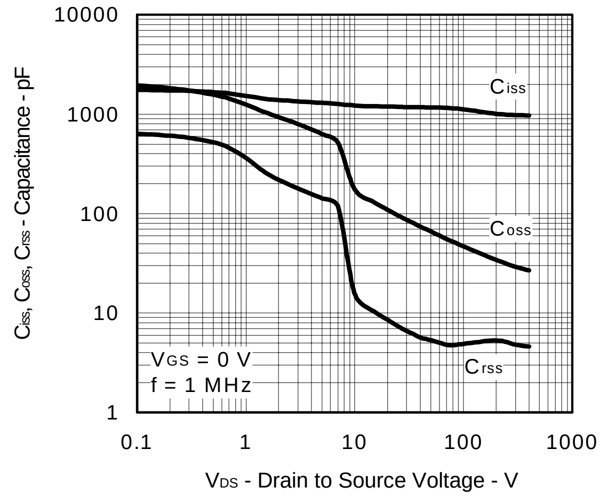
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



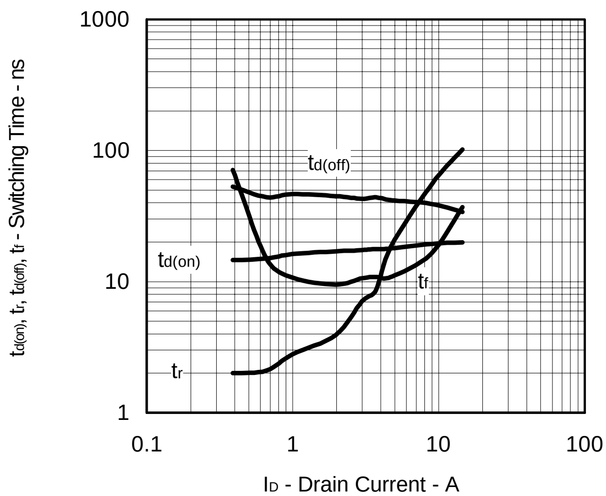
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
CHANNEL TEMPERATURE



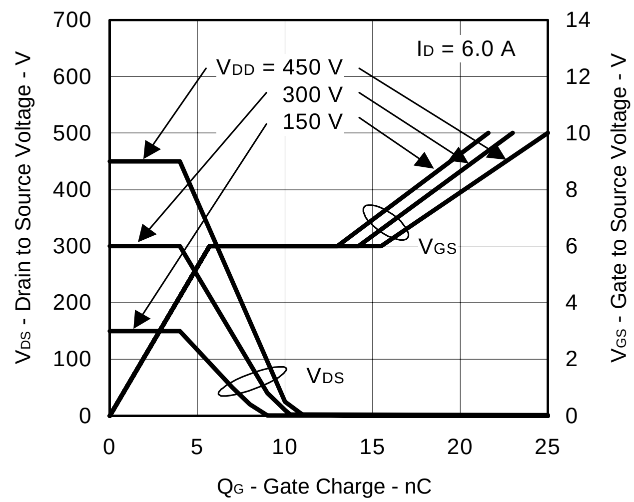
CAPACITANCE vs.
DRAIN TO SOURCE VOLTAGE



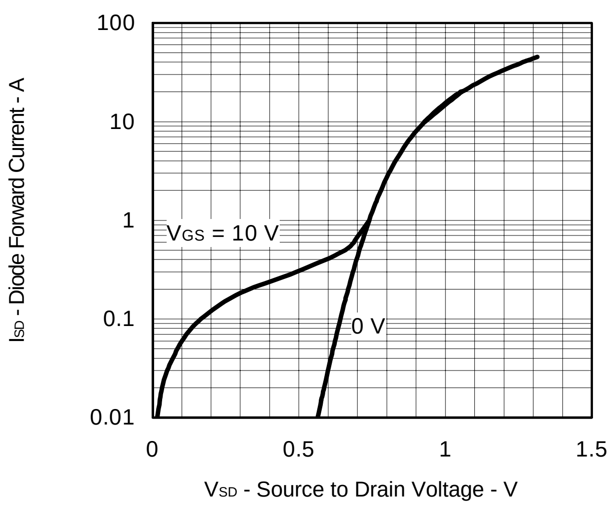
SWITCHING CHARACTERISTICS



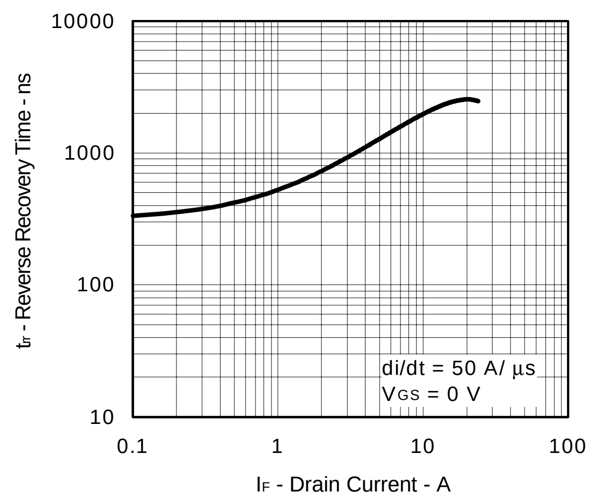
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



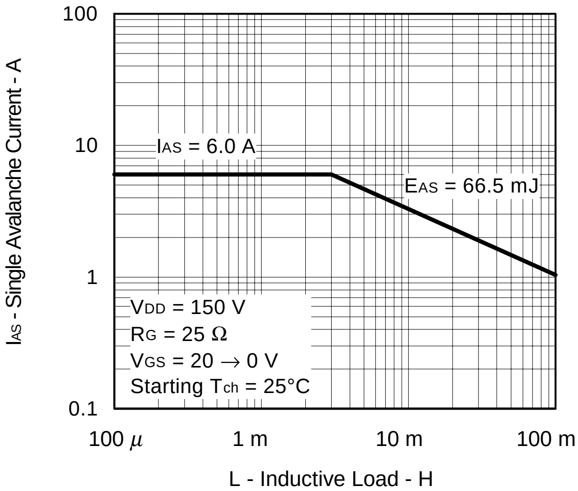
SOURCE TO DRAIN DIODE
FORWARD VOLTAGE



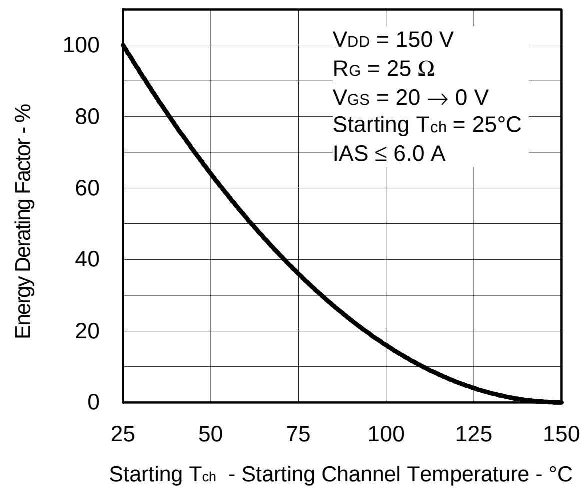
REVERSE RECOVERY TIME vs. DRAIN CURRENT



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD

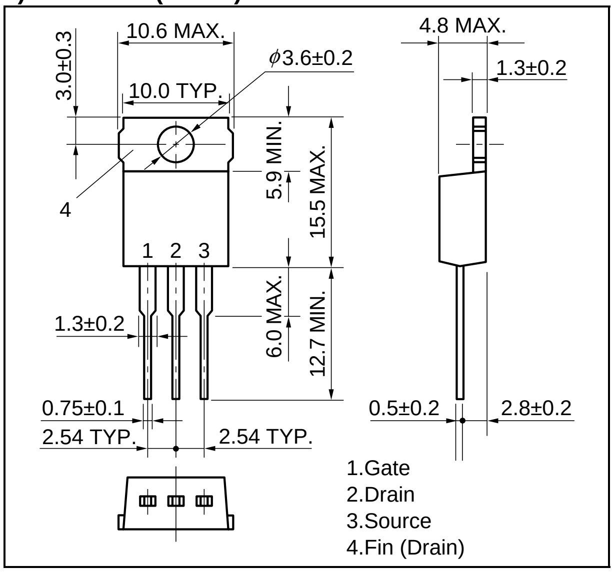


SINGLE AVALANCHE ENERGY DERATING FACTOR

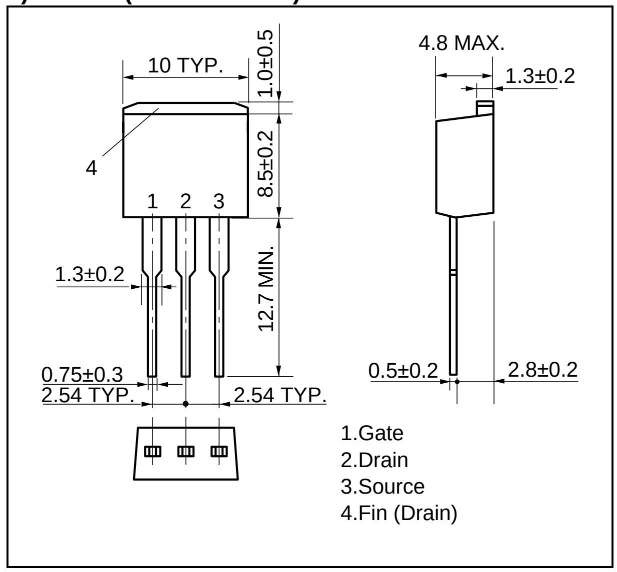


PACKAGE DRAWINGS (Unit: mm)

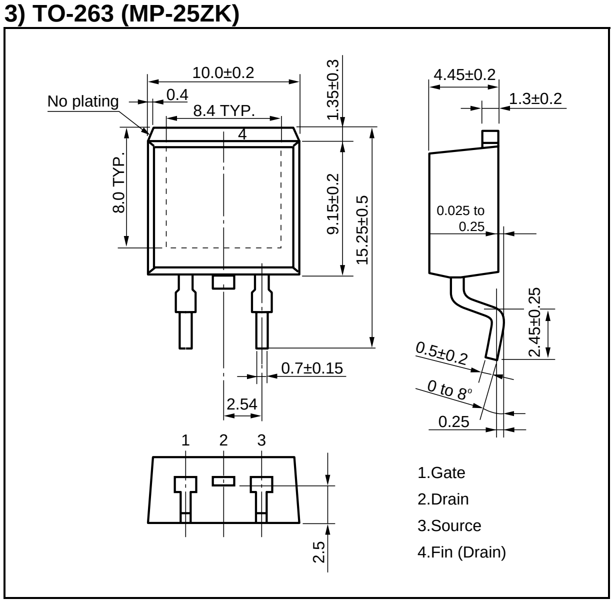
1) TO-220AB (MP-25)



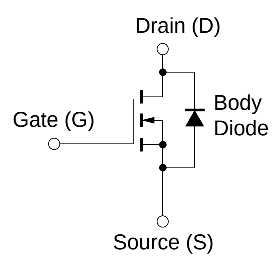
2) TO-262 (MP-25 Fin Cut)



3) TO-263 (MP-25ZK)



EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.