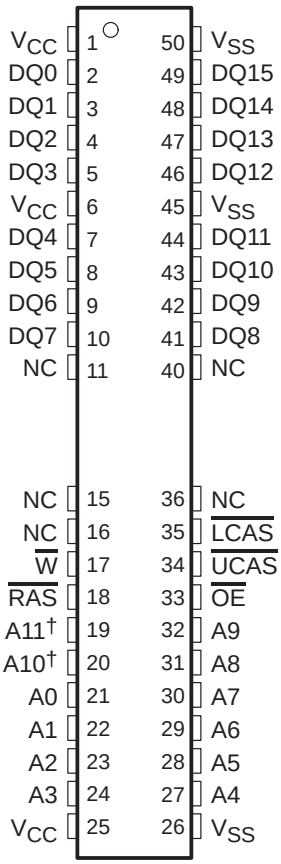
- **Organization . . . 1048576 × 16**
- **Single Power Supply (5 V or 3.3 V)**
- **Performance Ranges:**

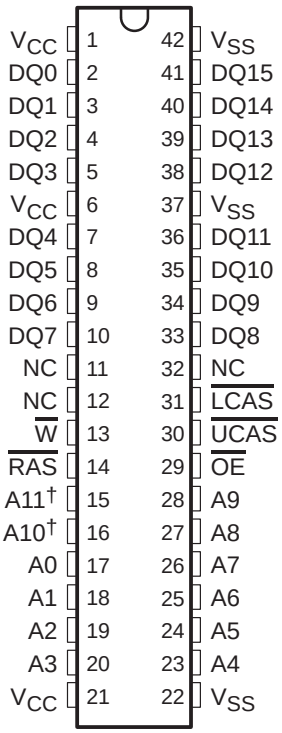
	ACCESS TIME t_{RAC} MAX	ACCESS TIME t_{CAC} MAX	ACCESS TIME t_{AA} MAX	READ OR WRITE CYCLE MIN
'4xx160/P-60	60 ns	15 ns	30 ns	110 ns
'4xx160/P-70	70 ns	18 ns	35 ns	130 ns
'4xx160/P-80	80 ns	20 ns	40 ns	150 ns

- **Enhanced Page-Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$ ($\overline{CBR}$) Refresh**
- **Long Refresh Period and Self-Refresh Option (TMS4xx160P)**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **High-Reliability Plastic 42-Lead (DZ Suffix) 400-Mil-Wide Surface-Mount (SOJ) Package and 44/50-Lead (DGE Suffix) Surface-Mount Thin Small-Outline Package (TSOP)**
- **Operating Free-Air Temperature Range 0°C to 70°C**
- **Fabricated Using the Texas Instruments Enhanced Performance Implanted CMOS (EPIC™) Technology**

DGE PACKAGE
(TOP VIEW)



DZ PACKAGE
(TOP VIEW)



† A10 and A11 are NC for TMS4x8160 and TMS4x8160P.

AVAILABLE OPTIONS

DEVICE	POWER SUPPLY	SELF REFRESH, BATTERY BACKUP	REFRESH CYCLES
TMS416160	5 V	—	4096 in 64 ms
TMS416160P	5 V	Yes	4096 in 128 ms
TMS418160	5 V	—	1024 in 16 ms
TMS418160P	5 V	Yes	1024 in 128 ms
TMS426160	3.3 V	—	4096 in 64 ms
TMS426160P	3.3 V	Yes	4096 in 128 ms
TMS428160	3.3 V	—	1024 in 16 ms
TMS428160P	3.3 V	Yes	1024 in 128 ms

PIN NOMENCLATURE

A0 – A11	Address Inputs
$\overline{DQ0}$ – DQ15	Data In / Data Out
$\overline{LCAS}$	Lower Column-Address Strobe
$\overline{UCAS}$	Upper Column-Address Strobe
$\overline{NC}$	No Internal Connection
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
V_{CC}	5-V or 3.3-V Supply‡
V_{SS}	Ground
$\overline{W}$	Write Enable

‡ See Available Options Table.

description

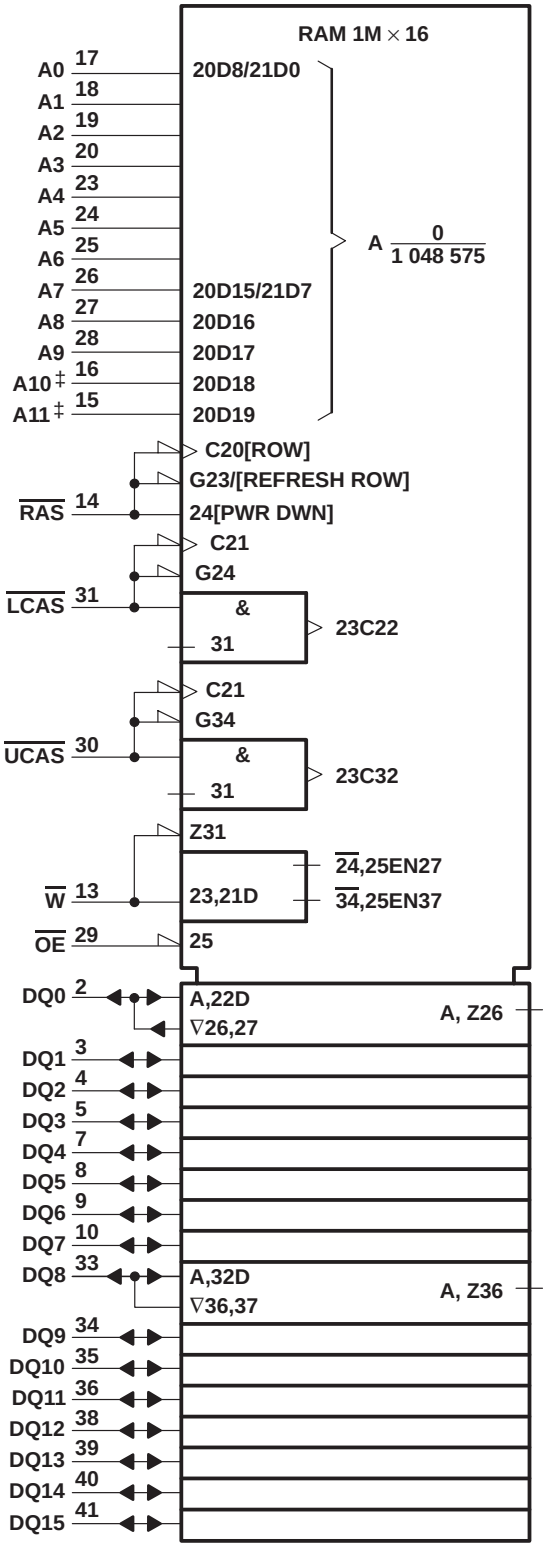
The TMS4xx160 series is a set of high-speed, 16777216-bit dynamic random-access memories (DRAMs) organized as 1048576 words of 16 bits each. The TMS4xx160P series is a similar set of high-speed, low-power, self-refresh, 16777216-bit DRAMs organized as 1048576 words of 16 bits each. Both sets employ state-of-the-art enhanced performance implanted CMOS (EPIC™) technology for high performance, reliability, and low power at low cost.

description (continued)

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. All addresses and data-in lines are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

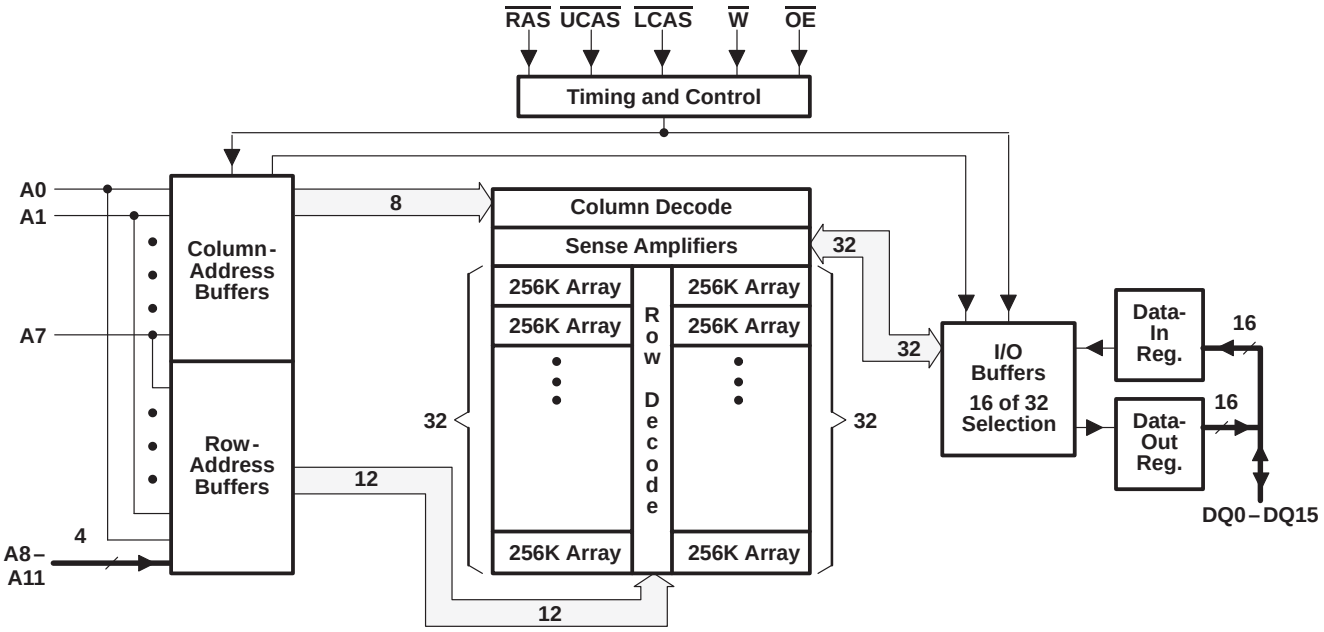
The TMS4xx160 and TMS4xx160P are offered in a 44/50-lead plastic surface-mount TSOP (DGE suffix) and a 42-lead plastic surface-mount SOJ (DZ suffix) package. These packages are characterized for operation from 0°C to 70°C.

logic symbol†



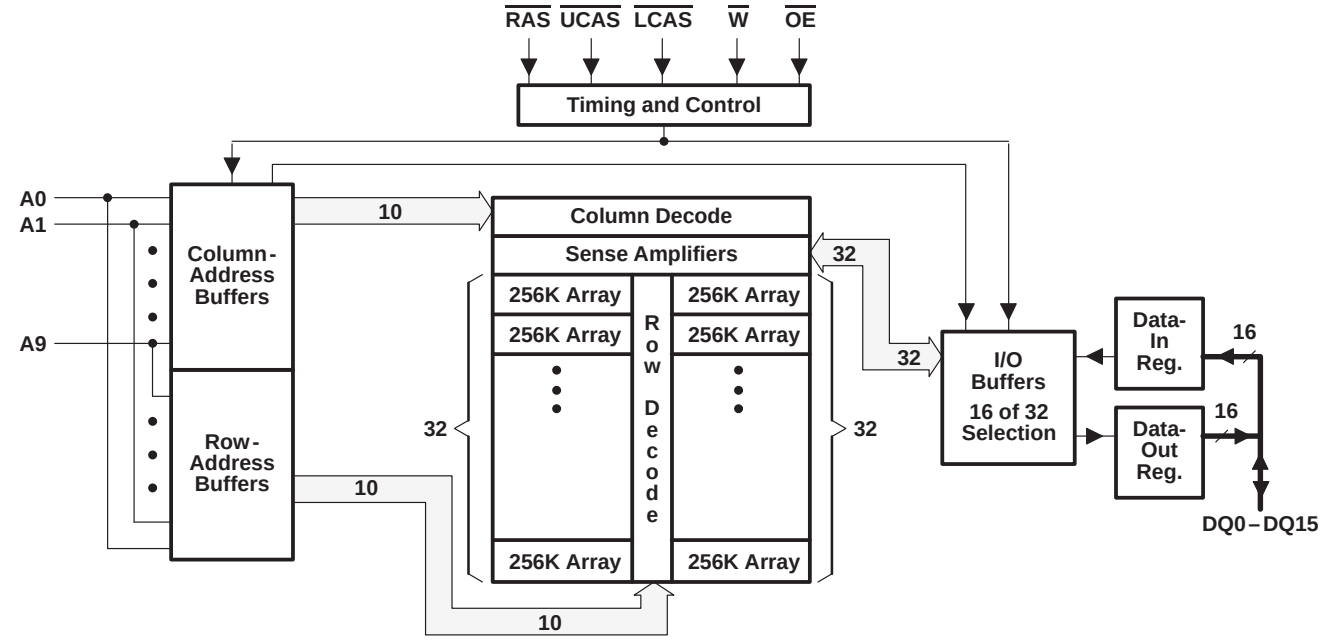
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown correspond to the DZ package.
‡ A10 and A11 are NC for TMS4x8160 and TMS4x8160P.

functional block diagrams (TMS4x6160/P)



(a) TMS4x6160, TMS4x6160P

functional block diagram (TMS4x8160/P)



(b) TMS4x8160, TMS4x8160P

operation

dual $\overline{CAS}$

Two $\overline{CAS}$ pins ($\overline{LCAS}$ and $\overline{UCAS}$) are provided to give independent control of the 16 data-I/O pins (DQ0–DQ15), with $\overline{LCAS}$ corresponding to DQ0–DQ7 and $\overline{UCAS}$ corresponding to DQ8–DQ15. For read or write cycles, the column address is latched on the first $\overline{xCAS}$ falling edge. Each $\overline{xCAS}$ going low enables its corresponding DQx pin with data associated with the column address latched on the first falling $\overline{xCAS}$ edge. All address setup and hold parameters are referenced to the first falling $\overline{xCAS}$ edge.The delay time from $\overline{xCAS}$ low to valid data out (see parameter t_{CAC}) is measured from each individual $\overline{xCAS}$ to its corresponding DQx pin.

In order to latch in a new column address, both $\overline{xCAS}$ pins must be brought high. The column-precharge time (see parameter t_{CP}) is measured from the last $\overline{xCAS}$ rising edge to the first $\overline{xCAS}$ falling edge of the new cycle. Keeping a column address valid while toggling $\overline{xCAS}$ requires a minimum setup time, t_{CLCH}. During t_{CLCH}, at least one $\overline{xCAS}$ must be brought low before the other $\overline{xCAS}$ is taken high.

For early-write cycles, the data is latched on the first $\overline{xCAS}$ falling edge. Only the DQs that have the corresponding $\overline{xCAS}$ low are written into. Each $\overline{xCAS}$ must meet t_{CAS} minimum in order to ensure writing into the storage cell. To latch a new address and new data, all $\overline{xCAS}$ pins must be high and meet t_{CP}.

enhanced page mode

Page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is eliminated. The maximum number of columns that can be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{xCAS}$ page-mode cycle time used. With minimum $\overline{xCAS}$ page-cycle time, all columns can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{xCAS}$ is high. The falling edge of the first $\overline{xCAS}$ latches the column addresses. This feature allows the devices to operate at a higher data bandwidth than conventional page-mode parts because data retrieval begins as soon as the column address is valid rather than when $\overline{xCAS}$ transitions low. This performance improvement is referred to as enhanced page mode. A valid column address may be presented immediately after t_{RAH} (row-address hold time) has been satisfied, usually well in advance of the falling edge of $\overline{xCAS}$. In this case, data is obtained after t_{CAC} maximum (access time from $\overline{xCAS}$ low) if t_{AA} maximum (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{xCAS}$ goes high, minimum access time for the next cycle is determined by t_{CPA} (access time from rising edge of the last $\overline{xCAS}$).

address: A0–A11 (TMS4x6160, TMS4x6160P) and A0–A9 (TMS4x8160, TMS4x8160P)

Twenty address bits are required to decode 1 of 1048576 storage cell locations. For the TMS4x6160 and TMS4x6160P, 12 row-address bits are set up on A0 through A11 and latched onto the chip by $\overline{RAS}$. Eight column-address bits are set up on A0 through A7 and latched onto the chip by the first $\overline{xCAS}$. For the TMS4x8160 and TMS4x8160P, 10 row-address bits are set up on A0–A9 and latched onto the chip by $\overline{RAS}$. Ten column-address bits are set up on A0–A9 and latched onto the chip by the first $\overline{xCAS}$. All addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{xCAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{xCAS}$ is used as a chip select, activating its corresponding output buffer and latching the address bits into the column-address buffers.

write enable ($\overline{W}$)

The read or write mode is selected through $\overline{W}$. A logic high on $\overline{W}$ selects the read mode and a logic low selects the write mode. The data inputs are disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{xCAS}$ (early write), data out remains in the high-impedance state for the entire cycle, permitting a write operation with $\overline{OE}$ grounded.

data in (DQ0 – DQ15)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{xCAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{xCAS}$ and the data is strobed in by the first occurring $\overline{xCAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{xCAS}$ is already low and the data is strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{OE}$ must be high to bring the output buffers to the high-impedance state prior to applying data to the I/O lines.

data out (DQ0 – DQ15)

Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{xCAS}$ and $\overline{OE}$ are brought low. In a read cycle, the output becomes valid after the access time interval t_{CAC} (which begins with the negative transition of $\overline{xCAS}$) as long as t_{RAC} and t_{AA} are satisfied.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle activates the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{xCAS}$ to be brought low for the output buffers to go into the low-impedance state, and they remain in the low-impedance state until either $\overline{OE}$ or $\overline{xCAS}$ is brought high.

$\overline{RAS}$-only refresh

TMS4x6160, TMS4x6160P

A refresh operation must be performed at least once every 64 ms (128 ms for TMS4x6160P) to retain data. This can be achieved by strobing each of the 4096 rows (A0 – A11). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding both $\overline{xCAS}$ at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh.

TMS4x8160, TMS4x8160P

A refresh operation must be performed at least once every 16 ms (128 ms for TMS4x8160P) to retain data. This can be achieved by strobing each of the 1024 rows (A0 – A9). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding both $\overline{xCAS}$ at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh.

hidden refresh

Hidden refresh can be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{xCAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle. The external address is ignored and the refresh address is generated internally.

$\overline{xCAS}$-before-$\overline{RAS}$ (xCBR) refresh

$\overline{xCBR}$ refresh is utilized by bringing at least one $\overline{xCAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{xCBR}$ refresh cycles, $\overline{xCAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

battery-backup refresh

TMS4x6160P

A low-power battery-backup refresh mode that requires less than 600 µA (5 V) or 350 µA (3.3 V) refresh current is available on the TMS4x6160P. Data integrity is maintained using $\overline{xCBR}$ refresh with a period of 31.25 µs while holding $\overline{RAS}$ low for less than 300 ns. To minimize current consumption, all input levels must be at CMOS levels ($V_{IL} < 0.2$ V, $V_{IH} > V_{CC} - 0.2$ V).

TMS4x8160P

A low-power battery-backup refresh mode that requires less than 600 μA (5 V) or 350 μA (3.3 V) refresh current is available on the TMS4x8160P. Data integrity is maintained using xCBR refresh with a period of 125 μs while holding $\overline{RAS}$ low for less than 300 ns. To minimize current consumption, all input levels must be at CMOS levels (V_{IL} < 0.2 V, $V_{IH} > V_{CC} – 0.2$ V).

self refresh (TMS4xx160P)

The self-refresh mode is entered by dropping $\overline{xCAS}$ low prior to $\overline{RAS}$ going low. Then $\overline{xCAS}$ and $\overline{RAS}$ are both held low for a minimum of 100 μs. The chip is then refreshed internally by an on-board oscillator. No external address is required because the CBR counter is used to keep track of the address. To exit the self-refresh mode, both $\overline{RAS}$ and $\overline{xCAS}$ are brought high to satisfy t_{CHS}. Upon exiting self-refresh mode, a burst refresh (refresh a full set of row addresses) must be executed before continuing with normal operation. The burst refresh ensures the DRAM is fully refreshed.

power up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after power up to the full V_{CC} level. These eight initialization cycles must include at least one refresh ($\overline{RAS}$-only or $\overline{xCBR}$) cycle.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}: TMS41x160, TMS41x160P . . . . . – 1 V to 7 V
TMS42x160, TMS42x160P . . . . . – 0.5 V to 4.6 V
Voltage range on any pin (see Note 1): TMS41x160, TMS41x160P . . . . . – 1 V to 7 V
TMS42x160, TMS42x160P . . . . . – 0.5 V to 4.6 V
Short-circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . – 55°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		TMS41x160			TMS42x160			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	3	3.3	3.6	V
V_{SS}	Supply voltage		0			0		V
V_{IH}	High-level input voltage	2.4		6.5	2		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	– 0.3		0.8	V
T_A	Operating free-air temperature	0		70	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

TMS416160/P

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		'416160-60 '416160P-60		'416160-70 '416160P-70		'416160-80 '416160P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{xCAS}$ high			± 10		± 10		± 10	µA
I_{CC1}‡§	Read- or write-cycle current	V_{CC} = 5.5 V, Minimum cycle			90		80		70	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high			2		2		2	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high	'416160		1		1		1	mA
			'416160P		500		500		500	µA
I_{CC3}§	Average refresh current ($\overline{RAS}$-only refresh or CBR)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{xCAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{xCAS}$ low (CBR)			90		80		70	mA
I_{CC4}‡¶	Average page current	V_{CC} = 5.5 V, t_{PC} = MIN, $\overline{RAS}$ low, $\overline{xCAS}$ cycling			90		80		70	mA
I_{CC6}#	Self-refresh current	$\overline{xCAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} min			500		500		500	µA
I_{CC10}#	Battery back-up operating current (equivalent refresh time is 128 ms); CBR only	t_{RC} = 31.25 µs, t_{RAS} ≤ 300 ns, V_{CC} – 0.2 V ≤ V_{IH} ≤ 6.5 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and data stable			600		600		600	µA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change while $\overline{xCAS}$ = V_{IH}
# For TMS416160P only

TMS418160/P

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS†		'418160-60 '418160P-60		'418160-70 '418160P-70		'418160-80 '418160P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{xCAS}$ high			± 10		± 10		± 10	µA
I_{CC1}‡§	Read- or write-cycle current	V_{CC} = 5.5 V, Minimum cycle			190		180		170	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high			2		2		2	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high	'418160		1		1		1	mA
			'418160P		500		500		500	µA
I_{CC3}§	Average refresh current ($\overline{RAS}$-only refresh or CBR)	V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{RAS}$ low after $\overline{xCAS}$ low (CBR)	Minimum cycle, $\overline{xCAS}$ high ($\overline{RAS}$ only),		190		180		170	mA
I_{CC4}‡¶	Average page current	V_{CC} = 5.5 V, $\overline{RAS}$ low,	t_{PC} = MIN, $\overline{xCAS}$ cycling		100		90		80	mA
I_{CC6}#	Self-refresh current	$\overline{xCAS}$ < 0.2 V, Measured after t_{RASS} min	$\overline{RAS}$ < 0.2 V,		500		500		500	µA
I_{CC10}#	Battery back-up operating current (equivalent refresh time is 128 ms); CBR only	t_{RC} = 125 µs, V_{CC} – 0.2 V ≤ V_{IH} ≤ 6.5 V, 0 V ≤ V_{IL} ≤ 0.2 V, Address and data stable	t_{RAS} ≤ 300 ns, $\overline{W}$ and $\overline{OE}$ = V_{IH},		600		600		600	µA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change while $\overline{xCAS}$ = V_{IH}
# For TMS418160P only

TMS426160/P

electrical characteristics over recommended ranges of supply voltage and operating free-air conditions (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS†		'426160-60 '426160P-60		'426160-70 '426160P-70		'426160-80 '426160P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 2 mA	LVTTL	2.4		2.4		2.4		V
		I_{OH} = – 100 µA	LVCMOS	V_{CC}–0.2		V_{CC}–0.2		V_{CC}–0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA	LVTTL		0.4		0.4		0.4	V
		I_{OL} = 100 µA	LVCMOS		0.2		0.2		0.2	
I_I	Input current (leakage)	V_{CC} = 3.6 V, V_I = 0 V to 3.9 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 3.6 V, V_O = 0 V to V_{CC}, $\overline{xCAS}$ high			± 10		± 10		± 10	µA
I_{CC1}‡§	Read- or write-cycle current	V_{CC} = 3.6 V, Minimum cycle			90		80		70	mA
I_{CC2}	Standby current	V_{IH} = 2 V (LVTTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high			1		1		1	mA
		V_{IH} = V_{CC} – 0.2 V (LVCMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high	'426160		500		500		500	µA
			'426160P		200		200		200	µA
I_{CC3}§	Average refresh current ($\overline{RAS}$-only refresh or CBR)	V_{CC} = 3.6 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{xCAS}$ high ($\overline{RAS}$-only refresh) $\overline{RAS}$ low after $\overline{xCAS}$ low (CBR)			90		80		70	mA
I_{CC4}‡¶	Average page current	V_{CC} = 3.6 V, t_{PC} = MIN, $\overline{RAS}$ low, $\overline{xCAS}$ cycling			90		80		70	mA
I_{CC6}#	Self-refresh current	$\overline{xCAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} min			250		250		250	µA
I_{CC10}#	Battery back-up operating current (equivalent refresh time is 128 ms), CBR only	t_{RC} = 31.25 µs, t_{RAS} ≤ 300 ns, V_{CC} – 0.2 V ≤ V_{IH} ≤ 3.9 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and data stable			350		350		350	µA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change while $\overline{xCAS}$ = V_{IH}
# For TMS426160P only

TMS428160/P

electrical characteristics over recommended ranges of supply voltage and operating free-air conditions (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS†		'428160-60 '428160P-60		'428160-70 '428160P-70		'428160-80 '428160P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 2 mA	LVTTL	2.4		2.4		2.4		V
		I_{OH} = – 100 µA	LVCMOS	V_{CC}–0.2		V_{CC}–0.2		V_{CC}–0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA	LVTTL		0.4		0.4		0.4	V
		I_{OL} = 100 µA	LVCMOS		0.2		0.2		0.2	
I_I	Input current (leakage)	V_{CC} = 3.6 V, V_I = 0 V to 3.9 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 3.6 V, V_O = 0 V to V_{CC}, $\overline{xCAS}$ high			± 10		± 10		± 10	µA
I_{CC1}‡§	Read- or write-cycle current	V_{CC} = 3.6 V, Minimum cycle			190		180		170	mA
I_{CC2}	Standby current	V_{IH} = 2 V (LVTTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high			1		1		1	mA
		V_{IH} = V_{CC} – 0.2 V (LVCMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high	'428160		500		500		500	µA
			'428160P		200		200		200	µA
I_{CC3}§	Average refresh current ($\overline{RAS}$-only refresh or CBR)	V_{CC} = 3.6 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{xCAS}$ high ($\overline{RAS}$-only refresh) $\overline{RAS}$ low after $\overline{xCAS}$ low (CBR)			190		180		170	mA
I_{CC4}‡¶	Average page current	V_{CC} = 3.6 V, t_{PC} = MIN, $\overline{RAS}$ low, $\overline{xCAS}$ cycling			100		90		80	mA
I_{CC6}#	Self-refresh current	$\overline{xCAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} min			250		250		250	µA
I_{CC10}#	Battery back-up operating current (equivalent refresh time is 128 ms), CBR only	t_{RC} = 125 µs, t_{RAS} ≤ 300 ns, V_{CC} – 0.2 V ≤ V_{IH} ≤ 3.9 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and data stable			350		350		350	µA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change while $\overline{xCAS}$ = V_{IH}
# For TMS428160P only

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0 – A11		5	pF
$C_{i(OE)}$	Input capacitance, $\overline{OE}$		7	pF
$C_{i(RC)}$	Input capacitance, $\overline{xCAS}$ and $\overline{RAS}$		7	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		7	pF
C_O	Output capacitance		7	pF

NOTE 3: V_{CC} = 5 V ± 0.5 V or 3.3 V ÷ 0.3 V (see Table 1), and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'4xx160-60 '4xx160P-60		'4xx160-70 '4xx160P-70		'4xx160-80 '4xx160P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address (see Note 4)		30		35		40	ns
t_{CAC}	Access time from $\overline{xCAS}$ low (see Note 4)		15		18		20	ns
t_{CPA}	Access time from column precharge (see Note 4)		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low (see Note 4)		60		70		80	ns
t_{OEA}	Access time from $\overline{OE}$ low (see Note 4)		15		18		20	ns
t_{CLZ}	Delay time, $\overline{xCAS}$ low to output in low-impedance state	0		0		0		ns
t_{OH}	Output data hold time (from $\overline{xCAS}$)	3		3		3		ns
t_{OHO}	Output data hold time (from $\overline{OE}$)	3		3		3		ns
t_{OFF}	Output disable time after $\overline{xCAS}$ high (see Note 5)	0	15	0	18	0	20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 5)	0	15	0	18	0	20	ns

NOTES: 4. Access times for TMS42x160 are measured with output reference levels of V_{OH} = 2 V and V_{OL} = 0.8 V.
5. t_{OFF} and t_{OEZ} are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'4xx160-60 '4xx160P-60		'4xx160-70 '4xx160P-70		'4xx160-80 '4xx160P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, read (see Note 6)	110		130		150		ns
t_{WC}	Cycle time, write (see Note 6)	110		130		150		ns
t_{RWC}	Cycle time, read-write (see Note 6)	155		181		205		ns
t_{PC}	Cycle time, page-mode read or write (see Notes 6 and 7)	40		45		50		ns
t_{PRWC}	Cycle time, page-mode read-write (see Note 6)	85		96		105		ns
t_{RASP}	Pulse duration, $\overline{RAS}$ low, page mode (see Note 8)	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, $\overline{RAS}$ low, nonpage mode (see Note 8)	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{xCAS}$ low (see Note 9)	15	10 000	18	10 000	20	10 000	ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Pulse duration, $\overline{W}$ low	10		10		10		ns
t_{ASC}	Setup time, column address before $\overline{xCAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data (see Note 9)	0		0		0		ns
t_{RCS}	Setup time, $\overline{W}$ high before $\overline{xCAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{xCAS}$ high	15		18		20		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{xCAS}$ low (early-write operation only)	0		0		0		ns
t_{CAH}	Hold time, column address after $\overline{xCAS}$ low	10		15		15		ns
t_{DH}	Hold time, data (see Note 10)	10		15		15		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Hold time, $\overline{W}$ high after $\overline{xCAS}$ high (see Note 11)	0		0		0		ns
t_{RRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ high (see Note 11)	0		0		0		ns
t_{WCH}	Hold time, $\overline{W}$ low after $\overline{xCAS}$ low (early-write operation only)	10		15		15		ns
t_{CLCH}	Hold time, $\overline{xCAS}$ low to $\overline{xCAS}$ high	5		5		5		ns
t_{RHCP}	Hold time, $\overline{RAS}$ high from $\overline{xCAS}$ precharge	35		40		45		ns
t_{OEH}	Hold time, $\overline{OE}$ command	15		18		20		ns
t_{ROH}	Hold time, $\overline{RAS}$ referenced to $\overline{OE}$	10		10		10		ns
t_{CHS}	Hold time, $\overline{xCAS}$ low after $\overline{RAS}$ high (self refresh)	– 50		– 50		– 50		ns
t_{CP}	Delay time, $\overline{xCAS}$ high (precharge)	10		10		10		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (read-write operation only)	55		63		70		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{xCAS}$ high ($\overline{xCBR}$ refresh only)	10		10		10		ns
t_{CRP}	Delay time, $\overline{xCAS}$ high to $\overline{RAS}$ low	5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{xCAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{xCAS}$ low to $\overline{RAS}$ low ($\overline{xCBR}$ refresh only)	5		5		5		ns
t_{CWD}	Delay time, $\overline{xCAS}$ low to $\overline{W}$ low (read-write operation only)	40		46		50		ns
t_{OED}	Delay time, $\overline{OE}$ to data	15		18		20		ns

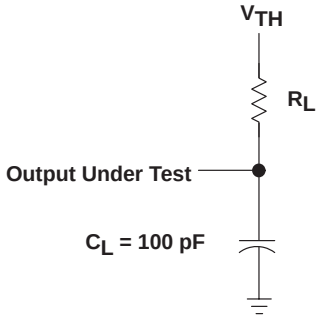
NOTES: 6. All cycle times assume t_T = 5 ns.
7. To assure t_{PC} min, t_{ASC} should be ≥ to t_{CP}.
8. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
9. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
10. Referenced to the later of $\overline{xCAS}$ or $\overline{W}$ in write operations
11. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

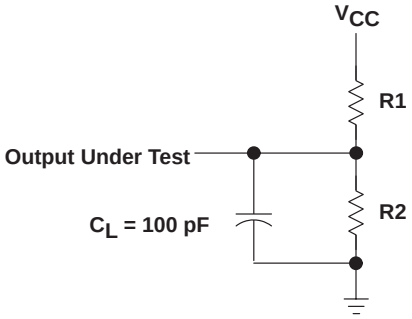
			'4xx160-60 '4xx160P-60		'4xx160-70 '4xx160P-70		'4xx160-80 '4xx160P-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 12)		15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high		30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{xCAS}$ high		30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{xCAS}$ low (see Note 12)		20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{xCAS}$ low		0		0		0		ns
t_{RSH}	Delay time, $\overline{xCAS}$ low to $\overline{RAS}$ high		15		18		20		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-write operation only)		85		98		110		ns
t_{CPW}	Delay time, $\overline{W}$ low after $\overline{xCAS}$ precharge (read-write operation only)		60		68		75		ns
t_{RASS}	Pulse duration, self-refresh entry from $\overline{RAS}$ low		100		100		100		µs
t_{RPS}	Pulse duration, $\overline{RAS}$ precharge after self refresh		110		130		150		ns
t_{REF}	Refresh time interval	'4x6160		64		64		64	ms
		'4x6160P		128		128		128	
		'4x8160		16		16		16	ms
		'4x8160P		128		128		128	
t_T	Transition time		3	30	3	30	3	30	ns

NOTE 12: The maximum value is specified only to assure access time.

PARAMETER MEASUREMENT INFORMATION



(a) LOAD CIRCUIT

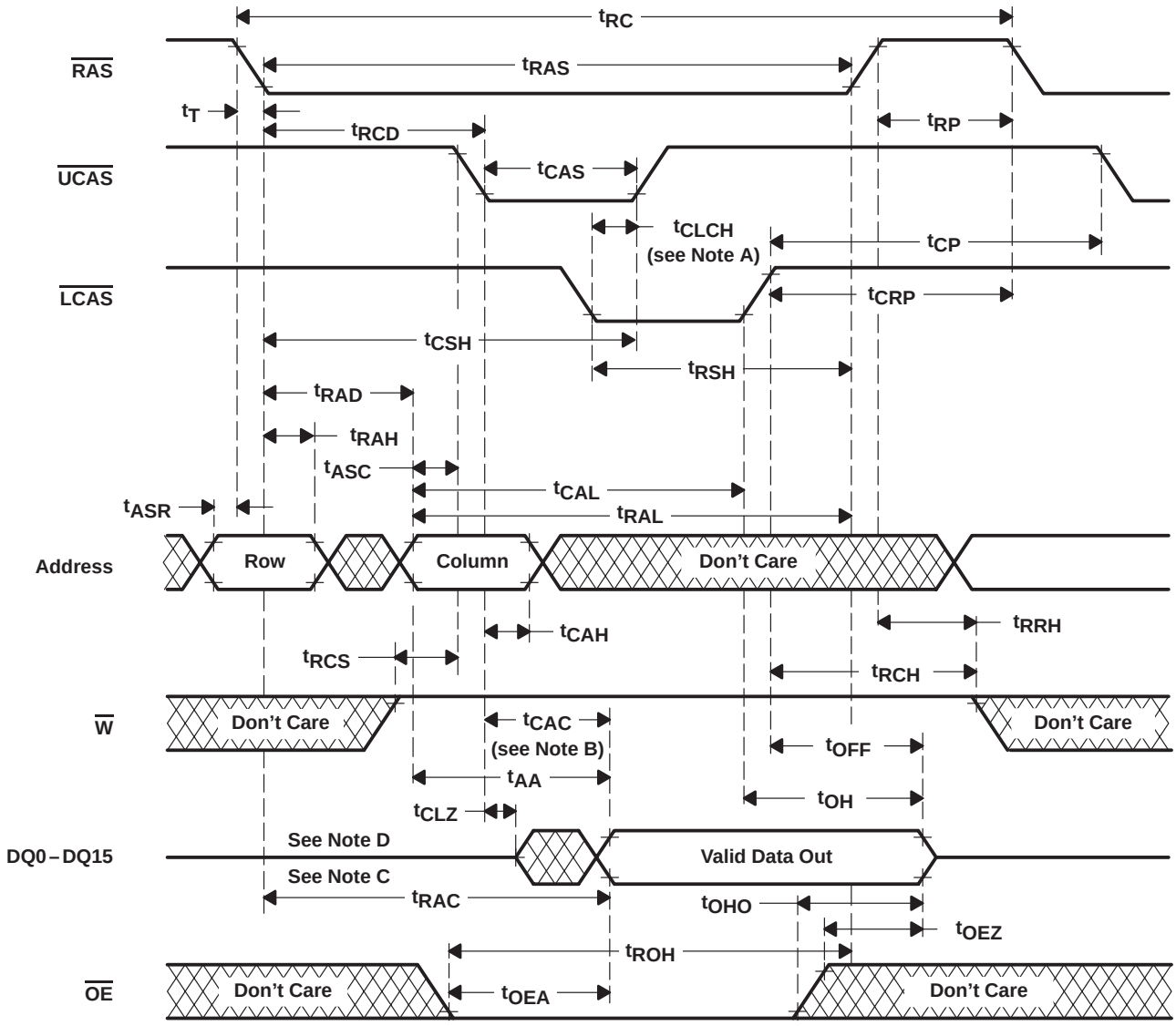


(b) ALTERNATE LOAD CIRCUIT

DEVICE	V_{CC} (V)	R1 (Ω)	R2 (Ω)	V_{TH} (V)	R_L (Ω)
41x160/P	5	828	295	1.31	218
42x160/P	3.3	1178	868	1.4	500

Figure 1. Load Circuits for Timing Parameters

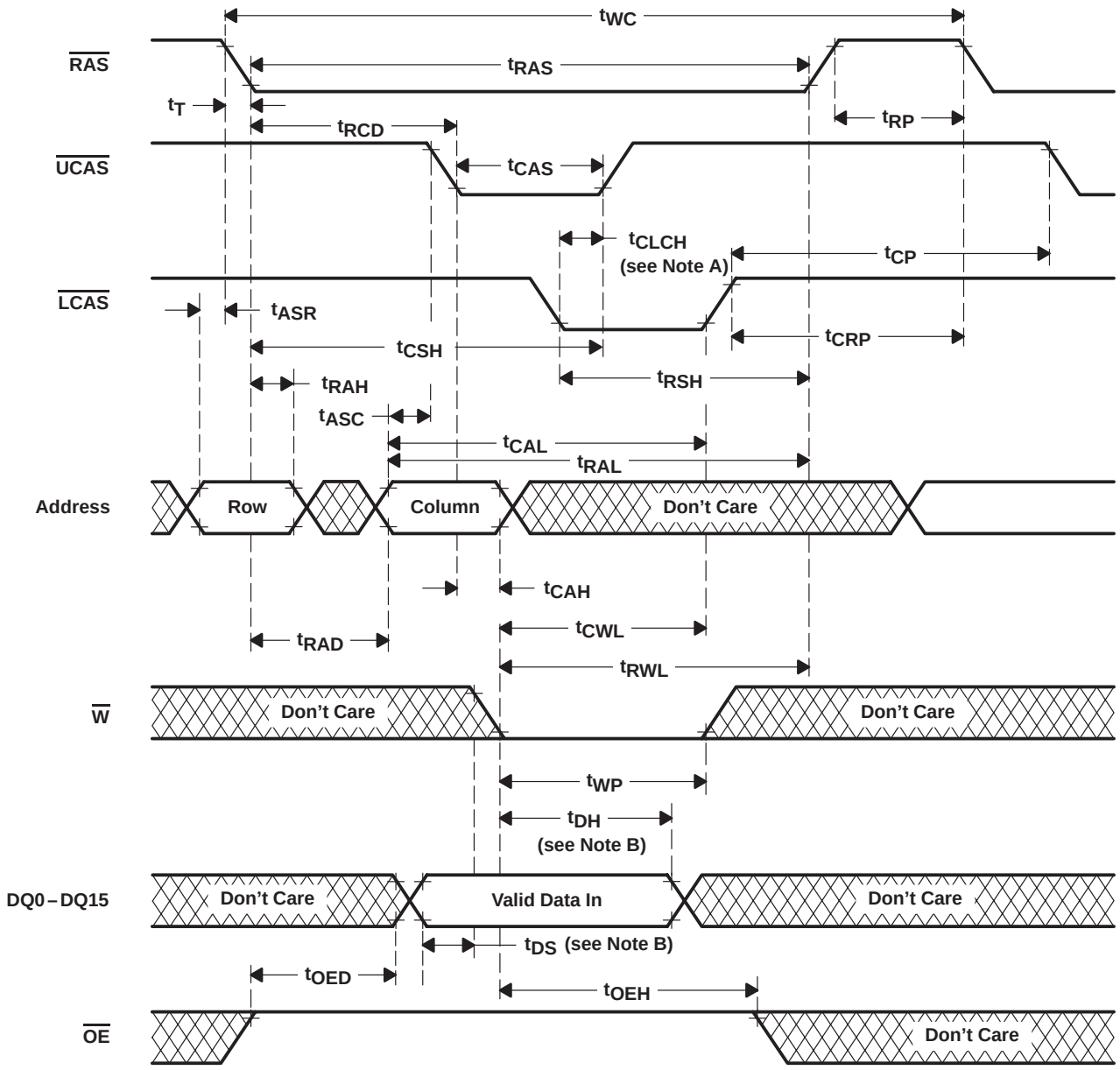
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{\text{xCAS}}$ to its corresponding DQx.
C. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
D. $\overline{\text{xCAS}}$ order is arbitrary.

Figure 2. Read-Cycle Timing

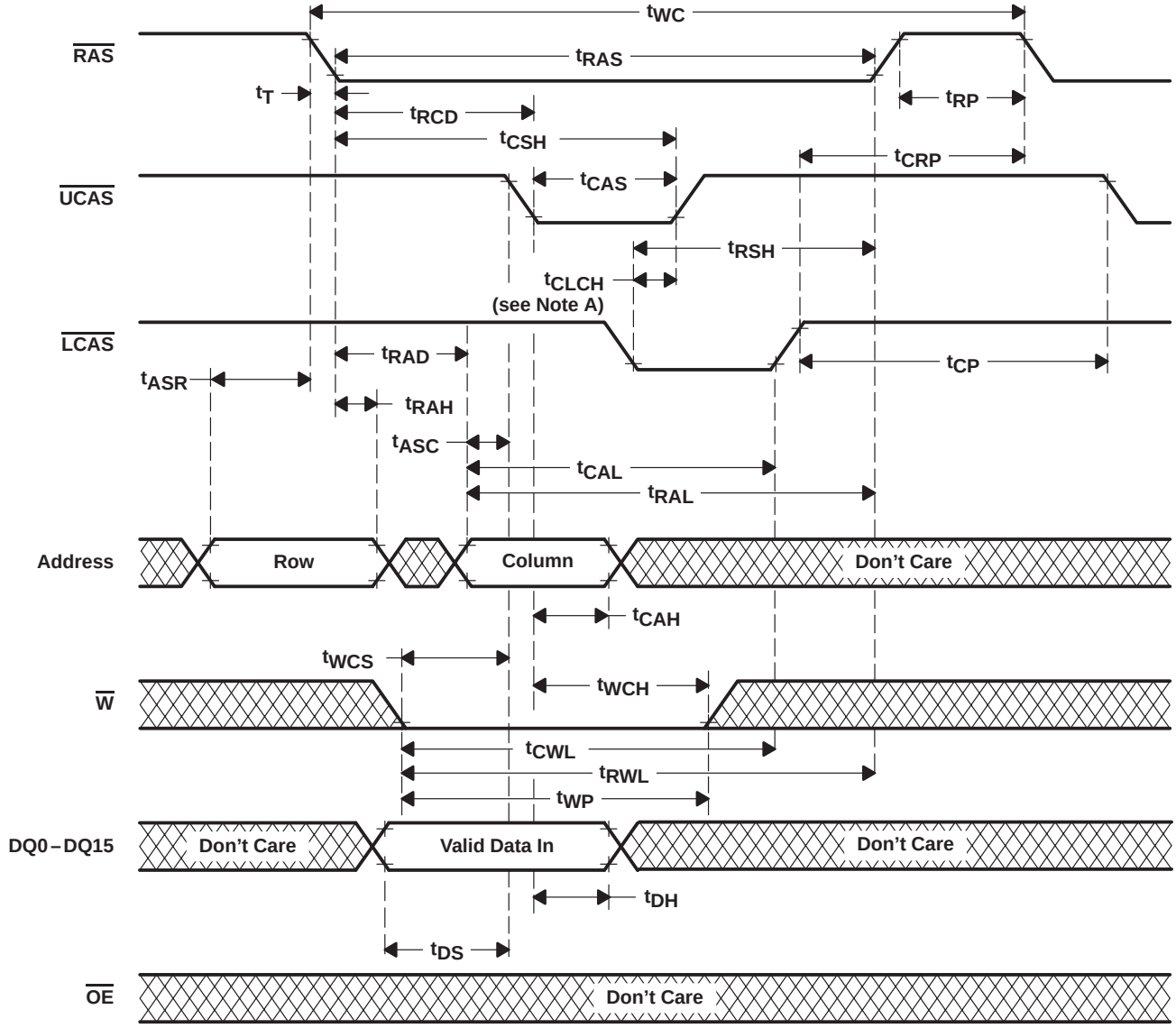
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. Referenced to the first $\overline{xCAS}$ or $\overline{W}$, whichever occurs last
C. $\overline{xCAS}$ order is arbitrary.

Figure 3. Write-Cycle Timing

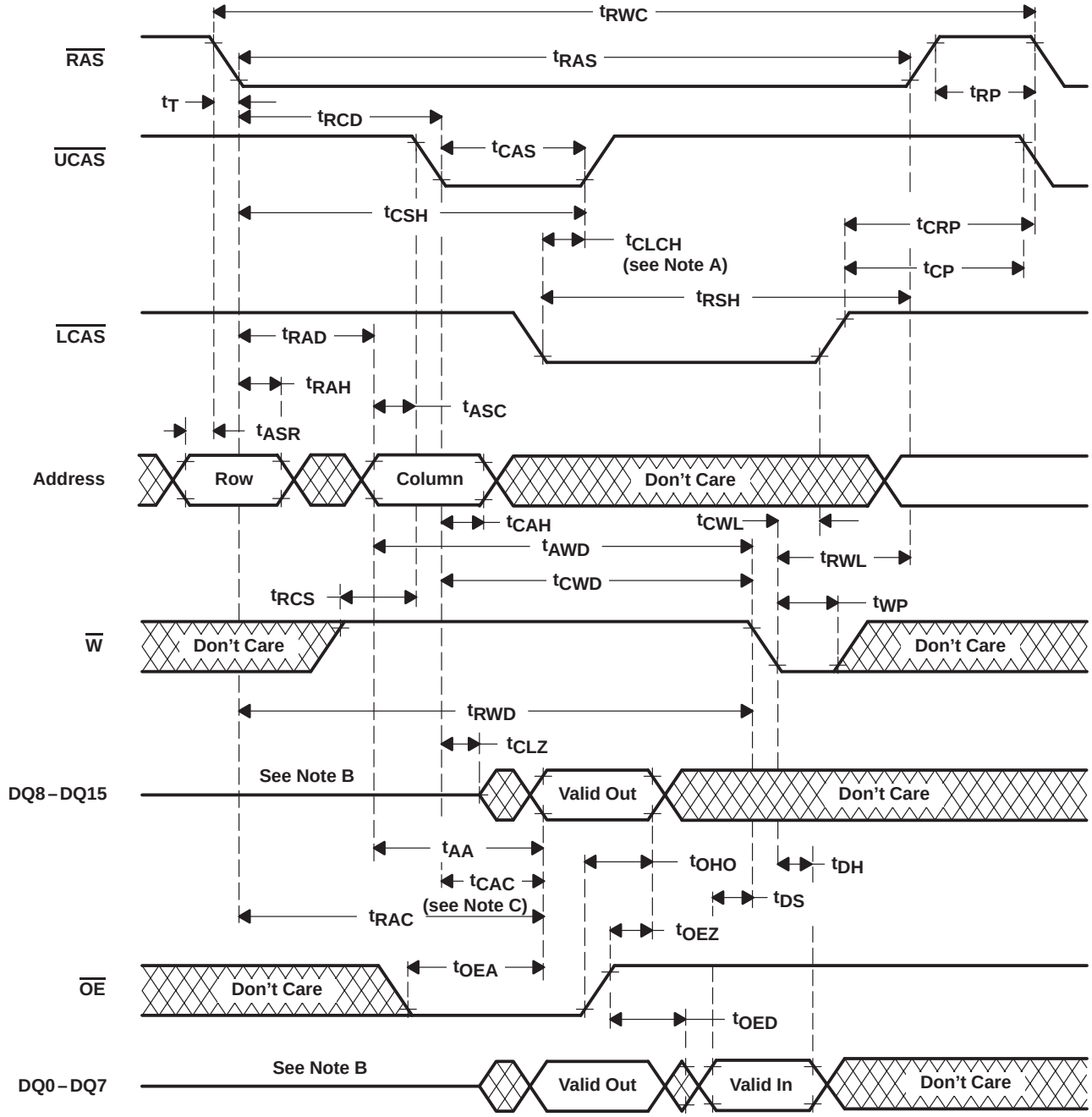
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. $\overline{\text{xCAS}}$ order is arbitrary.

Figure 4. Early-Write-Cycle Timing

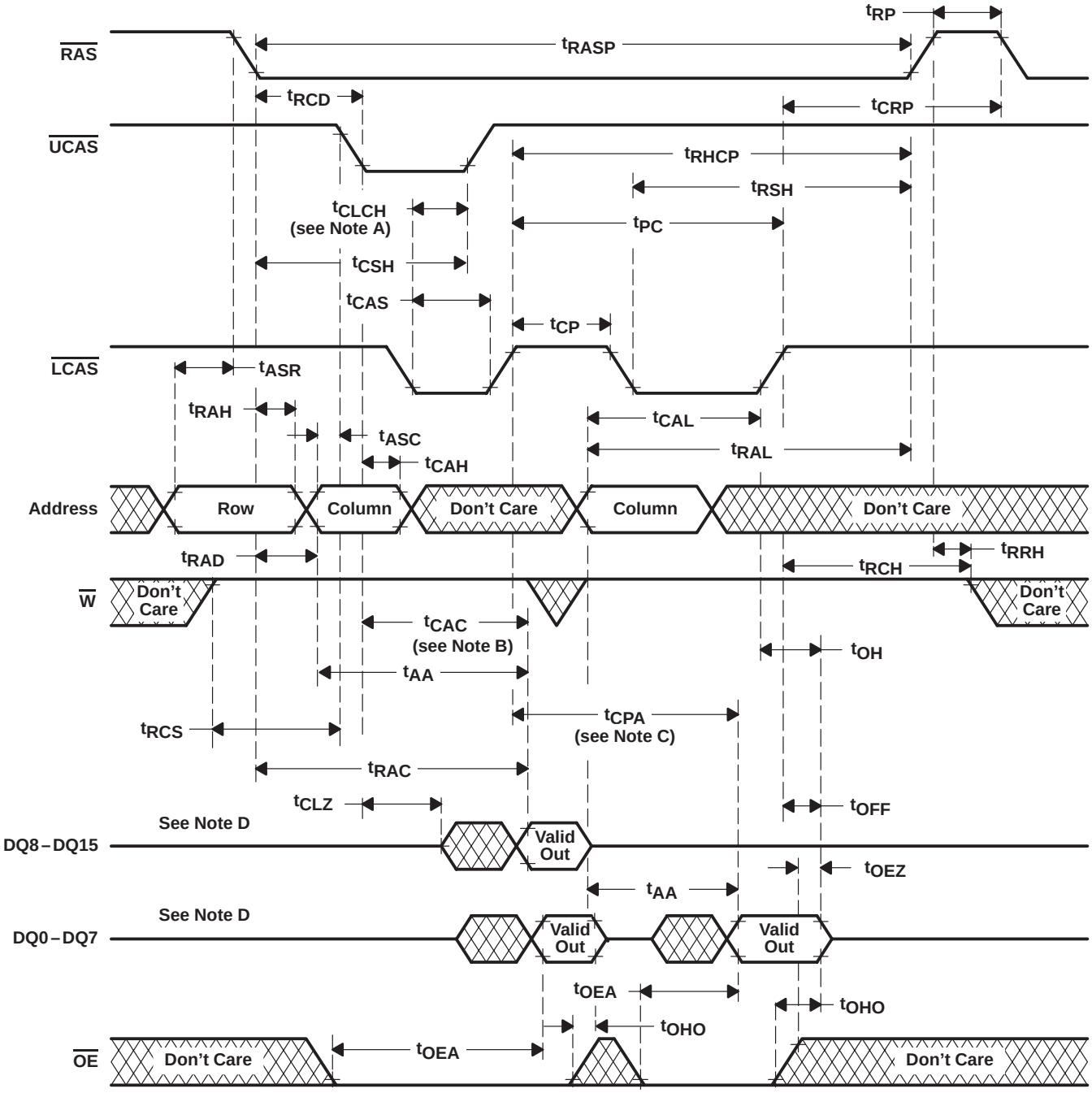
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first xCAS going low, the parameter t_{CLCH} must be met.
B. Output can go from a the high-impedance state to an invalid-data state prior to the specified access time.
C. t_{CAC} is measured from xCAS to its corresponding DQx.
D. xCAS order is arbitrary.

Figure 5. Read-Modify-Write-Cycle Timing

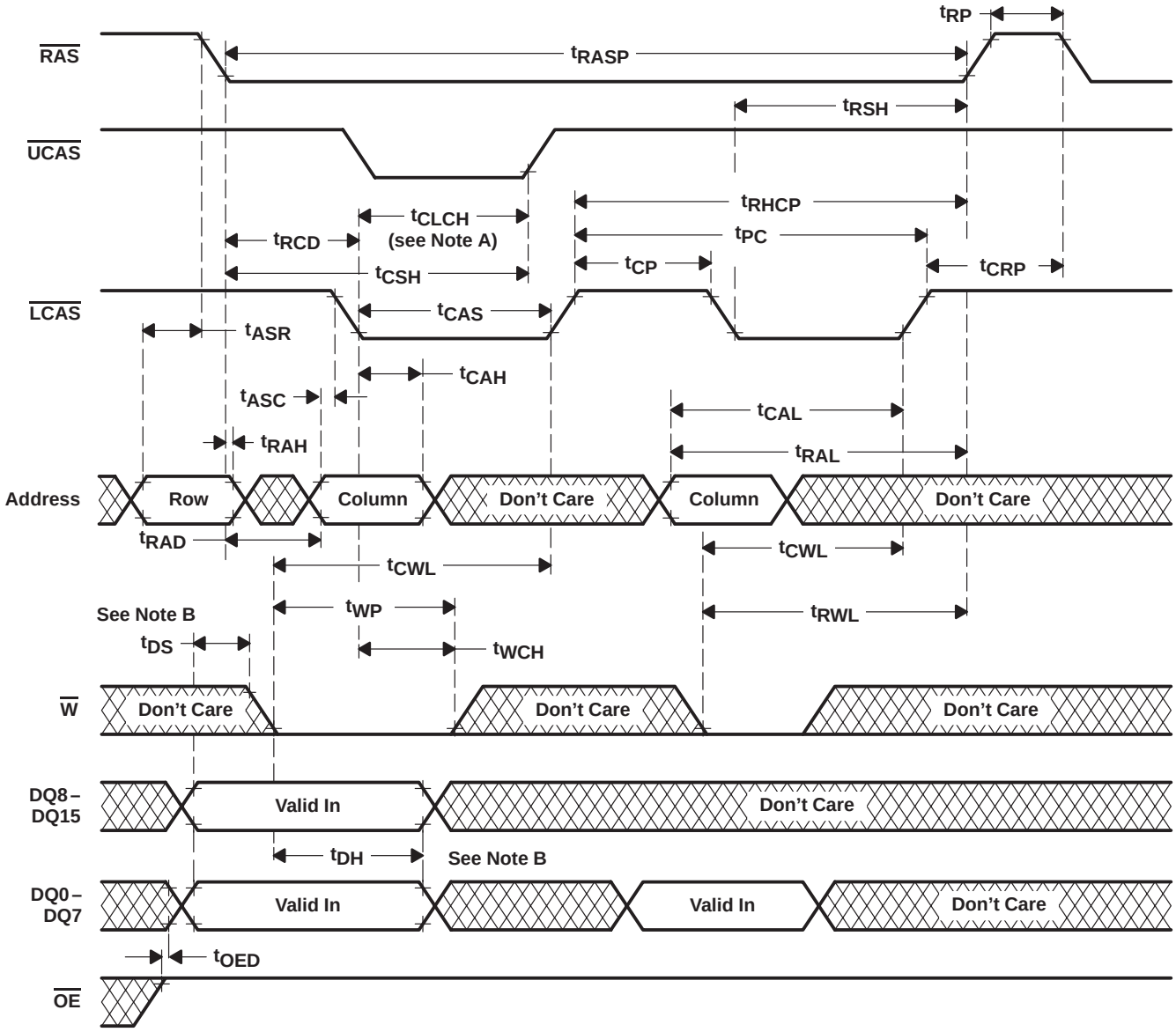
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{\text{xCAS}}$ to its corresponding DQx.
C. Access time is t_{CPA} or t_{AA} dependent.
D. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
E. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write- and read-modify-write-timing specifications are not violated.
F. $\overline{\text{xCAS}}$ order is arbitrary.

Figure 6. Enhanced-Page-Mode Read-Cycle Timing

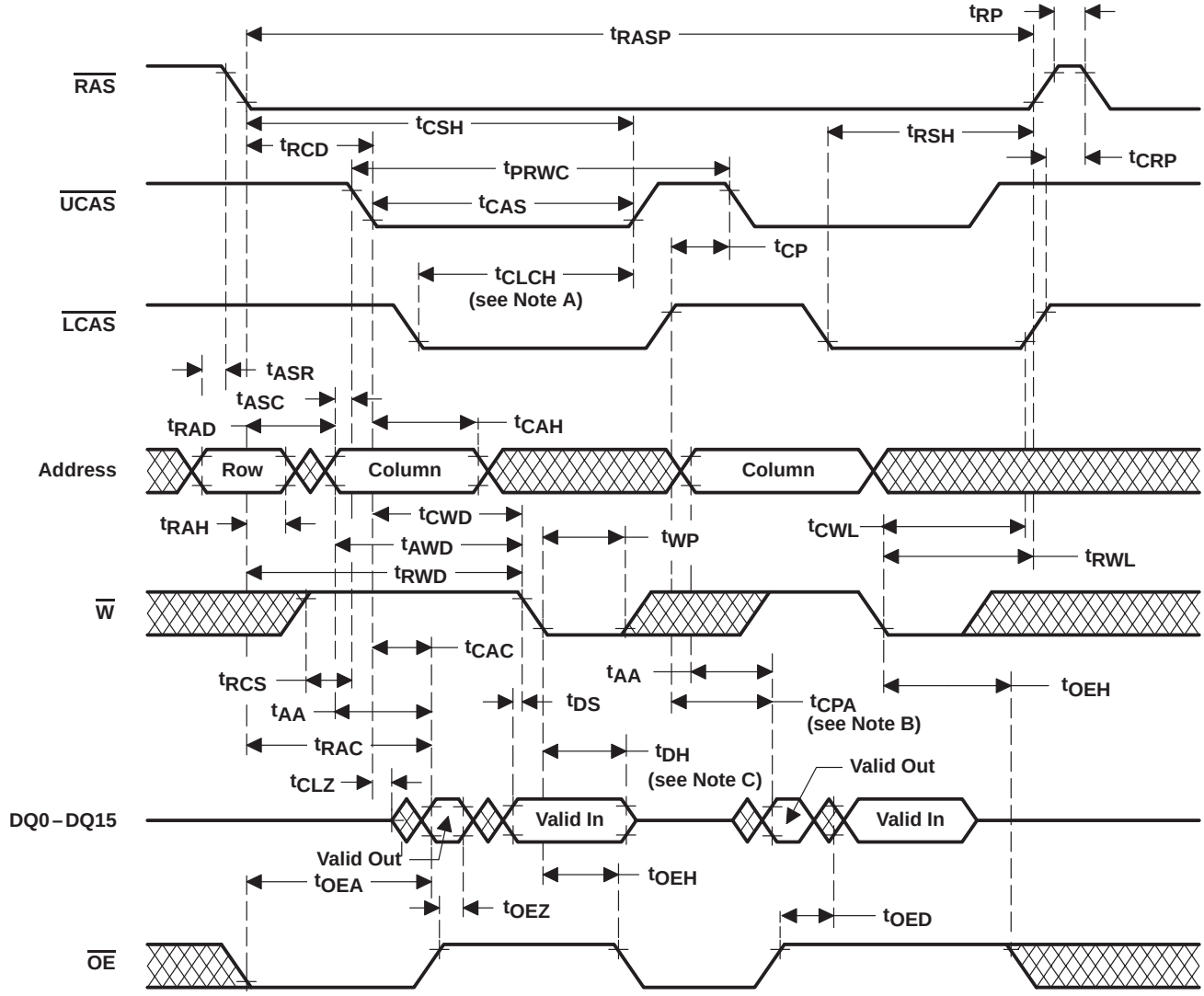
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first xCAS going low, the parameter t_{CLCH} must be met.
B. Referenced to the first xCAS or W, whichever occurs last
C. A read cycle or read-modify-write cycle can be mixed with the write cycles as long as the read- and read-modify-write-timing specifications are not violated.
D. xCAS order is arbitrary.

Figure 7. Enhanced-Page-Mode Write-Cycle Timing

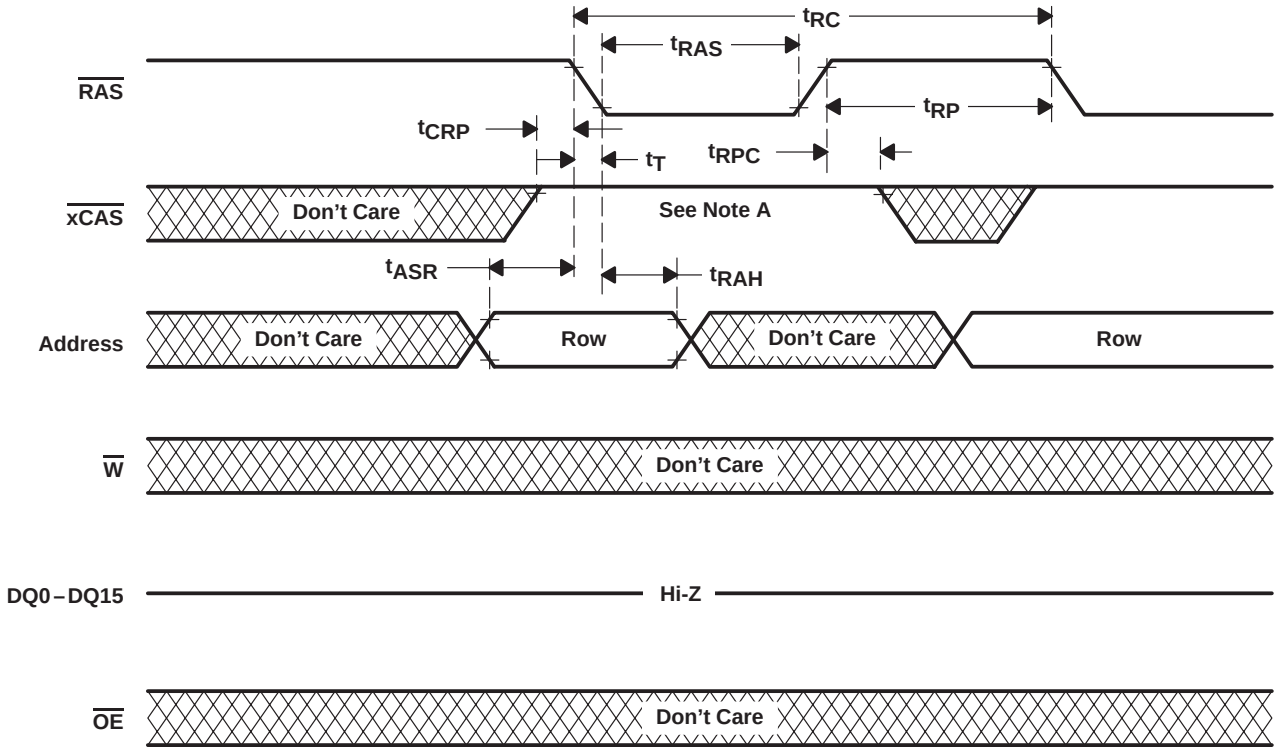
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. Access time is t_{CPA} or t_{AA} dependent.
C. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
D. xCAS order is arbitrary.
E. A read or write cycle can be intermixed with read-modify-write cycles as long as the read- and write-cycle timing specifications are not violated.
F. t_{CAC} is measured from $\overline{\text{xCAS}}$ to its corresponding DQx.

Figure 8. Enhanced-Page-Mode Read-Modify-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: All xCAS must be high.

Figure 9. RAS-Only Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

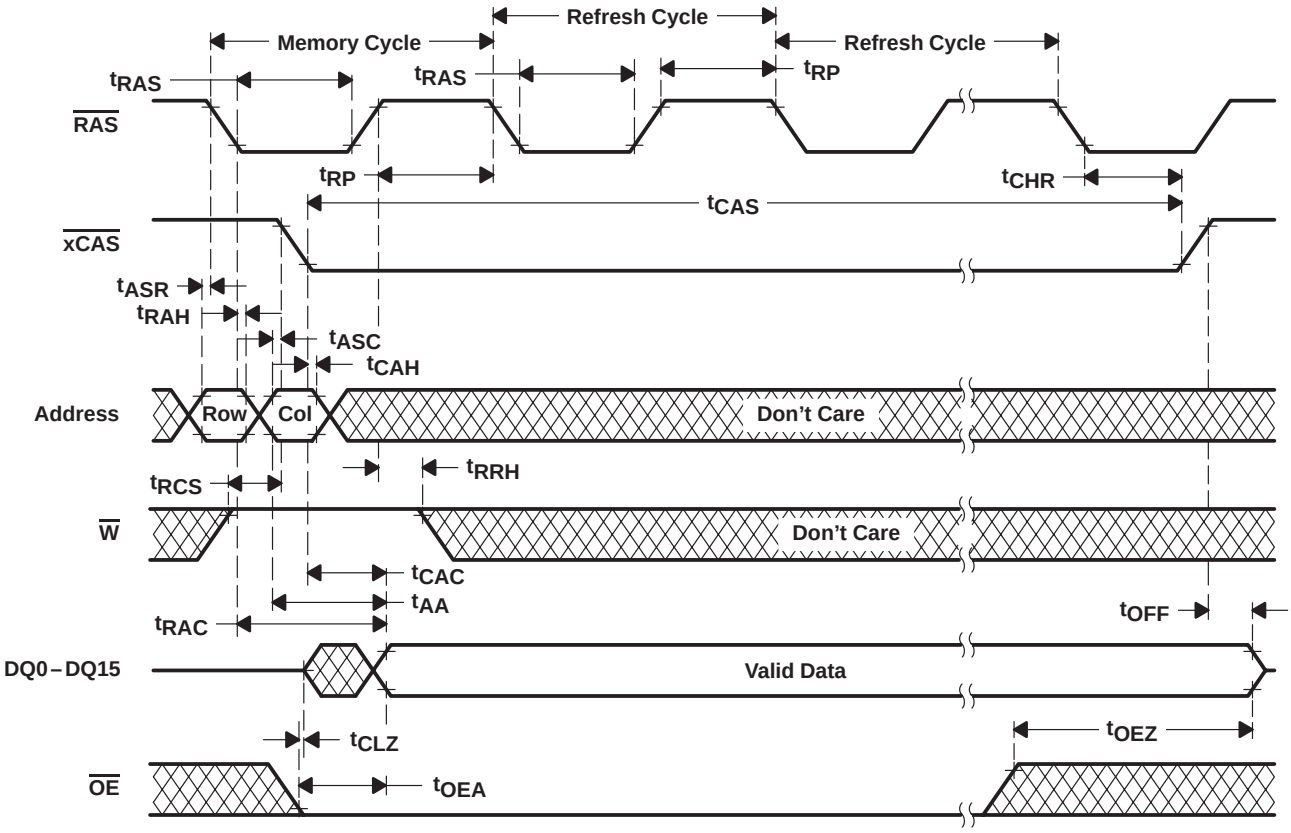
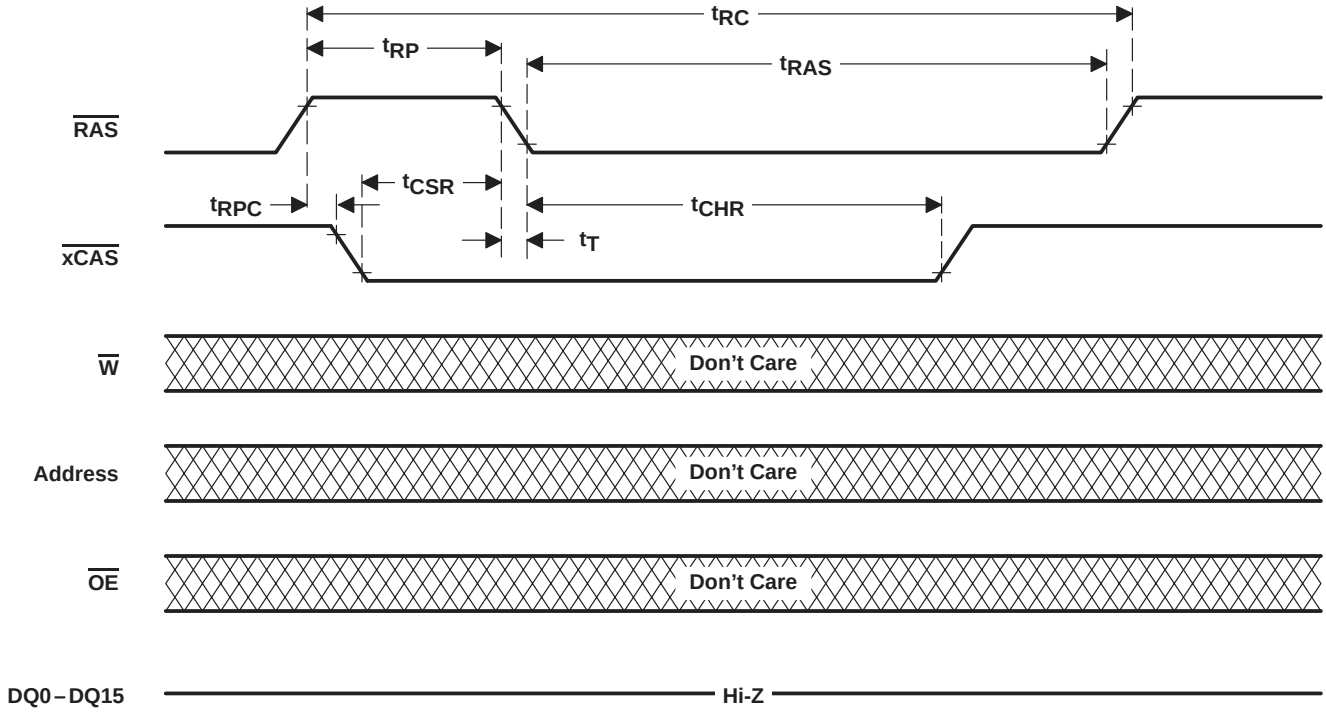


Figure 10. Hidden-Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: Any $\overline{\text{xCAS}}$ can be used.

Figure 11. Automatic-CBR-Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

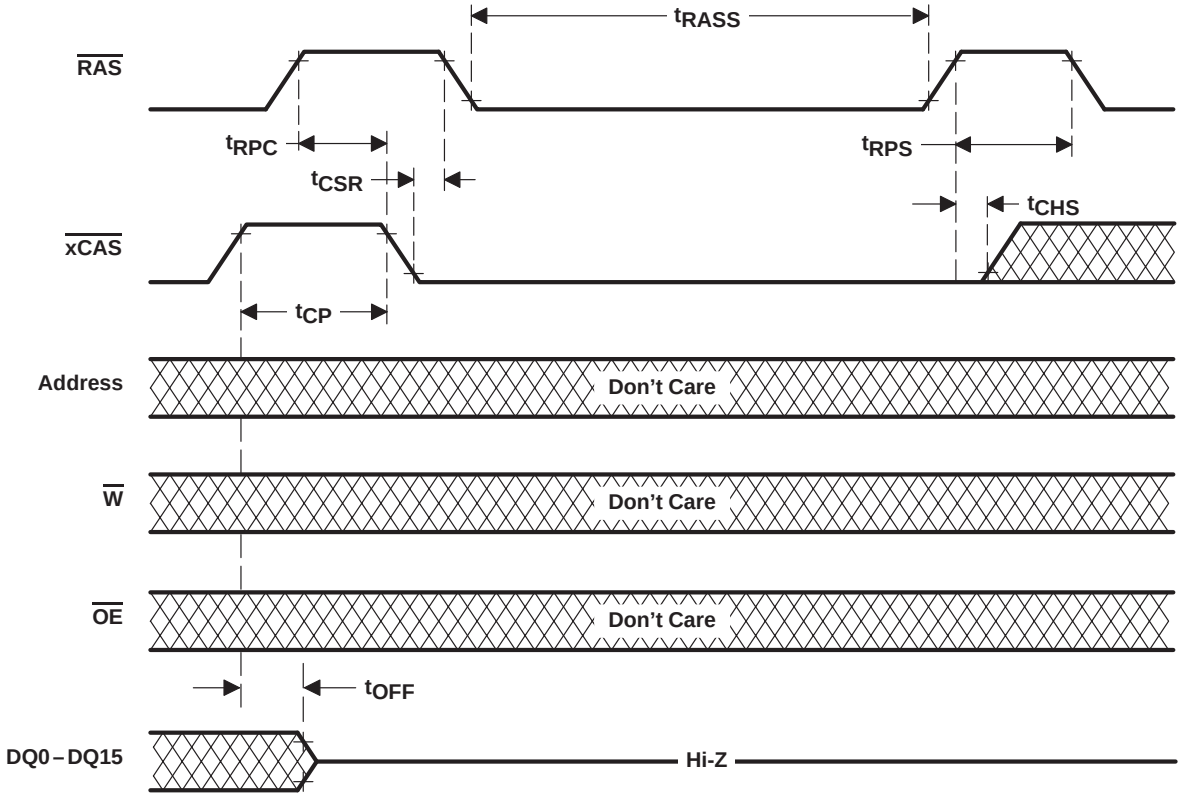
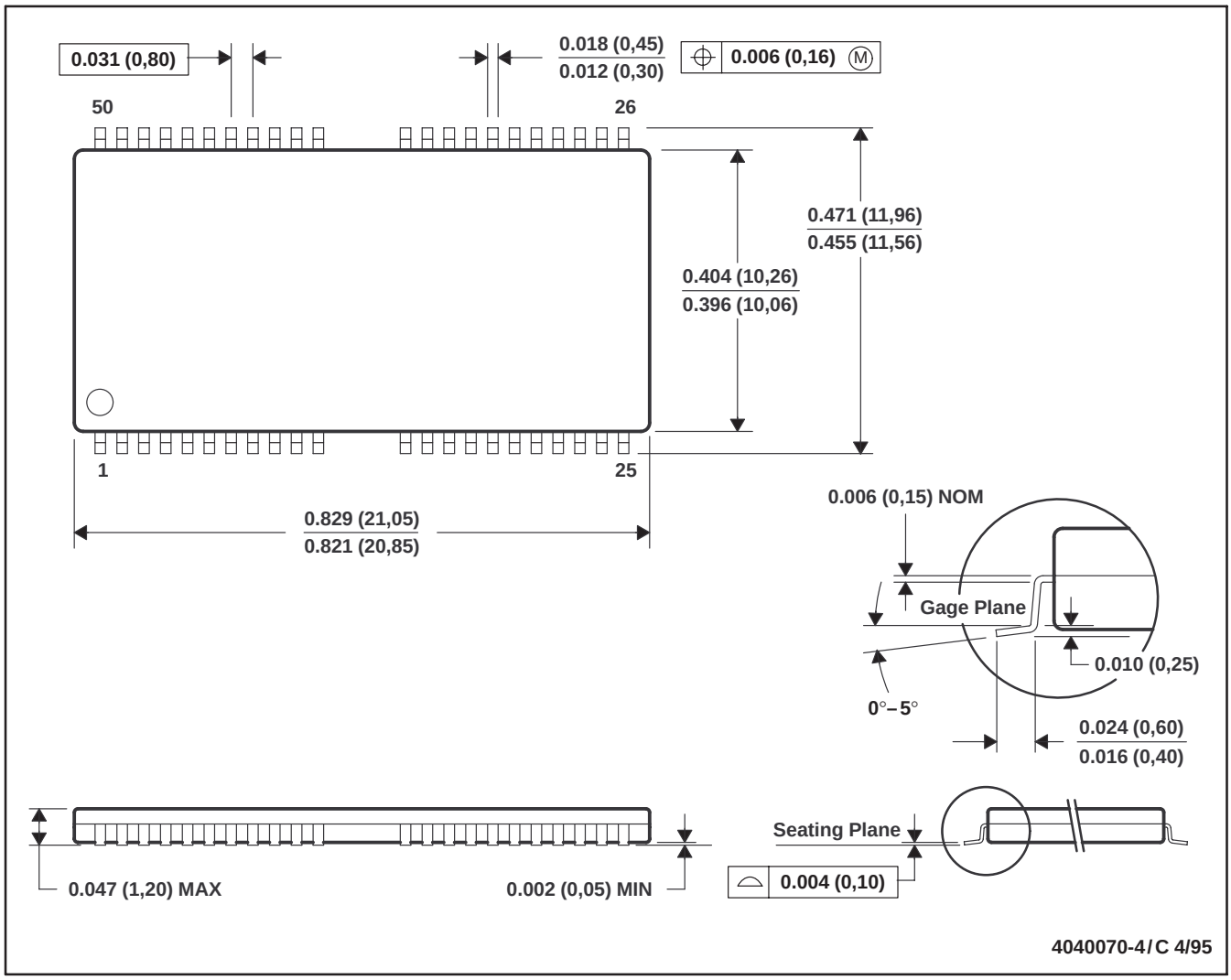


Figure 12. Self-Refresh-Cycle Timing

MECHANICAL DATA

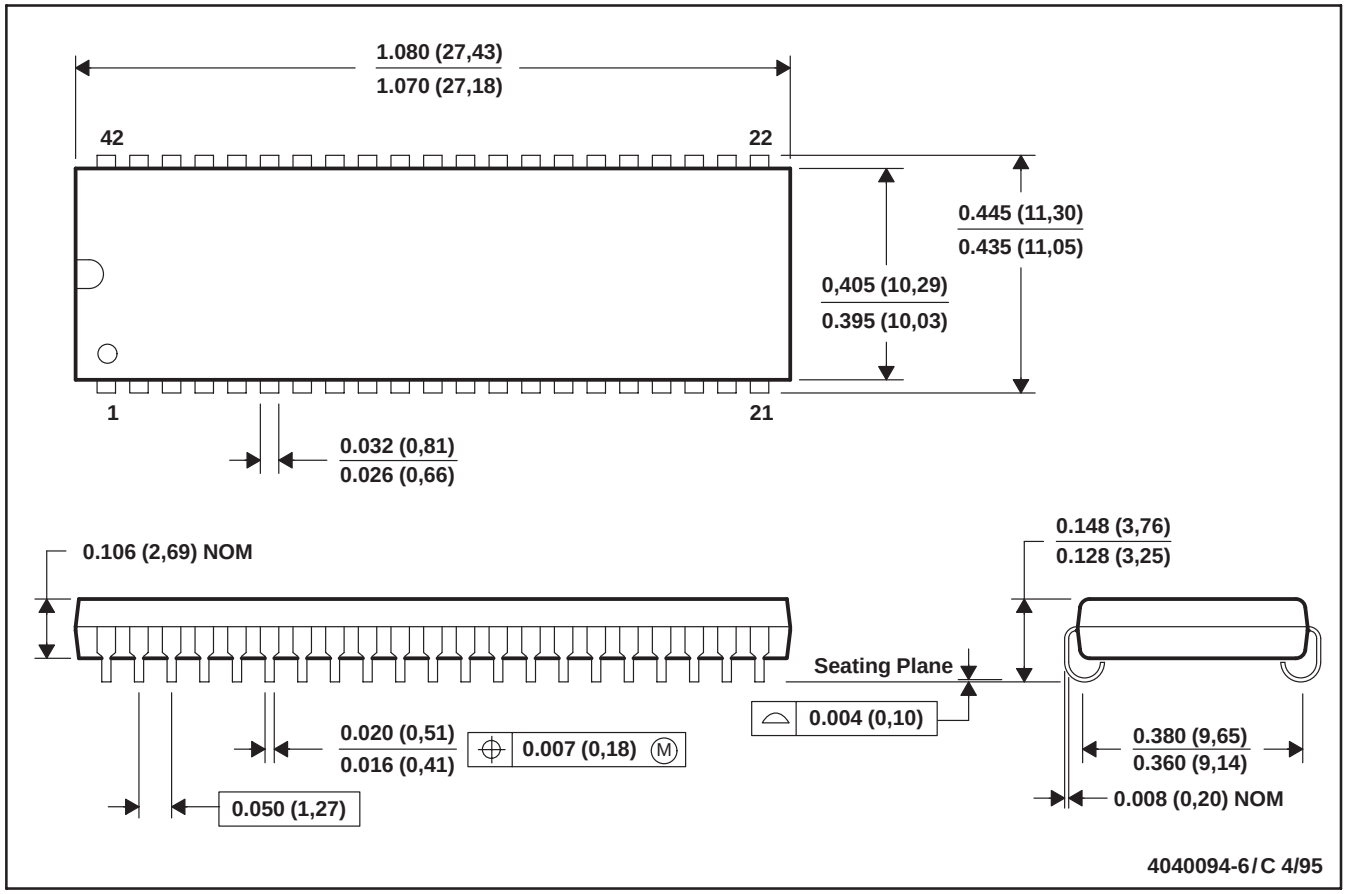
DGE (R-PDSO-G44/50) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.

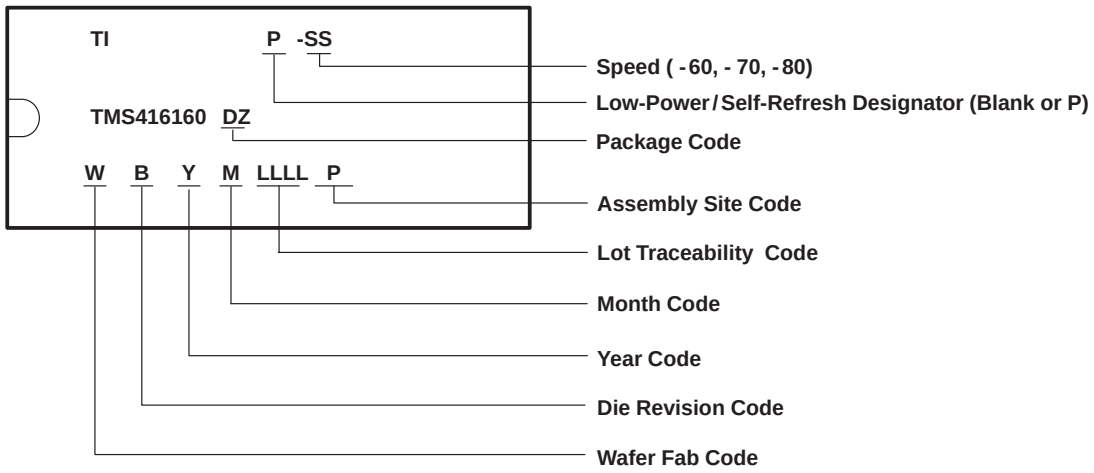
MECHANICAL DATA

DZ (R-PDSO-J42) **PLASTIC SMALL-OUTLINE J-LEAD PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0.005 (0,125).

device symbolization (TMS416160P illustrated)



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