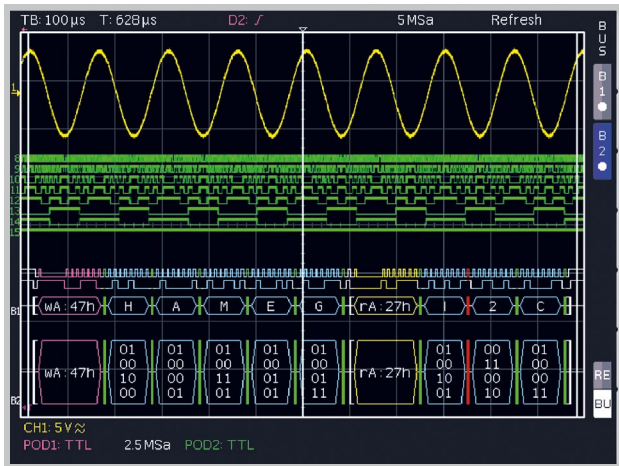
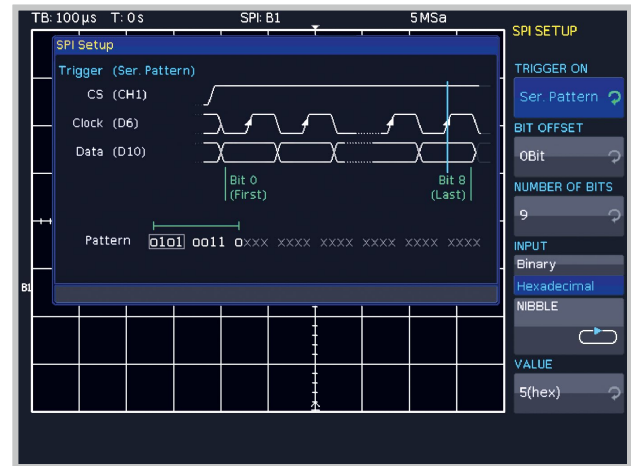


H0010 Serial Bus

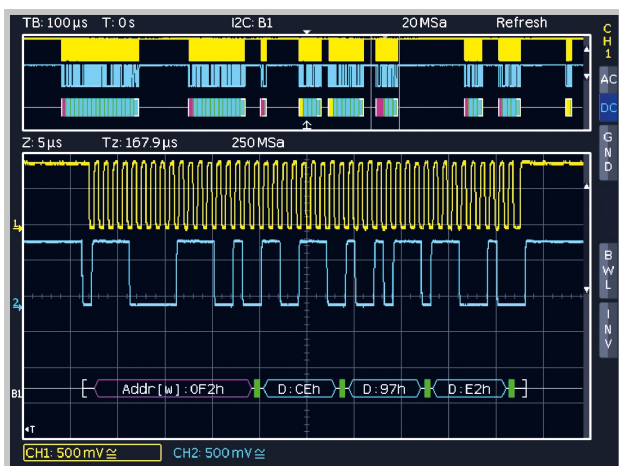
for all Oscilloscopes of the HMO Series



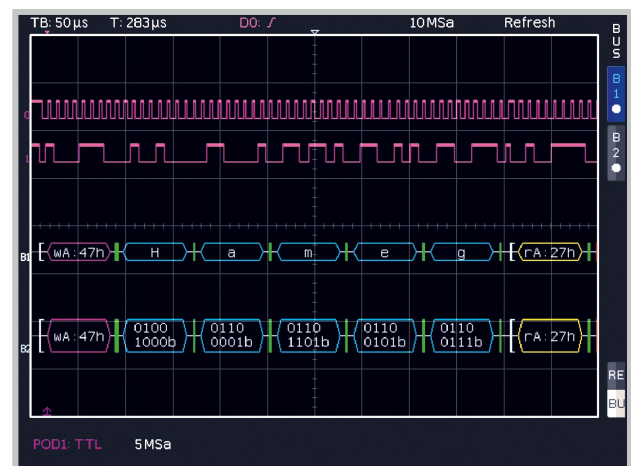
Mixed Signal and Bus Display



SPI Bus Trigger Setup



I²C Bus Hex decoding on the Analog Channel



I²C Bus ASCII and Binary

- ✓ Via Analog Channels and/or Logic Channels
- ✓ I²C, SPI, UART/RS-232 Bus Trigger and Decode
- ✓ Hardware accelerated Decode in Real Time
- ✓ Color Coded Display of the Content for intuitive Analysis and easy Overview
- ✓ More Details of the decoded Values become visible with increasing Zoom Factor
- ✓ Bus Display with synchronous Display of the Data and, if selected, Clock Signal
- ✓ Decode into ASCII, Binary, Hexadecimal or Decimal Format
- ✓ Up to four Lines to comfortably show the decoded Values
- ✓ Powerful Trigger to isolate specific Messages
- ✓ Option for all Oscilloscopes of the HMO Series, retrofittable

H0010 I²C, SPI, UART/RS-232 Bus Analysis

I ² C Bus		SPI Bus		UART/RS-232 Bus	
Bus Configuration					
Bit/Baud rate	up to 10 Mbit/s (HMO352x/2524), up to 5 Mbit/s (HMO72x...202x)	up to 25 Mbit/s (HMO352x/2524), up to 12.5 Mbit/s (HMO72x...202x)		300, 600, 1,200, 2,400, 4,800, 9,600, 19,200, 38,400, 57,600, 115,200 Baud, up to 62.5 Mbit/s (HMO352x/2524), up to 31 Mbit/s (HMO72x...202x)	
Number of Bit's	7 or 10 Bit for Address ID 8 Bit for Data	32 Bit for Data		8 Bit for Data 1, 1.5, 2 Bit for Stop Bit	
Polarity	n/a	Chip Select, positive or negative, or without Chip Select (2-wire SPI) Clock rising or falling edge Data High or Low active		High or Low active	
Parity	n/a	n/a		none, odd or even	
Trigger					
Source	digital Channels LCH 0...15 (Opt. H03508) analog Channels CH 1...2 [CH 1...4]	digital Channels LCH 0...15 (Opt. H03508) analog Channels CH 1...2, external Trigger Entry for Chip Select, [CH 1...4]		digital Channels LCH 0...15 (Opt. H03508) analog Channels CH 1...2 [CH 1...4]	
Event	7 or 10 Bit Address ID 7 or 10 Bit Address ID with 8 Bit Data Start, Stop, Restart missing Acknowledge Address ID without Acknowledge	Data packets up to 32 Bit with positive or negative Chip Select or without Chip Select, (2-wire SPI)		Data packets up to 8 Bit	
Input format	Hexadecimal or Binary	Hexadecimal or Binary		Hexadecimal or Binary	
Hardware accelerated Decode					
Source	digital Channels LCH 0...15 (Opt. H03508) analog Channels CH 1...2 [CH 1...4]	digital Channels LCH 0...15 (Opt. H03508) analog Channels CH 1...2, external Trigger Entry for Chip Select, [CH 1...4]		digital Channels LCH 0...15 (Opt. H03508) analog Channels CH 1...2 [CH 1...4]	
Display	Bus display, color coded for Read Address ID: Yellow Write Address ID: Magenta Data: Cyan Start: White Stop: White ACK/NACK: Green/Red Error: Red Trigger Condition: Green up to four lines for decoded values, synchronous display of the Bit lines	Bus display, color coded for Data: Cyan Start: White Stop: White Error: Red Trigger Condition: Green up to four lines for decoded values, synchronous display of the Bit lines		Bus display, color coded for Data: Cyan Start: White Stop: White Error: Red Trigger Condition: Green up to four lines for decoded values, synchronous display of the Bit lines	
Format	Address ID: hexadecimal Data: ASCII, binary, decimal, hexadecimal	n/a Data: ASCII, binary, decimal, hexadecimal		n/a Data: ASCII, binary, decimal, hexadecimal	