

## 12 Output Buffer for 2 DDR and 3 SDRAM DIMMS

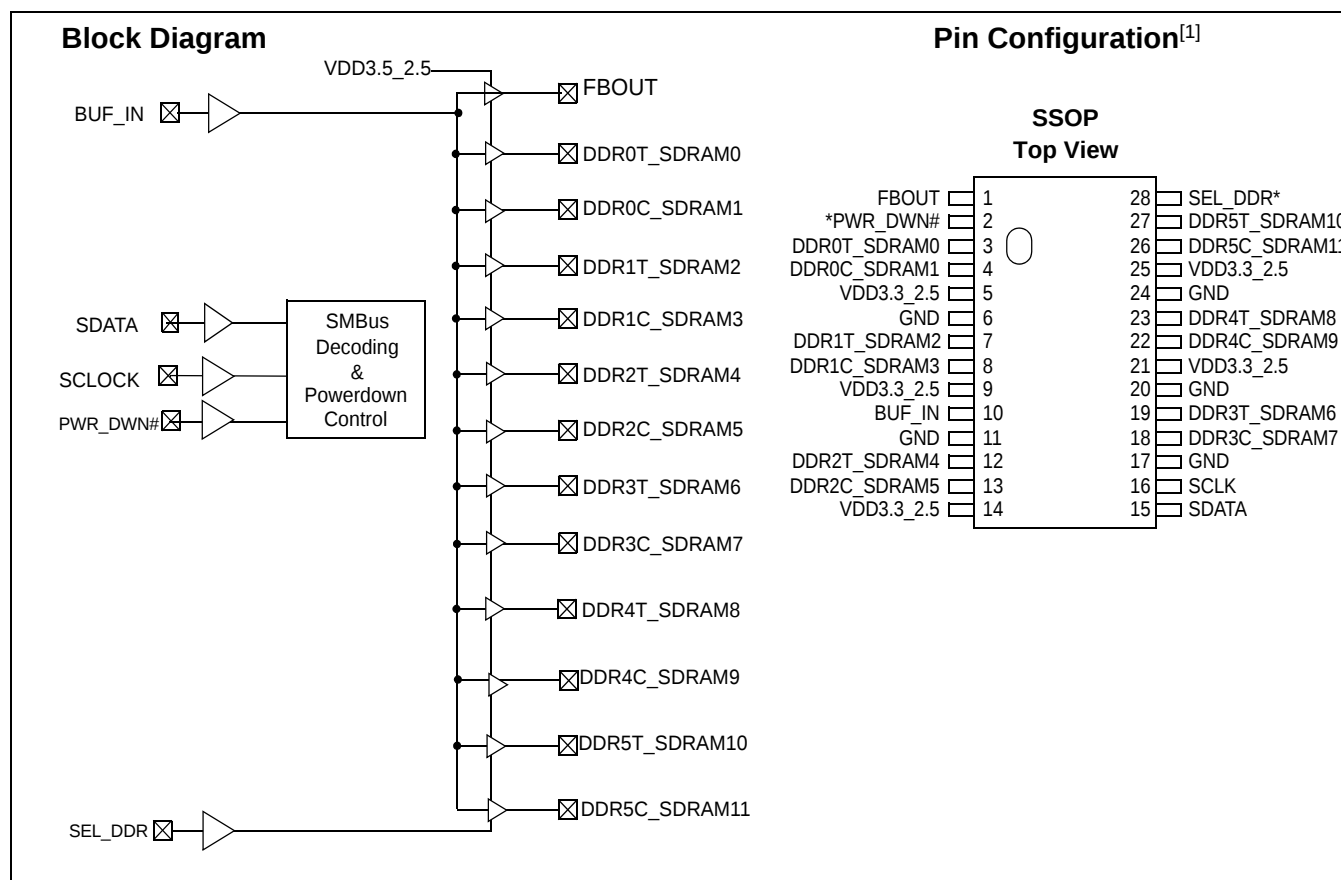
### Features

- One input to 12 output buffer/drivers
- Supports up to 2 DDR DIMMs or 3 SDRAM DIMMS
- One additional output for feedback
- SMBus interface for individual output control
- Low skew outputs (< 100 ps)
- Supports 266 MHz and 333 MHz DDR SDRAM
- Dedicated pin for power management support
- Space-saving 28-pin SSOP package

### Functional Description

The W256 is a 3.3V/2.5V buffer designed to distribute high-speed clocks in PC applications. The part has 12 outputs. Designers can configure these outputs to support 3 unbuffered standard SDRAM DIMMs and 2 DDR DIMMs. The W256 can be used in conjunction with the W250-02 or similar clock synthesizer for the VIA Pro 266 chipset.

The W256 also includes an SMBus interface which can enable or disable each output clock. On power-up, all output clocks are enabled (internal pull-up).



#### Note:

1. Internal 100K pull-up resistors present on inputs marked with \*. Design should not rely solely on internal pull-up resistor to set I/O pins HIGH.

**Pin Summary**

| Name                               | Pins                 | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|------------------------------------|----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SEL_DDR                            | 28                   | <b>Input to configure for DDR-ONLY mode or STANDARD SDRAM mode.</b><br>1 = DDR-ONLY mode.<br>0 = STANDARD SDRAM mode.<br>When SEL_DDR is pulled HIGH or configured for DDR-ONLY mode, all the buffers will be configured as DDR outputs.<br>Connect VDD3.3_2.5 to a 2.5V power supply in DDR-ONLY mode.<br>When SEL_DDR is pulled LOW or configured for STANDARD SDRAM output, all the buffers will be configured as STANDARD SDRAM outputs.<br>Connect VDD3.3_2.5 to a 3.3V power supply in STANDARD SDRAM mode. |
| SCLK                               | 16                   | <b>SMBus clock input.</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| SDATA                              | 15                   | <b>SMBus data input.</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| BUF_IN                             | 10                   | <b>Reference input from chipset.</b> 2.5V input for DDR-ONLY mode; 3.3V input for STANDARD SDRAM mode.                                                                                                                                                                                                                                                                                                                                                                                                            |
| FBOUT                              | 1                    | <b>Feedback clock for chipset.</b> Output voltage depends on VDD3.3_2.5V.                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| PWR_DWN#                           | 2                    | <b>Active LOW input to enable Power Down mode; all outputs will be pulled LOW.</b>                                                                                                                                                                                                                                                                                                                                                                                                                                |
| DDR[0:5]T_SDRAM<br>[0,2,4,6,8,10]  | 3, 7, 12, 19, 23, 27 | <b>Clock outputs.</b> These outputs provide copies of BUF_IN. Voltage swing depends on VDD3.3_2.5 power supply.                                                                                                                                                                                                                                                                                                                                                                                                   |
| DDR[0:5]C_SDRAM<br>[1,3,5,7,9, 11] | 4, 8, 13, 18, 22, 26 | <b>Clock outputs.</b> These outputs provide complementary copies of BUF_IN when SEL_DDR is active. These outputs provide copies of BUF_IN when SEL_DDR is inactive. Voltage swing depends on VDD3.3_2.5 power supply.                                                                                                                                                                                                                                                                                             |
| VDD3.3_2.5                         | 5, 9, 14, 21, 25     | <b>Connect to 2.5V power supply when W256 is configured for DDR-ONLY mode.</b><br>Connect to 3.3V power supply, when W256 is configured for standard SDRAM mode.                                                                                                                                                                                                                                                                                                                                                  |
| GND                                | 6, 11, 17, 20, 24    | <b>Ground.</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |

## Serial Configuration Map

- The Serial bits will be read by the clock driver in the following order:
  - Byte 0 — Bits 7, 6, 5, 4, 3, 2, 1, 0
  - Byte 1 — Bits 7, 6, 5, 4, 3, 2, 1, 0
  - ...
  - Byte N — Bits 7, 6, 5, 4, 3, 2, 1, 0
- Reserved and unused bits should be programmed to "0".
- SMBus Address for the W256 is:

**Table 1.**

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W |
|----|----|----|----|----|----|----|-----|
| 1  | 1  | 0  | 1  | 0  | 0  | 1  | —   |

## Byte 6: Outputs Active/Inactive Register (1 = Active, 0 = Inactive), Default = Active

| Bit   | Pin #  | Description                       | Default |
|-------|--------|-----------------------------------|---------|
| Bit 7 | —      | Reserved, drive to 0              | 0       |
| Bit 6 | —      | Reserved, drive to 0              | 0       |
| Bit 5 | —      | Reserved, drive to 0              | 0       |
| Bit 4 | 1      | FBOU                              | 1       |
| Bit 3 | 27, 26 | DDR5T_SDRAM10, DDR5C_S-<br>DRAM11 | 1       |
| Bit 2 | —      | Reserved, drive to 0              | 1       |
| Bit 1 | 23, 22 | DDR4T_SDRAM8, DDR4C_S-<br>DRAM9   | 1       |
| Bit 0 | —      | Reserved, drive to 0              | 1       |

## Byte 7: Outputs Active/Inactive Register (1 = Active, 0 = Inactive), Default = Active

| Bit   | Pin #  | Description                   | Default |
|-------|--------|-------------------------------|---------|
| Bit 7 | —      | Reserved, drive to 0          | 1       |
| Bit 6 | 19, 18 | DDR3T_SDRAM6,<br>DDR3C_SDRAM7 | 1       |
| Bit 5 | 12, 13 | DDR2T_SDRAM4,<br>DDR2C_SDRAM5 | 1       |
| Bit 4 | —      | Reserved, drive to 0          | 1       |
| Bit 3 | —      | Reserved, drive to 0          | 1       |
| Bit 2 | 7, 8   | DDR1T_SDRAM2,<br>DDR1C_SDRAM3 | 1       |
| Bit 1 | —      | Reserved, drive to 0          | 1       |
| Bit 0 | 3, 4   | DDR0T_SDRAM0,<br>DDR0C_SDRAM1 | 1       |

## Maximum Ratings

Supply Voltage to Ground Potential .....–0.5 to +7.0V  
 DC Input Voltage (except BUF\_IN) ..... –0.5V to  $V_{DD}+0.5$   
 Storage Temperature ..... –65°C to +150°C  
 Static Discharge Voltage .....>2000V  
 (per MIL-STD-883, Method 3015)

## Operating Conditions<sup>[2]</sup>

| Parameter   | Description                                 | Min.  | Typ. | Max.  | Unit |
|-------------|---------------------------------------------|-------|------|-------|------|
| $V_{DD3.3}$ | Supply Voltage                              | 3.135 |      | 3.465 | V    |
| $V_{DD2.5}$ | Supply Voltage                              | 2.375 |      | 2.625 | V    |
| $T_A$       | Operating Temperature (Ambient Temperature) | 0     |      | 70    | °C   |
| $C_{OUT}$   | Output Capacitance                          |       | 6    |       | pF   |
| $C_{IN}$    | Input Capacitance                           |       | 5    |       | pF   |

## Electrical Characteristics Over the Operating Range

| Parameter | Description                                      | Test Conditions                              | Min.               | Typ.       | Max.               | Unit |
|-----------|--------------------------------------------------|----------------------------------------------|--------------------|------------|--------------------|------|
| $V_{IL}$  | Input LOW Voltage                                | For all pins except SMBus                    |                    |            | 0.8                | V    |
| $V_{IH}$  | Input HIGH Voltage                               |                                              | 2.0                |            |                    | V    |
| $I_{IL}$  | Input LOW Current                                | $V_{IN} = 0V$                                |                    |            | 50                 | μA   |
| $I_{IH}$  | Input HIGH Current                               | $V_{IN} = V_{DD}$                            |                    |            | 50                 | μA   |
| $I_{OH}$  | Output HIGH Current                              | $V_{DD} = 2.375V$<br>$V_{OUT} = 1V$          | –18                | –32        |                    | mA   |
| $I_{OL}$  | Output LOW Current                               | $V_{DD} = 2.375V$<br>$V_{OUT} = 1.2V$        | 26                 | 35         |                    | mA   |
| $V_{OL}$  | Output LOW Voltage <sup>[3]</sup>                | $I_{OL} = 12\text{ mA}$ , $V_{DD} = 2.375V$  |                    |            | 0.6                | V    |
| $V_{OH}$  | Output HIGH Voltage <sup>[3]</sup>               | $I_{OH} = -12\text{ mA}$ , $V_{DD} = 2.375V$ | 1.7                |            |                    | V    |
| $I_{DD}$  | Supply Current <sup>[3]</sup><br>(DDR-Only mode) | Unloaded outputs, 133 MHz                    |                    |            | 400                | mA   |
| $I_{DD}$  | Supply Current<br>(DDR-Only mode)                | Loaded outputs, 133 MHz                      |                    |            | 500                | mA   |
| $I_{DDS}$ | Supply Current                                   | PWR_DWN# = 0                                 |                    |            | 100                | μA   |
| $V_{OUT}$ | Output Voltage Swing                             | See Test Circuitry (Refer to Figure 1)       | 0.7                |            | $V_{DD} + 0.6$     | V    |
| $V_{OC}$  | Output Crossing Voltage                          |                                              | $(V_{DD}/2) - 0.1$ | $V_{DD}/2$ | $(V_{DD}/2) + 0.1$ | V    |
| $IN_{DC}$ | Input Clock Duty Cycle                           |                                              | 48                 |            | 52                 | %    |

### Notes:

- Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
- Parameter is guaranteed by design and characterization. Not 100% tested in production.

## Switching Characteristics<sup>[4]</sup>

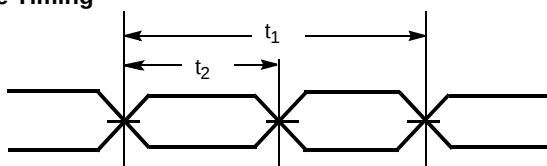
| Parameter | Name                                         | Test Conditions                                                               | Min.            | Typ. | Max.            | Unit |
|-----------|----------------------------------------------|-------------------------------------------------------------------------------|-----------------|------|-----------------|------|
| –         | Operating Frequency                          |                                                                               | 66              |      | 180             | MHz  |
| –         | Duty Cycle <sup>[4,5]</sup> = $t_2 \div t_1$ | Measured at 1.4V for 3.3V outputs<br>Measured at $V_{DD}/2$ for 2.5V outputs. | $IN_{DC} - 5\%$ |      | $IN_{DC} + 5\%$ | %    |
| $t_3$     | SDRAM Rising Edge Rate <sup>[4]</sup>        | Measured between 0.4V and 2.4V                                                | 1.0             |      | 2.50            | V/ns |
| $t_4$     | SDRAM Falling Edge Rate <sup>[4]</sup>       | Measured between 2.4V and 0.4V                                                | 1.0             |      | 2.50            | V/ns |

## Switching Characteristics<sup>[4]</sup>

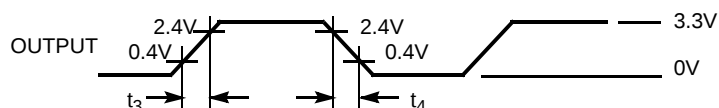
| Parameter | Name                                                 | Test Conditions                                                   | Min. | Typ. | Max. | Unit |
|-----------|------------------------------------------------------|-------------------------------------------------------------------|------|------|------|------|
| $t_{3d}$  | DDR Rising Edge Rate <sup>[4]</sup>                  | Measured between 20% to 80% of output (Refer to <i>Figure 1</i> ) | 0.5  |      | 1.50 | V/ns |
| $t_{4d}$  | DDR Falling Edge Rate <sup>[4]</sup>                 | Measured between 20% to 80% of output (Refer to <i>Figure 1</i> ) | 0.5  |      | 1.50 | V/ns |
| $t_5$     | Output to Output Skew <sup>[4]</sup>                 | All outputs equally loaded                                        |      |      | 100  | ps   |
| $t_6$     | Output $t_{4o}$ Output Skew for SDRAM <sup>[2]</sup> | All outputs equally loaded                                        |      |      | 150  | ps   |
| $t_7$     | SDRAM Buffer HH Prop. Delay <sup>[4]</sup>           | Input edge greater than 1 V/ns                                    | 5    |      | 10   | ns   |
| $t_8$     | SDRAM Buffer LL Prop. Delay <sup>[4]</sup>           | Input edge greater than 1 V/ns                                    | 5    |      | 10   | ns   |

## Switching Waveforms

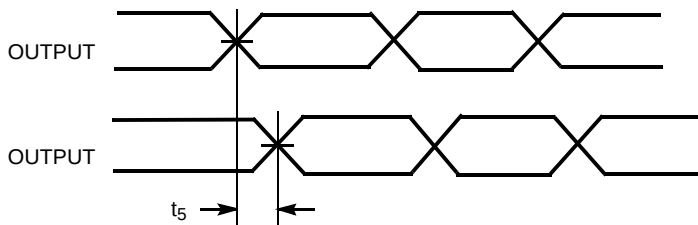
### Duty Cycle Timing



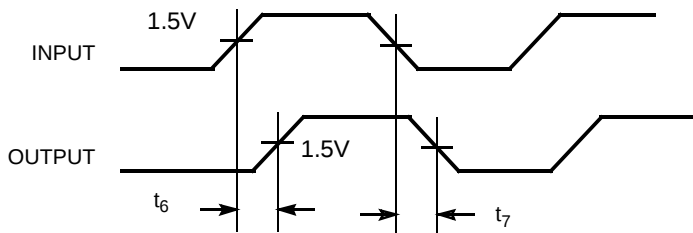
### All Outputs Rise/Fall Time



### Output-Output Skew



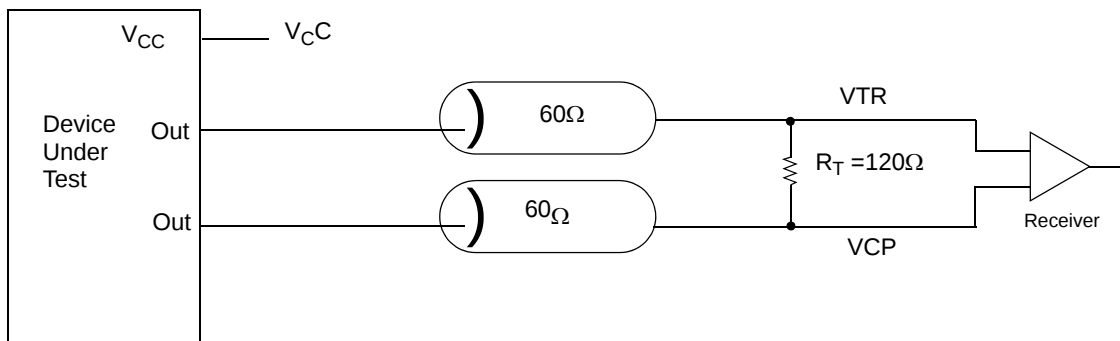
### SDRAM Buffer HH and LL Propagation Delay



### Notes:

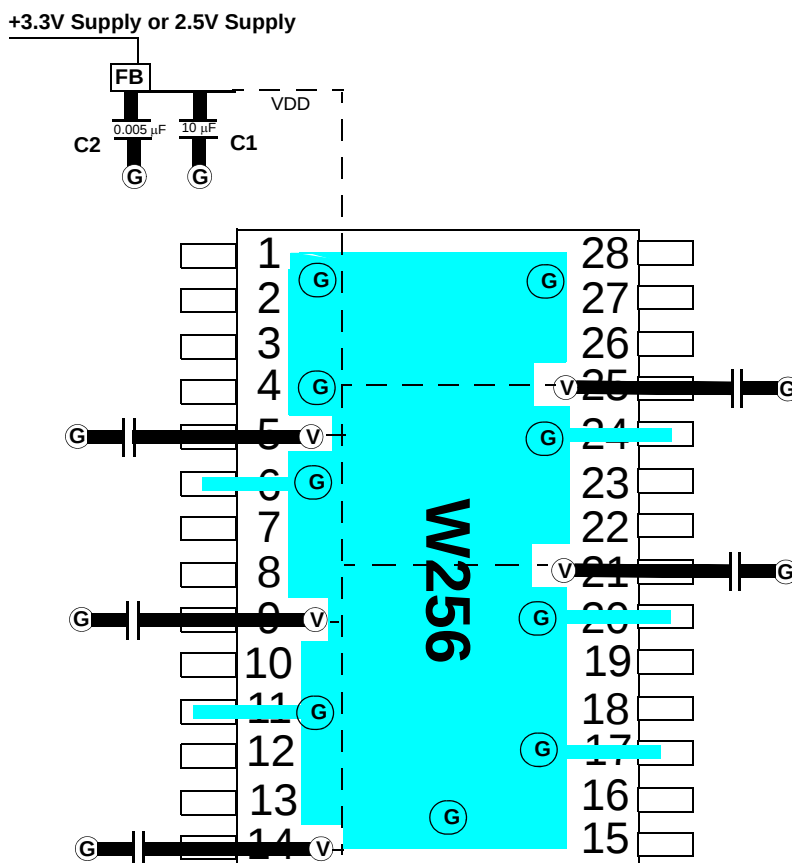
4. All parameters specified with loaded outputs.
5. Duty cycle of input clock is 50%. Rising and falling edge rate is greater than 1V/ns.

Figure 1 shows the differential clock directly terminated by a 120  $\Omega$  resistor.



**Figure 1. Differential Signal Using Direct Termination Resistor**

### Layout Example Single Voltage



FB = Dale ILB1206 – 300 (300 $\Omega$  @ 100 MHz)

Ceramic Caps C1 = 10–22  $\mu$ F C2 = 0.005  $\mu$ F

ⓐ = VIA to GND plane layer ⓑ = VIA to respective supply plane layer

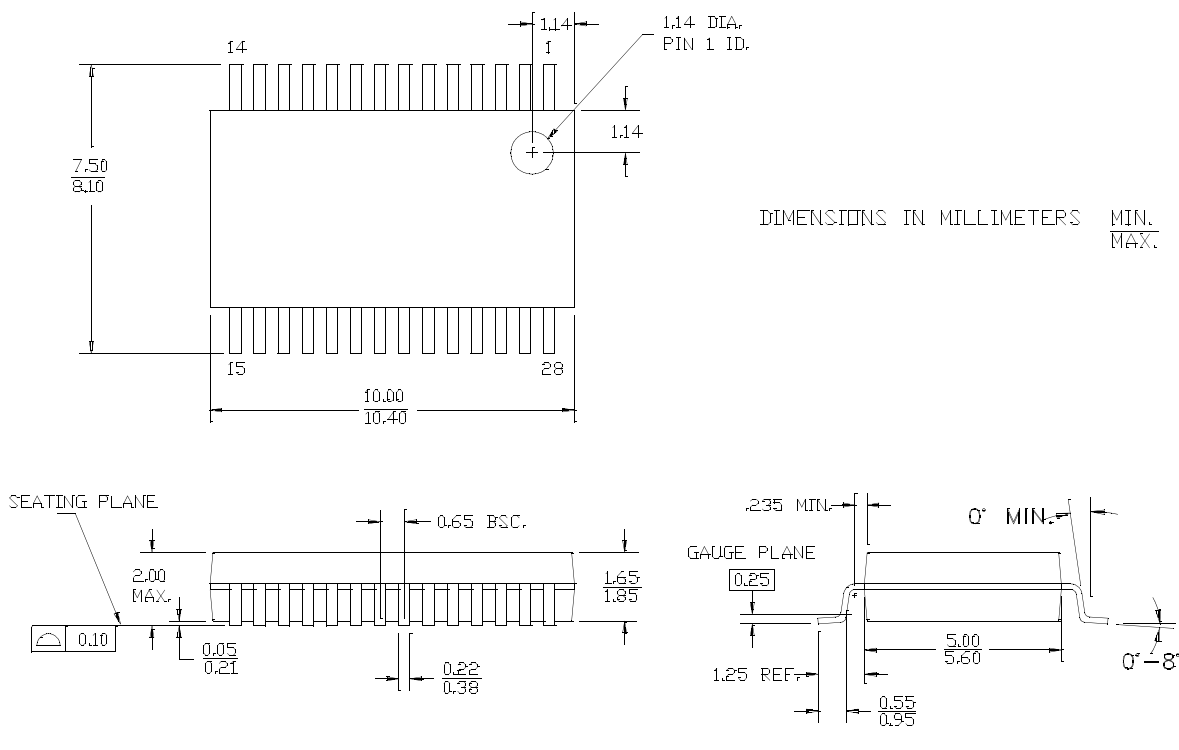
Note: Each supply plane or strip should have a ferrite bead and capacitors  
All bypass caps = 0.1  $\mu$ F ceramic

## Ordering Information

| Ordering Code    | Package Type                | Operating Range |
|------------------|-----------------------------|-----------------|
| W256H            | 28-pin SSOP                 | Commercial      |
| W256HT           | 28-pin SSOP – Tape and Reel | Commercial      |
| <b>Lead Free</b> |                             |                 |
| CYW256OXC        | 28-pin SSOP                 | Commercial      |
| CYW256OXCT       | 28-pin SSOP – Tape and Reel | Commercial      |

## Package Drawings and Dimension

### 28-Lead (5.3 mm) Shrunk Small Outline Package O28





## ClockBuilder Pro

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