

DESCRIPTION

The MP1493 is a fully integrated, high-efficiency 3A synchronous rectified step-down converter. The MP1493 operates at high efficiency over a wide output current load range. Adaptive Constant-On-Time (COT) control mode provides fast transient response, eases loop stabilization, and operates with a low-cost electrolytic capacitor.

The MP1493 requires a minimum number of readily available standard external components and is available in an 8-pin SOIC ROHS compliant package.

FEATURES

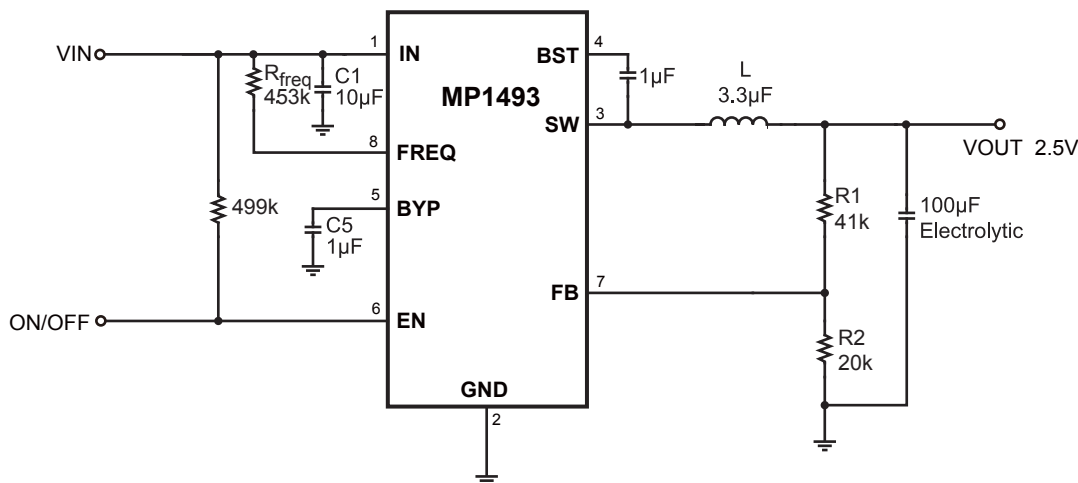
- Wide 4.2V to 16V Operating Input Range
- 3A Output Current
- Adaptive COT for Fast Transient Response
- Low $R_{DS(ON)}$ Internal Power MOSFETs
- Proprietary Switching Loss Reduction Technique
- Programmable Switching Frequency
- OCP, SCP, OVP, UVP Protection and Thermal Shutdown
- Optional OCP Protection: Latch-off Mode and Hiccup Mode
- Output Adjustable from 0.805V to 13V

APPLICATIONS

- Digital Set Top Boxes
- Flat Panel Television and Monitors
- Distributed Power Systems

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TYPICAL APPLICATION



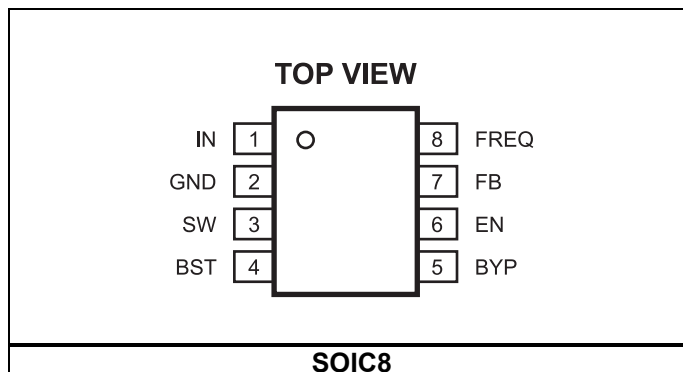
ORDERING INFORMATION

Part Number	OCP Protection	Package	Top Marking	Free Air Temperature (T _A)
MP1493DS*	Latch-off Mode	SOIC8	MP1493	-40°C to +85°C
MP1493DS-A	Hiccup Mode		MP1493-A	

* For Tape & Reel, add suffix -Z (e.g. MP1493DS-Z).

For RoHS Compliant Packaging, add suffix -LF (e.g. MP1493DS-LF-Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Supply Voltage V _{IN}	19V
V _{SW}	-0.3V to V _{IN} + 0.3V
V _{BST}	V _{SW} + 6V
All Other Pins	-0.3V to +6V
Continuous Power Dissipation (T _A = +25°C) ⁽²⁾	
SOIC8	1.39W
Junction Temperature	150°C
Lead Temperature	260°C
Storage Temperature	-65°C to +150°C

Recommended Operating Conditions ⁽³⁾

Supply Voltage V _{IN}	4.2V to 16V
Output Voltage V _{OUT}	0.805V to 13V
Maximum Junction Temp. (T _J)	+125°C

Thermal Resistance ⁽⁴⁾

	θ _{JA}	θ _{JC}
SOIC8	90	45... °C/W

Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

$V_{IN} = 12V$, $T_A = +25^{\circ}C$, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current (Shutdown)	I_{IN}	$V_{EN}=0V$		5		μA
Supply Current (Quiescent, Not Switching)	I_{IN}	$V_{EN}=2V$, $V_{FB}=0.9V$		1		mA
HS Switch On Resistance	HS_{RDS-ON}			120		m Ω
LS Switch On Resistance	LS_{RDS-ON}			60		m Ω
Switch Leakage	SW_{LKG}	$V_{EN}=0V$, $V_{SW}=0V$ or 12V		0	10	μA
Current Limit ⁽⁵⁾	I_{LIMIT}	After Soft-Start Time-out	4.0	5.0		A
One-Shot On Time	T_{ON}	$R_{freq}=300k\Omega$, $V_{OUT}=1.2V$		250		ns
Minimum Off Time	T_{OFF}			125		ns
Fold-back Off Time	T_{FB}	$I_{LIM}=1$		1.25		μs
OCF hold-off time	T_{OC}	$I_{LIM}=1$		50		μs
Feedback Voltage	V_{FB}		789	805	821	mV
Feedback Current	I_{FB}	$V_{FB}=800mV$		10	50	nA
Soft Start Time	T_{SS}			1		ms
EN Rising Threshold	V_{ILEN}		1.05	1.35	1.6	V
EN Threshold Hysteresis	V_{IHEN}			500		mV
EN Input Current	I_{EN}	$V_{EN}=2V$		2		μA
		$V_{EN}=0V$		0		
VIN Under Voltage Lockout Threshold Rising	$INUVVth$				3.1	V
VIN Under Voltage Lockout Threshold Hysteresis	$INUVHYS$			300		mV
Thermal Shutdown				150		$^{\circ}C$
Thermal Shutdown Hysteresis				25		$^{\circ}C$

Note:

5) Guaranteed by design and characterization..

PIN FUNCTIONS

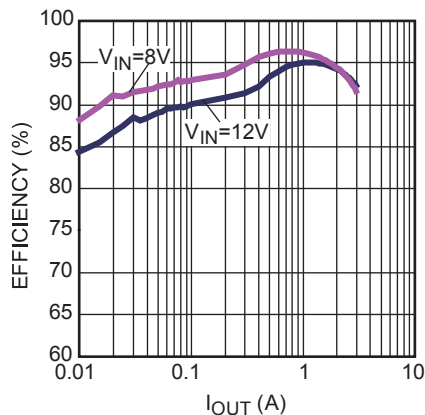
SOIC-8 Pin #	Name	Description
1	IN	Supply Voltage. The MP1493 operates from a +4.2V to +16V input rail. C1 is needed to decouple the input rail. Use wide PCB traces and multiple vias to make the connection.
2	GND	System Ground. This pin is the reference ground of the regulated output voltage. For this reason care must be taken in PCB layout.
3	SW	Switch Output. Use wide PCB traces and multiple vias to make the connection.
4	BST	Bootstrap. A capacitor connected between SW and BST pins is required to form a floating supply across the high-side switch driver.
5	BYP	Internal LDO output. Decouple with a 1 μ F ceramic capacitor. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.
6	EN	EN=1 to enable the MP1493. For automatic start-up, connect EN pin to VIN with a pull-up resistor.
7	FB	Feedback. An external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage.
8	FREQ	Switching frequency setting pin during CCM operation. Connect a resistor R_{freq} to IN to set the switching frequency. An optional 1nF decoupling capacitor can be added to improve any switching frequency jitter that may be present.

TYPICAL PERFORMANCE CHARACTERISTICS

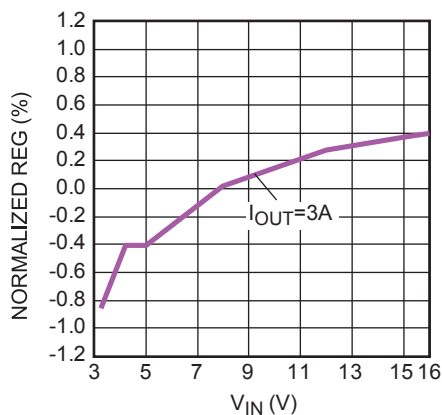
$V_{IN}=12V$, $V_{OUT}=1.2V$, $L=2.2\mu H$, $T_A=+25^\circ C$, unless otherwise noted.

Efficiency

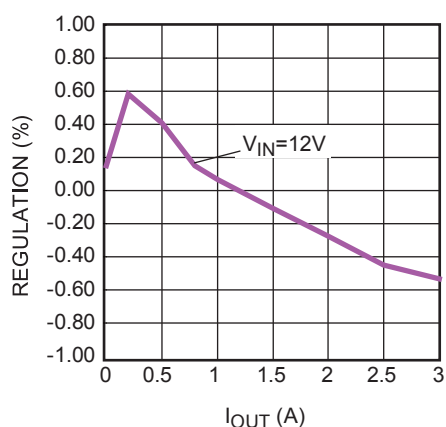
$V_{OUT}=5V$, $f_s=600kHz$, $L=6.2\mu H$



Line Regulation

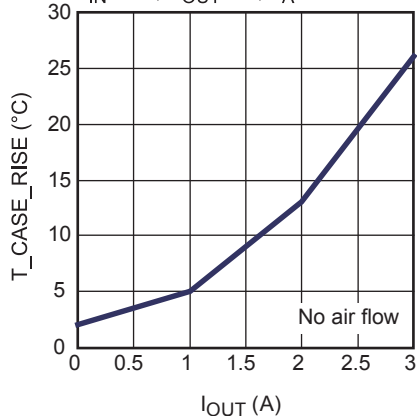


Load Regulation

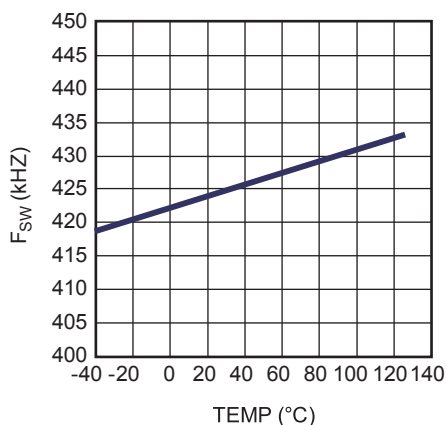


Case Temperature Rise vs. Load Current

$V_{IN}=12V$, $V_{OUT}=5V$, $T_A=25^\circ C$

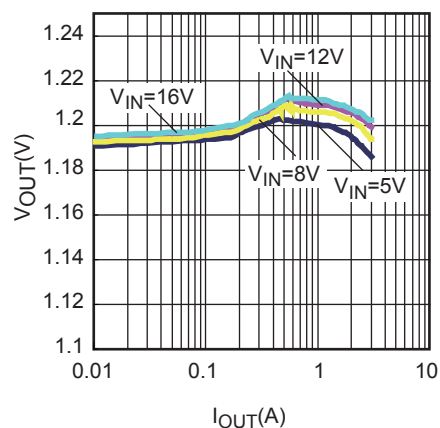


Frequency vs. Temperature



VOUT VS. IOUT

$V_{OUT}=1.2V$, Freq=500kHz

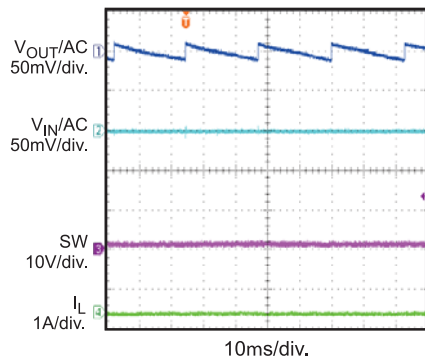


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN}=12V$, $V_{OUT}=1.2V$, $L=2.2\mu H$, $T_A=+25^{\circ}C$, unless otherwise noted.

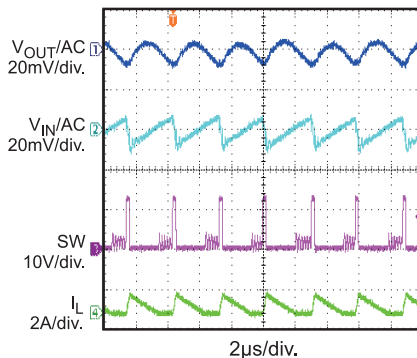
Input/Output Voltage Ripple

$I_{OUT} = 0A$



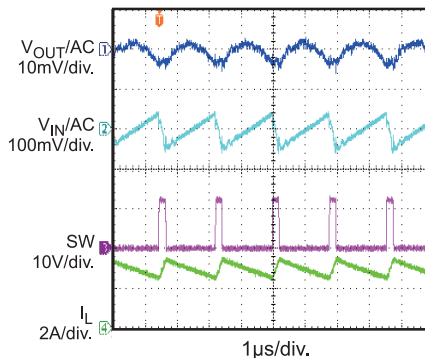
Input/Output Voltage Ripple

$I_{OUT} = 0.3A$



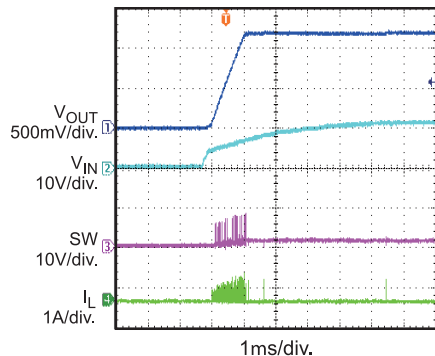
Input/Output Voltage Ripple

$I_{OUT} = 3A$



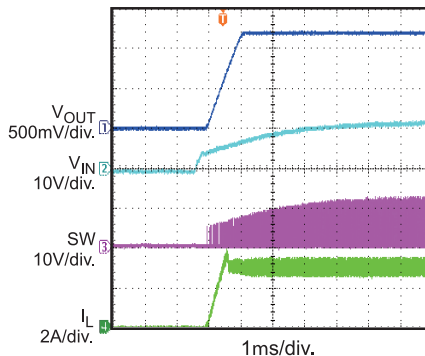
Start Up Through V_{IN}

$I_{OUT} = 0A$



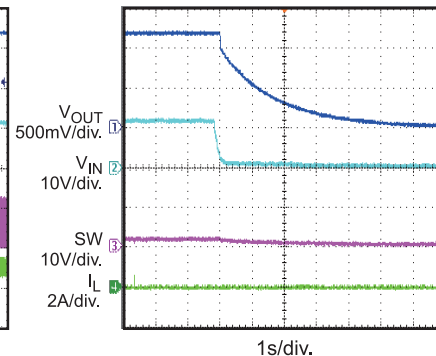
Start Up Through V_{IN}

$I_{OUT} = 3A$



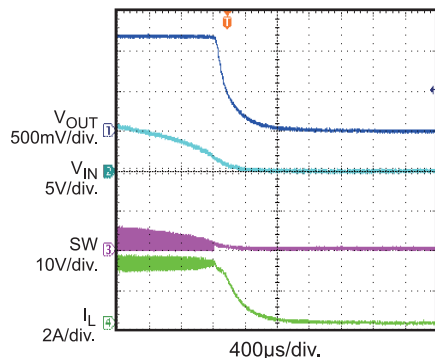
Shut Down Through V_{IN}

$I_{OUT} = 0A$



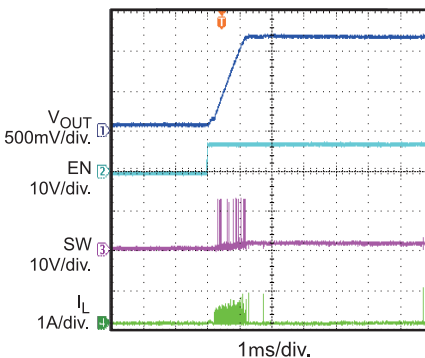
Shut Down Through V_{IN}

$I_{OUT} = 3A$



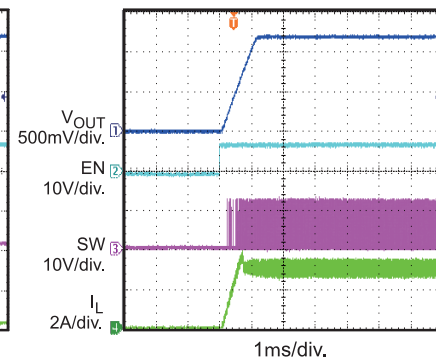
Start Up Through EN

$I_{OUT} = 0A$



Start Up Through EN

$I_{OUT} = 3A$

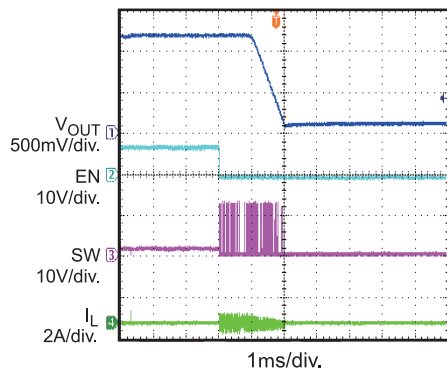


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN}=12V$, $V_{OUT}=1.2V$, $L=2.2\mu H$, $T_A=+25^{\circ}C$, unless otherwise noted.

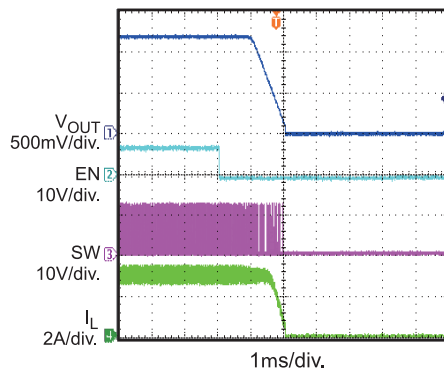
Shut Down Through EN

$I_{OUT} = 0A$



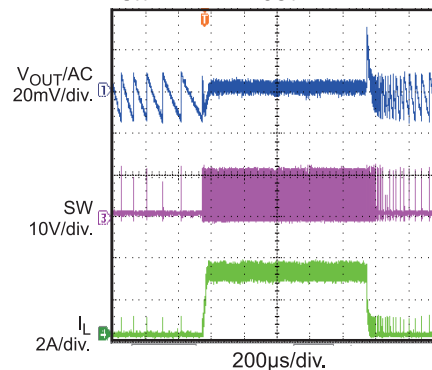
Shut Down Through EN

$I_{OUT} = 3A$



Transient Response

$I_{OUT} = 0A \sim 3A @ 2.5A/\mu s$
 $F_{SW}=500kHz$, $C_{OUT}=2 \times 22\mu F$



BLOCK DIAGRAM

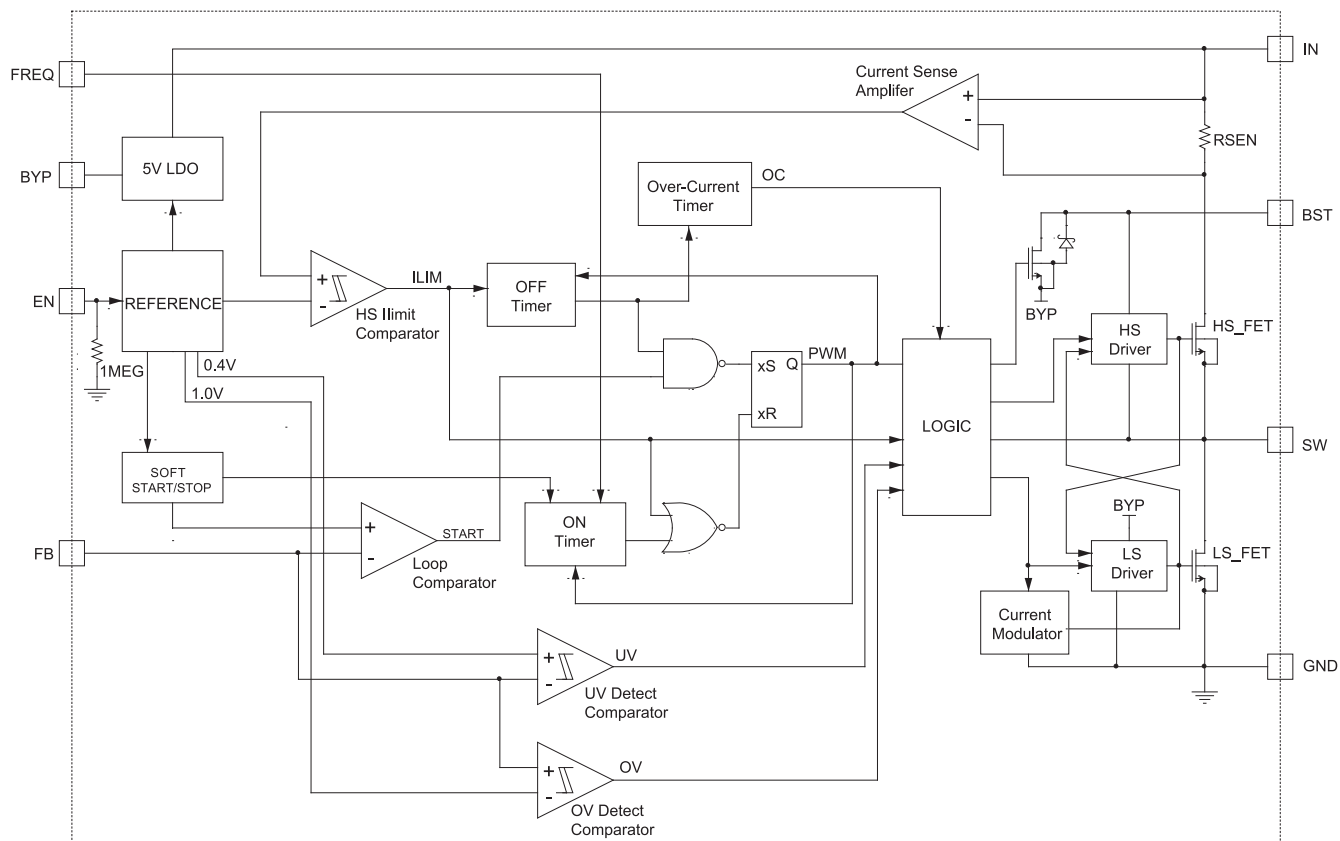


Figure 1—Function Block Diagram

OPERATION

PWM Operation

The MP1493 is a fully integrated synchronous rectified step-down converter. Adaptive constant-on-time (COT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned ON when the feedback voltage (FB) is below the reference voltage (REF) which indicates insufficient output voltage. The ON period is determined by the input voltage and the frequency-set resistor as follows:

$$T_{ON}(ns) = \frac{9.3 \times R_{FREQ}(k\Omega)}{V_{IN}(V) - 0.4} \quad (1)$$

After the ON period elapses, the HS-FET is turned off. It is turned ON again when FB drops below REF. By repeating operation in this way, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS-FET is in its OFF state to minimize the conduction loss. There will be a dead short between input and GND if both HS-FET and LS-FET are turned on at the same time. It's called shoot-through. In order to avoid shoot-through, a dead-time (DT) is internally generated between HS-FET off and LS-FET on.

When the output current is high, the HS-FET and LS-FET repeat on/off as described above. In this operation, the inductor current will never go to zero. It's called continuous-conduction-mode (CCM) operation. In CCM operation, the switching frequency (F_s) is fairly constant.

Light-Load Operation

When the load current decreases, MP1493 reduces the switching frequency automatically to maintain high efficiency. As the output current reduces from heavy-load condition, the inductor current decreases as well, and eventually comes close to zero current. The LS-FET driver turns into tri-state (high Z) whenever the inductor current reaches zero level. The current modulator takes over the control of LS-FET and limits the inductor current to less than -1mA. Hence, efficiency at light-load condition is optimized.

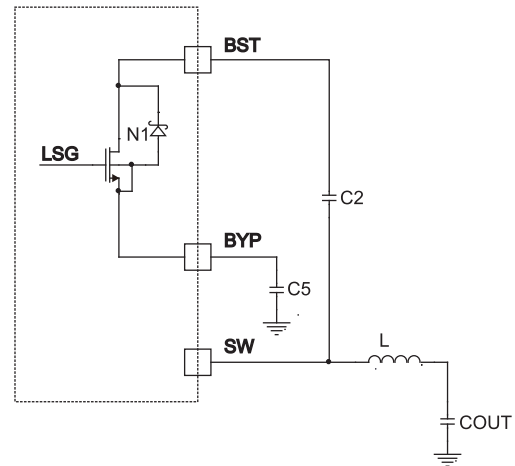


Figure 2

Floating Driver and Bootstrap Charging

The floating power MOSFET driver is powered by an external bootstrap capacitor. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is charged from VCC through N1 (Figure 3). N1 turns on when LS switches turns on and turns off when LS switch turns off.

Switching Frequency

Adaptive constant-on-time (COT) control is used in MP1493 and there is no dedicated oscillator in the IC. The input voltage is feed-forwarded to the on-time one-shot timer through the resistor R_{freq} . The duty ratio is kept as V_{OUT}/V_{IN} . Hence the switching frequency is fairly constant over the input voltage range. The switching frequency can be set as follows:

$$F_s(kHz) = \frac{10^6}{\frac{9.3 \times R_{FREQ}(k\Omega)}{V_{IN}(V) - 0.4} \times \frac{V_{IN}(V)}{V_{OUT}(V)} + T_{DELAY}(ns)} \quad (2)$$

Where TDELAY is the comparator delay, it's about 40ns.

MP1493 is optimized to operate at high switching frequency but with high efficiency. High switching frequency makes it possible to utilize small sized LC filter components to save system PCB space.

Soft Start/Stop

MP1493 employs soft start/stop (SS) mechanism to ensure smooth output during power up and power shut-down. When the EN pin becomes high, an internal SS voltage ramps up slowly. The SS voltage takes over the REF voltage to the PWM comparator. The output voltage smoothly ramps up with the SS voltage. Once SS voltage reaches the same level of the REF voltage, it keeps ramping up, while REF takes over the PWM comparator. At this point, the soft start finishes, it enters steady state operation. The SS time is about 1ms.

When the EN pin becomes low, the internal SS voltage is discharged through an internal current source. Once the SS voltage reaches REF voltage, it takes over the PWM comparator. The output voltage will decrease smoothly with SS voltage until zero level.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

MP1493 has cycle-by cycle over-current limit control. The inductor current is monitored during the ON state. And it has two optional OCP/SCP protection modes: latch-off mode and hiccup mode.

For MP1493DS, the HS-FET turns off when the inductor current exceeds the current limit and the OCP timer—set at 50 μ s—starts. The OCP triggers if the inductor current reaches or exceeds the current limit every cycle in those 50 μ s. The MP1493DS short-circuit protection (SCP) occurs when dead shorts occur—when the inductor current exceeds the current limit and the FB voltage is lower than 50% of the V_{REF} —and will trigger the OCP.

For MP1493DS-A, enters hiccup mode, that periodically restarts the part when the inductor current peak value exceeds the current limit and V_{FB} drops below the under-voltage (UV) threshold. Typically, the UV threshold is 50% below the REF voltage. In OCP/SCP, MP1493DS-A will disable the output voltage power, discharge internal soft-start cap, and then automatically try to soft-start again. If the over-current circuit condition still holds after soft-start ends, it repeats this operation cycle until the over-current circuit condition disappears, and output rises back to regulation level.

Over/Under-voltage Protection (OVP/UVP)

MP1493 monitors the output voltage through a resistor divided feedback (FB) voltage to detect over and under voltage on the output. When the FB voltage is higher than 125% of the REF voltage, it'll trigger OVP. Once it triggers OVP, the LS-FET is always on, while the HS-FET is off. It needs power cycle to power up again. When the FB voltage is below 50% of the REF voltage (0.805V), UVP will be triggered. Usually UVP comes with current limit is hit, hence it results in SCP.

UVLO protection

MP1493 has under-voltage lock-out protection (UVLO). When the input voltage is higher than the UVLO rising threshold voltage, the MP1493 powers up. It shuts off when the input voltage is lower than the UVLO falling threshold voltage. This is non-latch protection.

Thermal Shutdown

Thermal shutdown is employed in MP1493. The junction temperature of the IC is monitored internally. If the junction temperature exceeds the threshold value (typically 150°C), the converter shuts off. This is non-latch protection. There is about 25°C hysteresis. Once the junction temperature drops around 125°C, it initiates a SS.

APPLICATION INFORMATION

Setting the Output Voltage

The output voltage is set by using a resistive voltage divider from the output voltage to FB pin. For applications that use electrolytic capacitor with a controlled output of ESR, the output voltage is set by feedback resistors R1 and R2. First, choose a value for R2. A value within 40kΩ is recommended to ensure stable operation. Then R1 is determined as follows which the output ripple is considered:

$$R_1 = \frac{V_{OUT} - \frac{1}{2} \Delta V_{OUT} - V_{REF}}{V_{REF}} \cdot R_2 \quad (3)$$

ΔV_{OUT} is the output ripple determined by equation 13.

When using low ESR ceramic output capacitor, an external voltage ramp should be added to FB through resistor R4 and capacitor C4. Choose a value within 5kΩ-40kΩ for R2. The value of R1 then is determined as follows:

$$R_1 = \frac{1}{\frac{V_{REF} + \frac{1}{2} V_{RAMP}}{R_2 \times (V_{OUT} - V_{REF} - \frac{1}{2} V_{RAMP})} - \frac{1}{R_{RAMP}}} \quad (4)$$

V_{RAMP} is determined by equation (11)

As VRAMP changes due to changes in VOUT and VIN, VFB also varies. To improve the output voltage accuracy and simplify the calculation of R1 in equation 4, a DC-blocking capacitor Cdc can be added. Figure 3 shows a simplified circuit with external ramp compensation and a DC-blocking capacitor. With this capacitor, R1 can easily be obtained by using equation 5.

Cdc is suggested to be 1-4.7μF for better DC blocking performance.

$$R_1 = \frac{1}{\frac{V_{REF} + \frac{1}{2} V_{RAMP}}{R_2 (V_{OUT} - V_{REF} - \frac{1}{2} V_{RAMP})}} \quad (5)$$

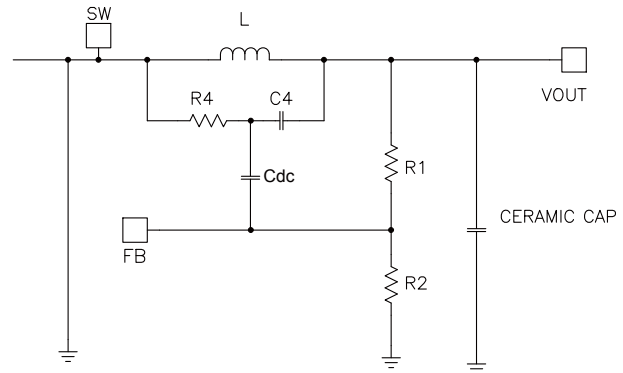


Figure 3—Simplified Circuit of External Ramp Compensation with DC blocking capacitor.

Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance. In the layout, it's recommended to put the input capacitor as close as possible to the VIN pin.

The capacitance varies significantly over temperature. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable over temperature.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated as follows:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (6)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (7)$$

For simplification, choose the input capacitor whose RMS current rating is greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system design, choose the input capacitor that meets the specification.

The input voltage ripple can be estimated as follows:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_S \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_S \times C_{IN}} \quad (9)$$

Output Capacitor

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_S^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

The output voltage ripple caused by ESR is very small. So it needs an external ramp to stabilize the system. The voltage ramp is expected to around 30mV. The external ramp can be generated through resistor R_4 and capacitor C_4 follows:

$$V_{RAMP} = \frac{(V_{IN} - V_{OUT}) \times T_{ON}}{R_4 \times C_4} \quad (11)$$

C_4 should be chosen so that it meets the following condition:

$$\frac{1}{2\pi \times F_S \times C_4} < \frac{1}{5} \times (\frac{R_1 \times R_2}{R_1 + R_2}) \quad (12)$$

In the case of POSCAP or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. The ramp voltage generated from the ESR is high enough to stabilize the system. So the external ramp is not recommended. A minimum ESR value of 12mΩ is required to ensure stable operation of the converter. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_S \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (13)$$

Maximum output capacitor limitation should be also considered in design application. MP1493 has an around 1ms soft-start time period. If the output capacitor value is too high, the output voltage can't reach the design value during the soft-start time, and then it will fail to regulate. The maximum output capacitor value C_{O_MAX} can be limited approximately by:

$$C_{O_MAX} = (I_{LIM_AVG} - I_{OUT}) \times T_{ss} / V_{OUT} \quad (14)$$

Where, I_{LIM_AVG} is the average start-up current during soft-start period. T_{ss} is the soft-start time.

Inductor

The inductor is required to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will result in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current. A good rule of thumb for determining the inductance to use is to allow the peak-to-peak ripple current in the inductor to be approximately 30~40% of the maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$$L = \frac{V_{OUT}}{F_S \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (15)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated by:

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2F_S \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (16)$$

Application Recommendation

As Figure 4 shown, when output cap is electrolytic POSCAP, etc with large ESR, no external ramp is needed. Recommended parameters are as below Table 1 to Table 3 shown.

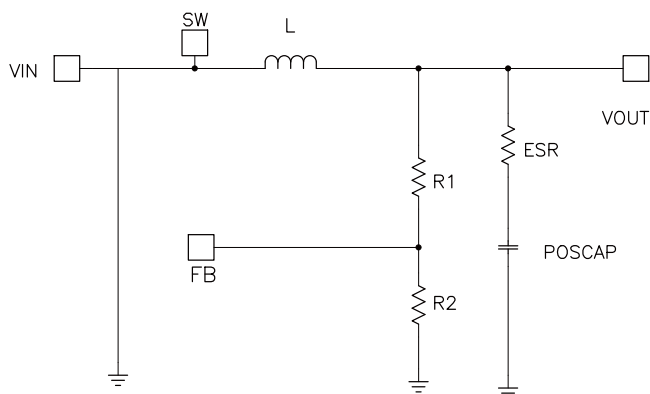


Figure 4—Simplified Circuit in PWM Mode without External Ramp Compensation

Table 1—300kHz recommended parameters without External Ramp Compensation

Recommended Conditions: $V_{IN}=12V$, $I_{OUT}=3A$

V_{OUT} (V)	L (μH)	R1 (k Ω)	R2 (k Ω)	Rfreq (k Ω)
1.2	3.3	12.1	26.1	402
2.5	3.3	30	14.3	820
3.3	3.3	40.2	13.3	1000

Table 2—500kHz recommended parameters without External Ramp Compensation

Recommended Conditions: $V_{IN}=12V$, $I_{OUT}=3A$

V_{OUT} (V)	L (μH)	R1 (k Ω)	R2 (k Ω)	Rfreq (k Ω)
1.2	3.3	12.1	26.1	240
2.5	3.3	30	14.3	510
3.3	3.3	40.2	13.3	649

Table 3—700kHz recommended parameters without External Ramp Compensation

Recommended Conditions: $V_{IN}=12V$, $I_{OUT}=3A$

V_{OUT} (V)	L (μH)	R1 (k Ω)	R2 (k Ω)	Rfreq (k Ω)
1.2	2.2	12.1	26.1	174
2.5	2.2	30	14.3	348
3.3	2.2	40.2	13.3	475

As Figure 5 shown, when output cap is ceramic CAP with lower ESR, external ramp is needed. Recommended parameters are as below Table 4 to Table 6 shown.

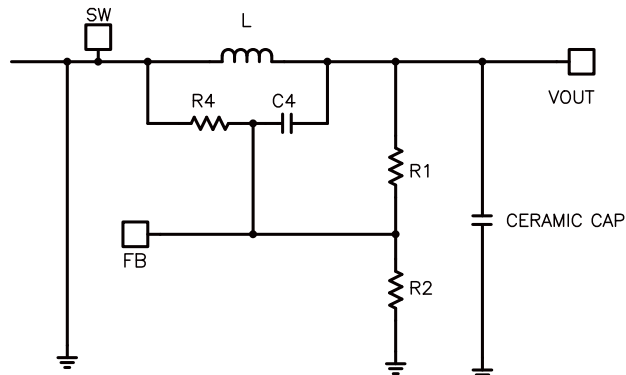


Figure 5—Simplified Circuit in PWM Mode with External Ramp Compensation

Table 4—300kHz recommended parameters with External Ramp Compensation

Recommended Conditions: $V_{IN}=12V$, $I_{OUT}=3A$

V_{OUT} (V)	L (μH)	R1 (k Ω)	R2 (k Ω)	R4 (k Ω)	C4 (pF)	Rfreq (k Ω)
1.2	3.3	12.1	26.1	330	220	402
2.5	3.3	30	14.3	698	220	820
3.3	3.3	40.2	12.7	698	220	1000

Table 5—500kHz recommended parameters with External Ramp Compensation

Recommended Conditions: $V_{IN}=12V$, $I_{OUT}=3A$

V_{OUT} (V)	L (μH)	R1 (k Ω)	R2 (k Ω)	R4 (k Ω)	C4 (pF)	Rfreq (k Ω)
1.2	3.3	12.1	26.1	402	220	240
2.5	3.3	30	14.3	549	220	510
3.3	3.3	40.2	12.7	698	220	649

Table 6—700kHz recommended parameters with External Ramp Compensation

Recommended Conditions: $V_{IN}=12V$, $I_{OUT}=3A$

V_{OUT} (V)	L (μH)	R1 (k Ω)	R2 (k Ω)	R4 (k Ω)	C4 (pF)	Rfreq (k Ω)
1.2	2.2	12.1	26.1	330	220	174
2.5	2.2	30	14.3	549	220	348
3.3	2.2	40.2	12.7	698	220	475

According to equation (14) and some design abundance are reserved, recommended maximum output capacitor value is as below Table 7 shown.

Table 7—Recommended maximum output capacitor value ($F_S=500$ kHz)

Recommended Conditions: $V_{IN}=12V$, $I_{OUT}=3A$

V_{OUT} (V)	1.2	1.8	2.5	3.3	5
C_{O_MAX} (μF)	680	570	390	330	220

The detailed application schematic is shown in Figure 6 and Figure 7. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more possible applications of this device, please refer to related Evaluation Board Data Sheets.

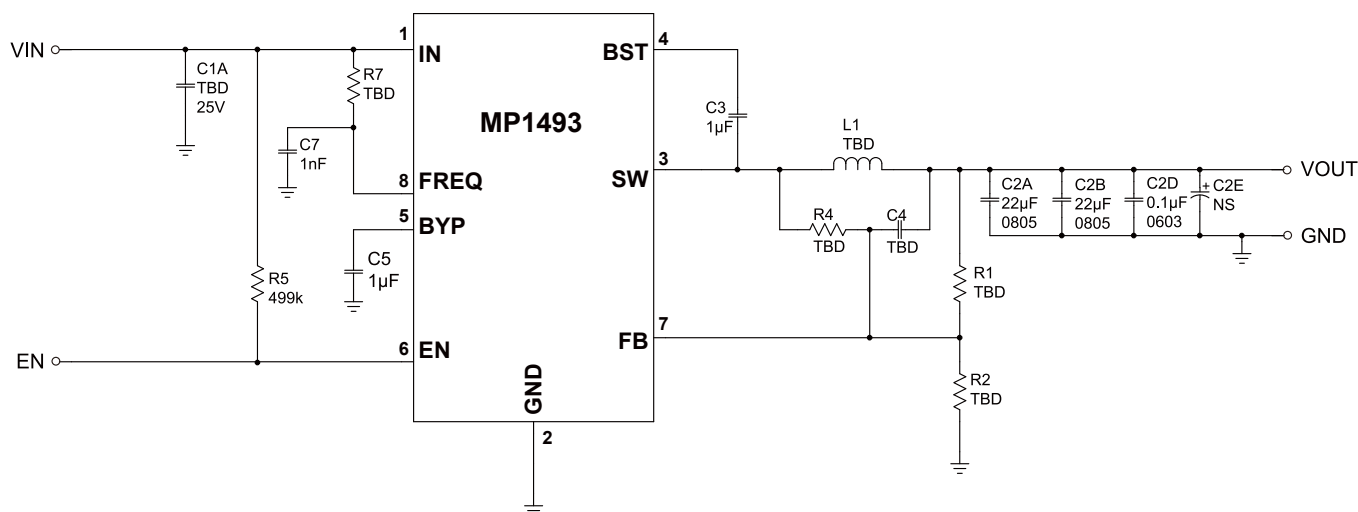


Figure 6—Detailed Application Schematic

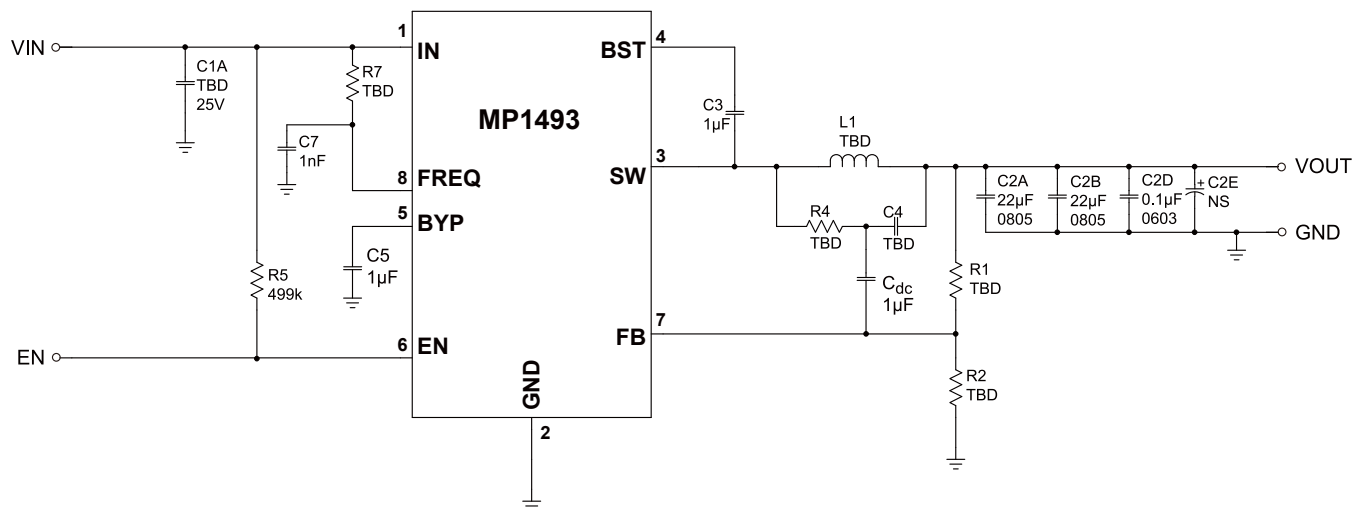


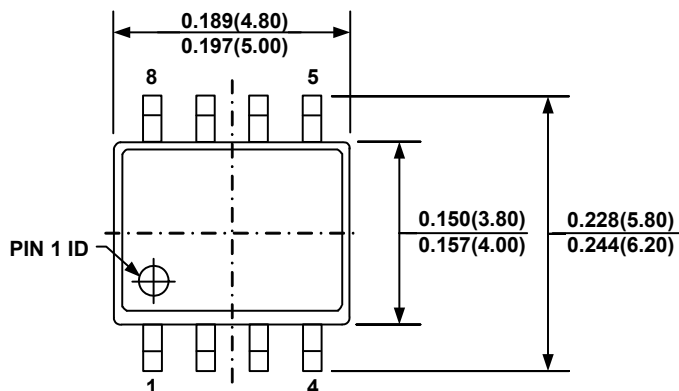
Figure 7—Detailed Application Schematic with Low ESR Ceramic Capacitor and DC Blocking Capacitor.

Layout Recommendation

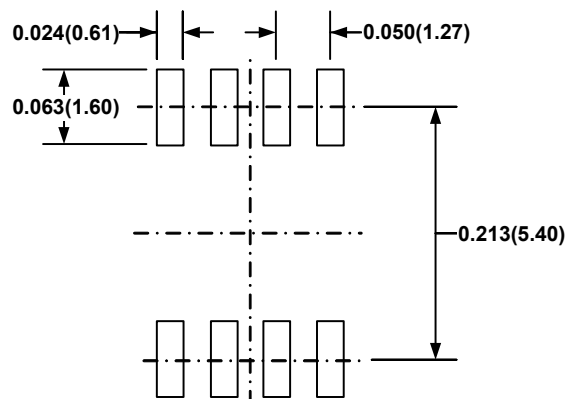
- 1) Put the input capacitors as close as possible to the IN pin.
- 2) Put the decoupling capacitor as close as possible to the V_{CC} pin.
- 3) Put the inductor as close as possible to SW pin. Make the SW pad as large as possible to minimize the switching noise interference.
- 4) The FB pin is directly connected to the PWM comparator. It should be routed away from the noisy SW node.

PACKAGE INFORMATION

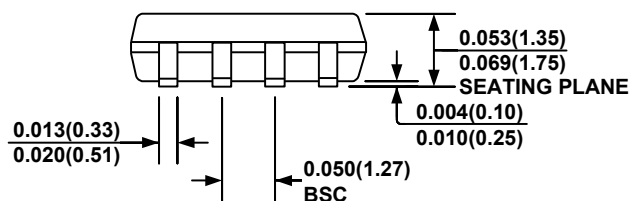
SOIC8



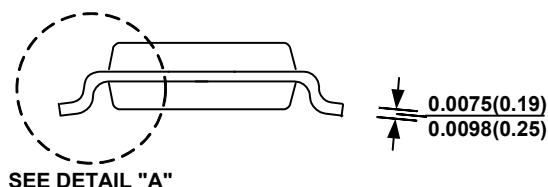
TOP VIEW



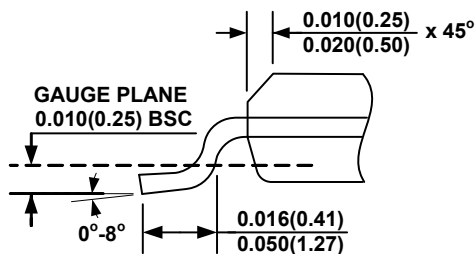
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
- 6) DRAWING IS NOT TO SCALE.

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