

TLP718

Isolated Bus Drivers
High Speed Line Receivers
Microprocessor System Interfaces

The Toshiba TLP718 consists of a GaAlAs light-emitting diode and an integrated high-gain, high-speed photodetector. This unit is a 6-pin SDIP. The TLP718 is 50% smaller than the 8-PIN DIP and meets the reinforced insulation class requirements of international safety standards. Therefore the mounting area can be reduced in equipment requiring safety standard certification.

The detector has a totem pole output stage to provide both source and sink driving. The detector IC has an internal shield that provides a guaranteed common-mode transient immunity of 10 kV/μs.

The TLP718 is inverter logic type. For buffer logic type, the TLP715 is in line-up.

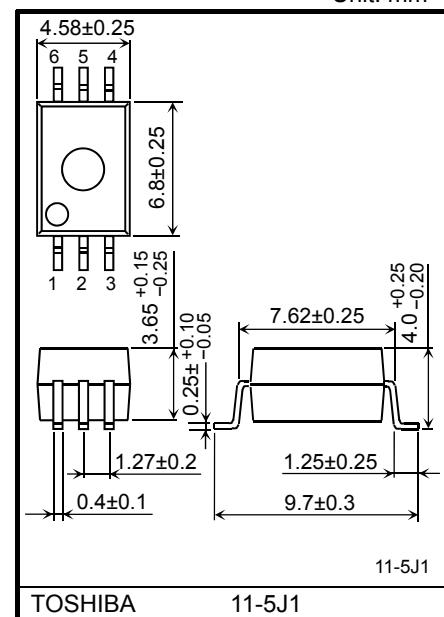
- Inverter logic type (totem pole output)
- Guaranteed performance over temperature : -40 to 100°C
- Power supply voltage : 4.5 to 20 V
- Input current: $I_{FHL} = 3\text{mA}$ (max)
- Switching time (t_{pHL} / t_{pLH}) : 250 ns (max)
- Common-mode transient immunity : $\pm 10 \text{ kV}/\mu\text{s}$ (min)
- Isolation voltage : 5000 Vrms (min)
- UL recognized
UL1577, File No.E67349
- c-UL recognized
CSA Component Acceptance Service No. 5A, File No.E67349
- Option (D4)
TÜV recognized / VDE under application : DIN EN60747-5-5
Maximum Operating Insulation Voltage : 890V_{pk}
Highest Permissible Over Voltage : 8000V_{pk}
- (Note) : When a EN60747-5-5 approved type is needed,
Please designate "Option(D4)"

- Construction Mechanical Rating

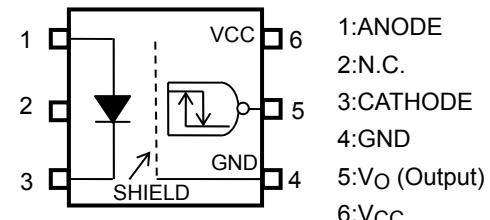
	7.62 mm pitch standard type	10.16 mm pitch TLPXXXF type
Creepage Distance	7.0 mm (min)	8.0 mm (min)
Clearance	7.0 mm (min)	8.0 mm (min)
Insulation Thickness	0.4 mm (min)	0.4 mm (min)

Truth Table

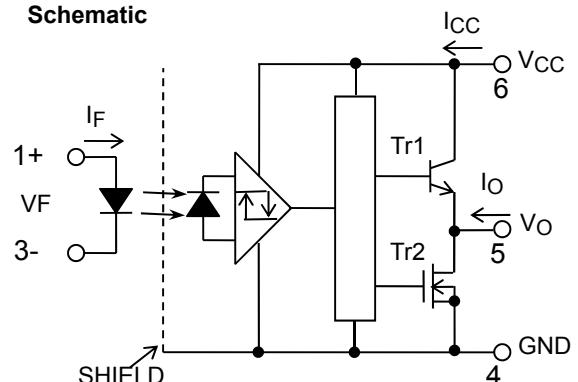
Input	LED	Tr1	Tr2	Output
H	ON	OFF	ON	L
L	OFF	ON	OFF	H



Pin Configuration (Top View)



Schematic



0.1 μF bypass capacitor must be connected between pins 6 and 4. (Note 5)

Start of commercial production
2008/12

Absolute Maximum Ratings (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
LED	Forward Current (Ta ≤ 83°C)	I _F	20	mA
	Forward Current Derating (Ta ≥ 83°C)	ΔI _F /ΔTa	-0.48	mA/°C
	Peak Transient Forward Current (Note 1)	I _{FPT}	1	A
	Reverse Voltage	V _R	5	V
	Junction Temperature	T _j	125	°C
DETECTOR	Output Current 1 (Ta ≤ 25°C)	I _{O1}	25 / -15	mA
	Output Current 2 (Ta ≤ 100°C)	I _{O2}	13 / -13	mA
	Output Voltage	V _O	-0.5 to 20	V
	Supply Voltage	V _{CC}	-0.5 to 20	V
	Junction Temperature	T _j	125	°C
Operating Temperature Range		T _{opr}	-40 to 100	°C
Storage Temperature Range		T _{stg}	-55 to 125	°C
Lead Solder Temperature (10 s)		T _{sol}	260	°C
Isolation Voltage (AC, 1 minute, R.H. ≤ 60%, Ta = 25°C) (Note 2)		B _V _S	5000	V _{rms}

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 1: Pulse width PW ≤ 1μs, 300pps.

Note 2: Device Considered a two terminal device: pins 1, 2 and 3 shorted together and pins 4, 5 and 6 shorted together.

Recommended Operating Conditions

CHARACTERISTIC	SYMBOL	MIN	TYP.	MAX	UNIT
Input Current, ON	I _F (ON)	4.5	-	10	mA
Input Voltage, OFF	V _F (OFF)	0	-	0.8	V
Supply Voltage*	V _{CC}	4.5	-	20	V
Operating Temperature	T _{opr}	-40	-	100	°C

* This item denotes operating ranges, not meaning of recommended operating conditions.

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Electrical Characteristics

(Unless otherwise specified, $T_a = -40$ to 100°C , $V_{CC} = 4.5$ to 20 V)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	CONDITION		MIN	TYP. *	MAX	UNIT
Input forward voltage	V_F	—	$I_F = 5$ mA, $T_a = 25^\circ\text{C}$		1.4	1.6	1.7	V
Temperature coefficient of forward voltage	$\Delta V_F/\Delta T_a$	—	$I_F = 5$ mA		—	-2.0	—	$\text{mV}/^\circ\text{C}$
Input reverse current	I_R	—	$V_R = 5$ V, $T_a = 25^\circ\text{C}$		—	—	10	μA
Input capacitance	C_T	—	$V = 0$ V, $f = 1$ MHz, $T_a = 25^\circ\text{C}$		—	45	—	pF
Logic LOW output voltage	V_{OL}	1	$I_{OL} = 3.5$ mA, $I_F = 5$ mA		—	0.2	0.6	V
Logic HIGH output voltage (Note3)	V_{OH}	2	$I_{OH} = -2.6$ mA, $V_F = 0.8$ V	$V_{CC} = 4.5$ V	2.7	3.5	—	V
				$V_{CC} = 20$ V	17.4	19	—	
Logic LOW supply current	I_{CCL}	3	$I_F = 5$ mA		—	—	3.0	mA
Logic HIGH supply current	I_{CCH}	4	$V_F = 0$ V		—	—	3.0	mA
Logic LOW short circuit output current	I_{OSL}	5	$I_F = 5$ mA	$V_{CC} = V_O = 5.5$ V	15	80	—	mA
				$V_{CC} = V_O = 20$ V	20	90	—	
Logic HIGH short circuit output current (Note4)	I_{OSH}	6	$V_F = 0$ V, $V_O = \text{GND}$	$V_{CC} = 5.5$ V	-5	-15	—	mA
				$V_{CC} = 20$ V	-10	-20	—	
Input current logic LOW output (Note4)	I_{FHL}	—	$I_O = 3.5$ mA, $V_O < 0.6$ V		—	0.4	3	mA
Input voltage logic HIGH output	V_{FLH}	—	$I_O = -2.6$ mA, $V_O > 2.4$ V		0.8	—	—	V
Input current hysteresis	I_{HYS}	—	$V_{CC} = 5$ V		—	0.05	—	mA

* All typical values are at $T_a=25^\circ\text{C}$, $V_{CC}=5$ V unless otherwise specifiedNote 3: $V_{OH}=V_{CC}-V_O$ [V]

Note 4: Duration of output short circuit time should not exceed 10 ms.

Note 5: A ceramic capacitor (0.1 μF) should be connected from pin 6 to pin 4 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching property. The total lead length between capacitor and coupler should not exceed 1 cm.

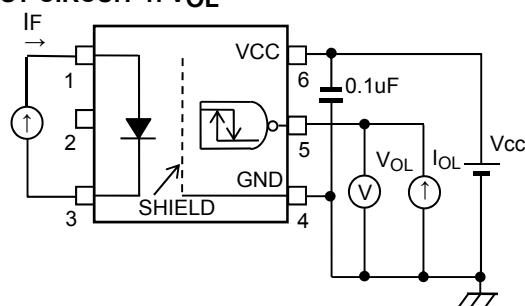
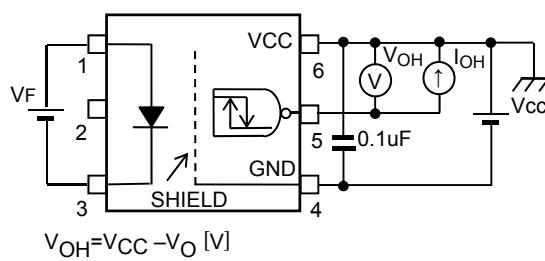
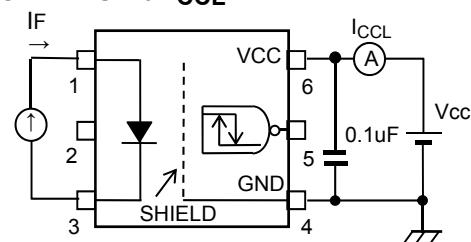
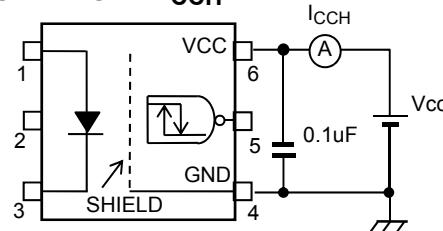
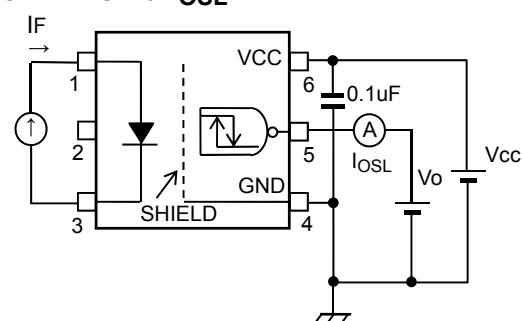
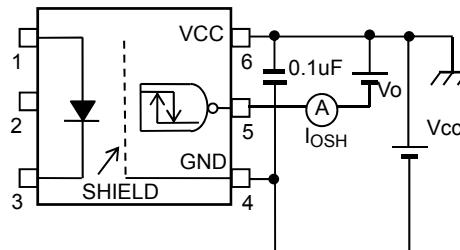
Isolation Characteristics ($T_a = 25^\circ\text{C}$)

CHARACTERISTIC	SYMBOL	TEST CONDITION		MIN	TYP.	MAX	UNIT
Capacitance input to output	C_S	$V = 0$ V, $f = 1$ MHz (Note 2)		—	1.0	—	pF
Isolation resistance	R_S	R.H. $\leq 60\%$, $V_S = 500$ V (Note 2)		1×10^{12}	10^{14}	—	Ω
Isolation voltage	BV_S	AC, 1 minute		5000	—	—	V_{rms}
		AC, 1 second, in oil		—	10000	—	
		DC, 1 minute, in oil		—	10000	—	V_{dc}

Switching Characteristics

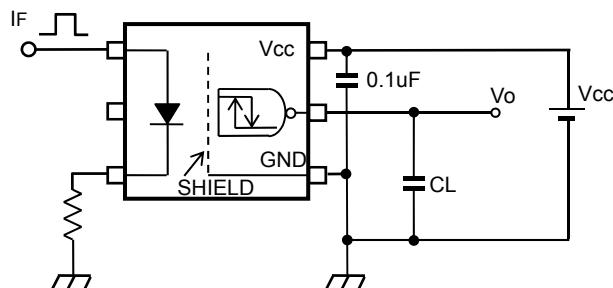
(Unless otherwise specified, $T_a = -40$ to 100°C , $V_{CC} = 4.5$ to 20 V)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	CONDITION	MIN	TYP. *	MAX	UNIT
Propagation delay time to logic HIGH output	t_{PLH}	7,8	$I_F = 3 \rightarrow 0$ mA	30	120	250	ns
Propagation delay time to logic LOW output	t_{pHL}		$I_F = 0 \rightarrow 3$ mA	30	120	250	ns
Switching time dispersion between ON and OFF	$ t_{pHL} - t_{PLH} $		—	—	—	220	ns
Rise Time (10 – 90 %)	t_r		$I_F = 3 \rightarrow 0$ mA, $V_{CC} = 5$ V	—	30	—	ns
Fall Time (90 – 10 %)	t_f		$I_F = 0 \rightarrow 3$ mA, $V_{CC} = 5$ V	—	30	—	ns
Common-mode transient immunity at HIGH level output	CM_H	9	$V_{CM} = 1000$ V _{p-p} , $I_F = 0$ mA, $V_{CC} = 20$ V, $T_a = 25^\circ\text{C}$	10000	—	—	V/us
Common-mode transient immunity at LOW level output	CM_L		$V_{CM} = 1000$ V _{p-p} , $I_F = 5$ mA, $V_{CC} = 20$ V, $T_a = 25^\circ\text{C}$	-10000	—	—	V/us

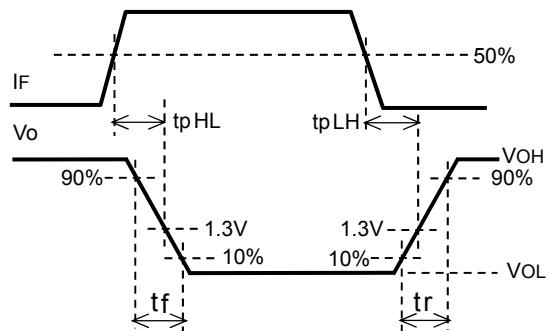
*All typical values are at $T_a = 25^\circ\text{C}$.TEST CIRCUIT 1: V_{OL} TEST CIRCUIT 2: V_{OH} TEST CIRCUIT 3: I_{CCL} TEST CIRCUIT 4: I_{CCH} TEST CIRCUIT 5: I_{OSL} TEST CIRCUIT 6: I_{OSH} 

TEST CIRCUIT 7: Switching Time Test Circuit

$I_F=3\text{ mA(P.G)}$
($f=50\text{ kHz}$, duty=50%
less than $t_r = t_f = 5\text{ ns}$)

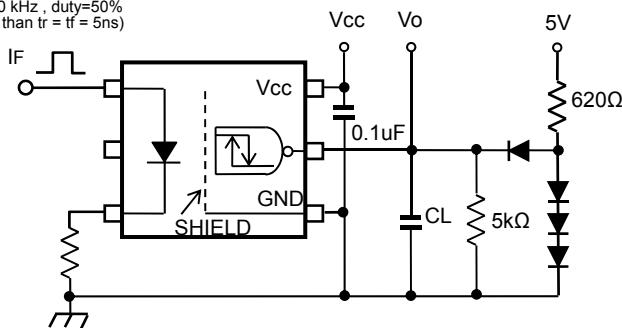


CL: stray capacitance of probe and wiring (to 15 pF)

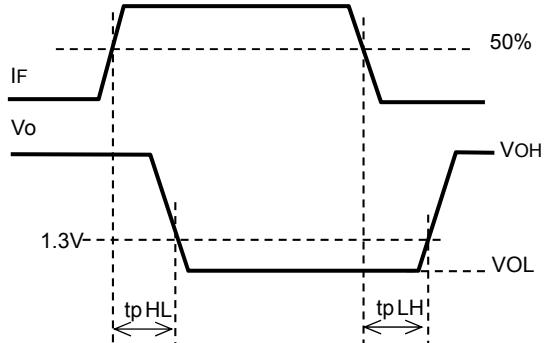


TEST CIRCUIT 8: Switching Time Test Circuit

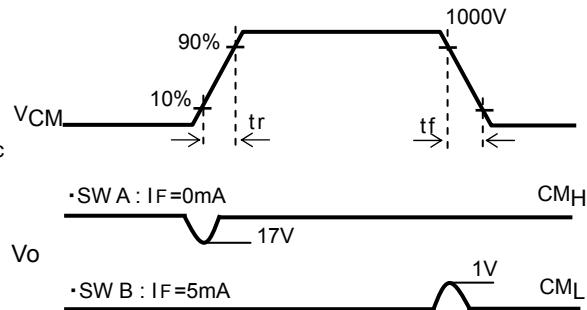
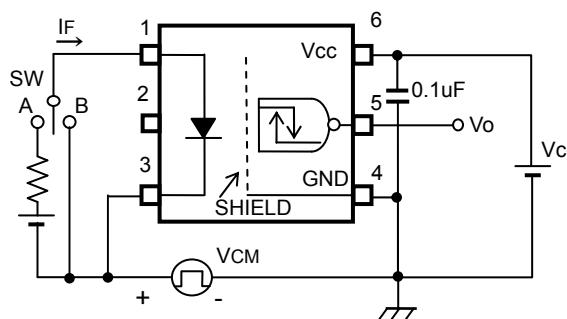
$I_F=3\text{ mA(P.G)}$
($f=50\text{ kHz}$, duty=50%
less than $t_r = t_f = 5\text{ ns}$)



CL: stray capacitance of probe and wiring (to 15 pF)



TEST CIRCUIT 9: Common-Mode Transient Immunity Test Circuit



$$CM_H = \frac{800(V)}{t_r(\mu s)} \quad CM_L = -\frac{800(V)}{t_f(\mu s)}$$

CM_H (CM_L) is the maximum rate of rise (fall) of the common mode voltage that can be sustained with the output voltage in the high (low) state.

EN60747-5-5 Option:(D4)

Types : TLP718, TLP718F

Type designations for “option: (D4)”, which are tested under EN60747 requirements.

Ex.: TLP718 (D4-TP,F) D4 : EN60747 option
 TP : Standard tape & reel type
 F : [[G]]/RoHS COMPATIBLE

Note: Use TOSHIBA standard type number for safety standard application.

Ex.: TLP718 (D4-TP,F) → TLP718

EN60747 Isolation Characteristics

Description	Symbol	Rating	Unit
Application classification for rated mains voltage≤300V _{rms} for rated mains voltage≤600V _{rms}		I-IV I-III	—
Climatic classification		40/ 100 / 21	—
Pollution degree		2	—
Maximum operating insulation voltage	TLPxxx type	890	V _{pk}
	TLPxxxF type	1140	
Input to output test voltage, method A V _{pr} =1.5×V _{IORM} , type and sample test t _p =10s, partial discharge<5pC	TLPxxx type	1335	V _{pk}
	TLPxxxF type	1710	
Input to output test voltage, method B V _{pr} =1.875×V _{IORM} , 100% production test t _p =1s, partial discharge<5pC	TLPxxx type	1670	V _{pk}
	TLPxxxF type	2140	
Highest permissible overvoltage (transient overvoltage, t _{pr} = 60s)	V _{TR}	8000	V _{pk}
Safety limiting values (max. permissible ratings in case of fault, also refer to thermal derating curve) current (input current I _F , P _{si} = 0) power (output or total power dissipation) temperature	I _{si}	300	mA
	P _{si}	700	mW
	T _{si}	150	°C
Insulation resistance, V _{IO} =500V, Ta=25°C V _{IO} =500V, Ta=100°C V _{IO} =500V, Ta=T _{si}	R _{si}	≥10 ¹² ≥10 ¹¹ ≥10 ⁹	Ω

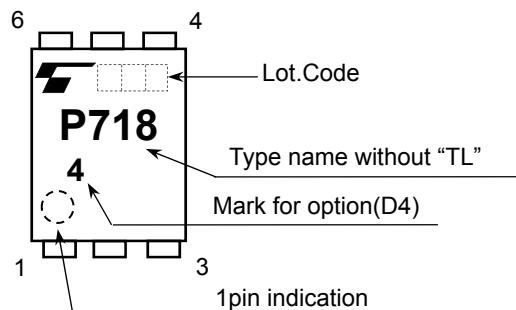
Insulation Related Specifications

		7.62mm pitch TLPxxx type	10.16mm pitch TLPxxxF type
Minimum creepage distance	Cr	7.0mm	8.0mm
Minimum clearance	Cl	7.0mm	8.0mm
Minimum insulation thickness	ti		0.4mm
Comparative tracking index	CTI		175

1. If a printed circuit is incorporated, the creepage distance and clearance may be reduced below this value. (e.g. at a standard distance between soldering eye centres of 7.5mm). If this is not permissible, the user shall take suitable measures.
2. This photocoupler is suitable for 'safe electrical isolation' only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.

Marking on product for EN60747 : **4**

Marking Example :



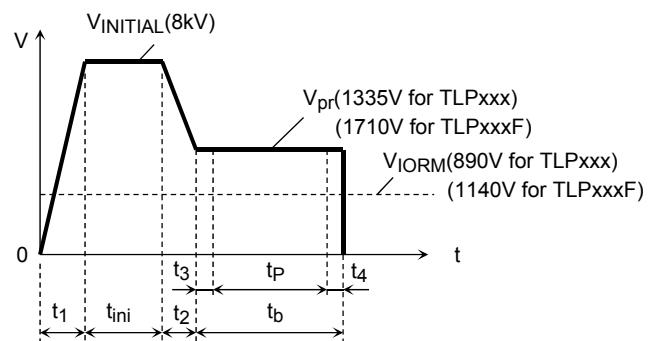
Figure

1 Partial discharge measurement procedure according to EN60747
Destructive test for qualification and sampling tests.

Method A

(for type and sampling tests,
destructive tests)

t_1, t_2	= 1 to 10 s
t_3, t_4	= 1 s
t_p (Measuring time for partial discharge)	= 10 s
t_b	= 12 s
t_{ini}	= 60 s



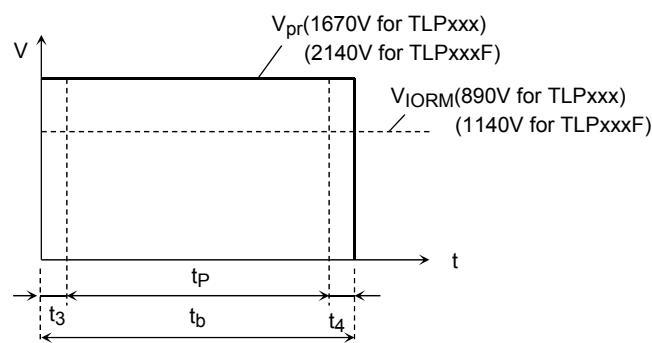
Figure

2 Partial discharge measurement procedure according to EN60747
Non-destructive test for 100% inspection.

Method B

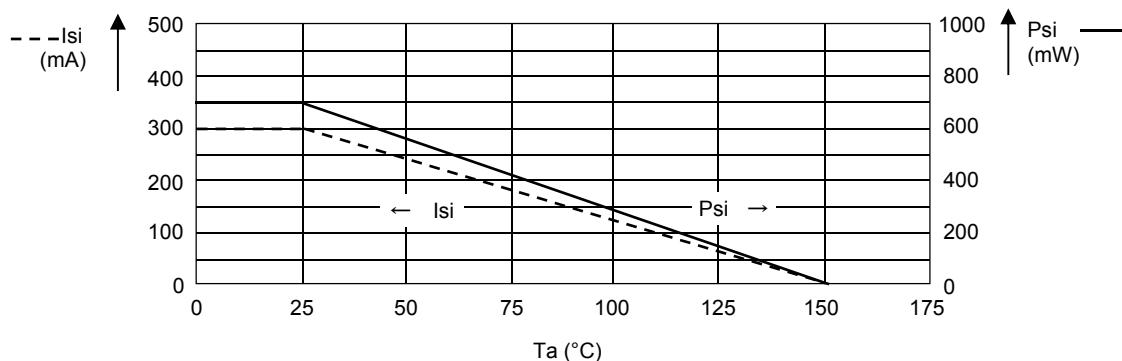
(for sample test, non-
destructive test)

t_3, t_4	= 0.1 s
t_p (Measuring time for partial discharge)	= 1 s
t_b	= 1.2 s



Figure

3 Dependency of maximum safety ratings on ambient temperature



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