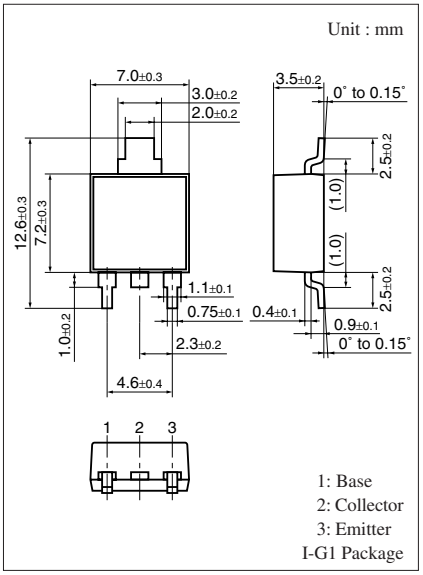
2SD1752, 2SD1752A

Silicon NPN epitaxial planar type

For power amplification and low-voltage switching
Complementary to 2SB1148 and 2SB1148A

■ Features

- Low collector-emitter saturation voltage $V_{CE(sat)}$
- High-speed switching
- Satisfactory liniarity of forward current transfer ratio h_{FE}
- Large collector current I_C
- I type package enabling direct soldering of the radiating fin to the printed circuit board, etc. of small electronic equipment



Note) Self-supported type package is also prepared.

■ Absolute Maximum Ratings $T_C = 25°C$

Parameter		Symbol	Rating	Unit
Collector-base voltage (Emitter open)	2SD1752	V_{CBO}	40	V
	2SD1752A		50	
Collector-emitter voltage (Base open)	2SD1752	V_{CEO}	20	V
	2SD1752A		40	
Emitter-base voltage (Collector open)		V_{EBO}	5	V
Collector current		I_C	10	A
Peak collector current		I_{CP}	20	A
Collector power dissipation		P_C	15	W
	$T_a = 25°C$		1.3	
Junction temperature		T_j	150	°C
Storage temperature		T_{stg}	−55 to +150	°C

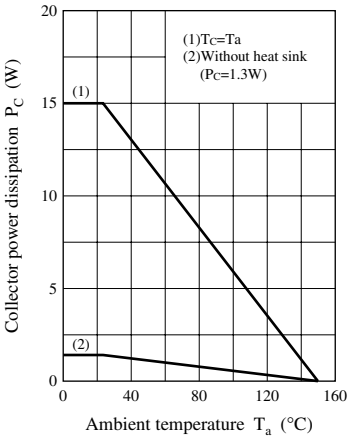
■ Electrical Characteristics $T_C = 25°C \pm 3°C$

Parameter		Symbol	Conditions	Min	Typ	Max	Unit
Collector-emitter voltage (Base open)	2SD1752	V_{CEO}	I_C = 10 mA, I_B = 0	20			V
	2SD1752A			40			
Collector-base cutoff current (Emitter open)	2SD1752	I_{CBO}	V_{CB} = 40 V, I_E = 0			50	μA
	2SD1752A		V_{CB} = 50 V, I_E = 0			50	
Emitter-base cutoff current (Collector open)		I_{EBO}	V_{EB} = 5 V, I_C = 0			50	μA
Forward current transfer ratio		h_{FE1}	V_{CE} = 2 V, I_C = 0.1 A	45			—
		h_{FE2} *	V_{CE} = 2 V, I_C = 3 A	90		260	
Collector-emitter saturation voltage		$V_{CE(sat)}$	I_C = 10 A, I_B = 0.33 A			0.6	V
Base-emitter saturation voltage		$V_{BE(sat)}$	I_C = 10 A, I_B = 0.33 A			1.5	V
Forward current transfer ratio		f_T	V_{CE} = 10 V, I_C = 0.5 A, f = 10 MHz		120		MHz
Collector output capacitance (Common base, input open circuited)		C_{ob}	V_{CB} = 10 V, I_E = 0, f = 1 MHz		200		pF
Turn-on time		t_{on}	I_C = 3 A, I_{B1} = 0.1 A, I_{B2} = − 0.1 A		0.3		μs
Storage time		t_{stg}	V_{CC} = 20 V		0.4		μs
Fall time		t_f			0.1		μs

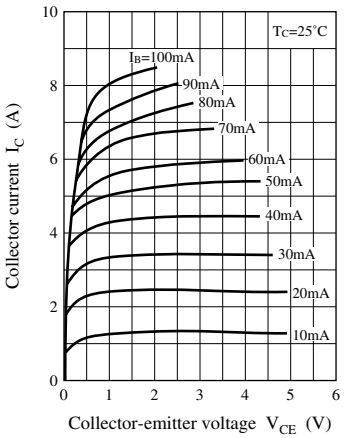
Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.
2. *: Rank classification

Rank	Q	P
h_{FE2}	90 to 180	130 to 260

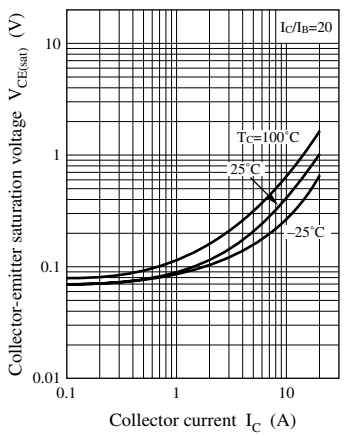
P_C — T_a



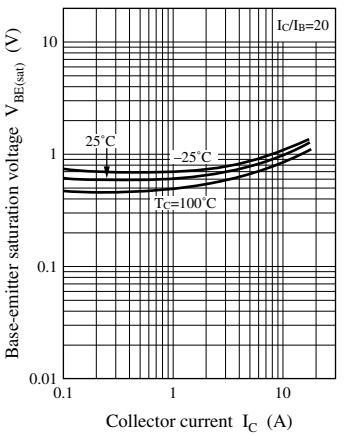
I_C — V_{CE}



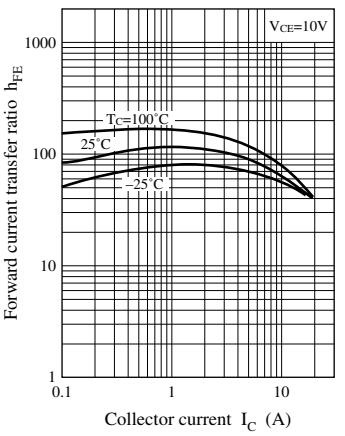
$V_{CE(sat)}$ — I_C



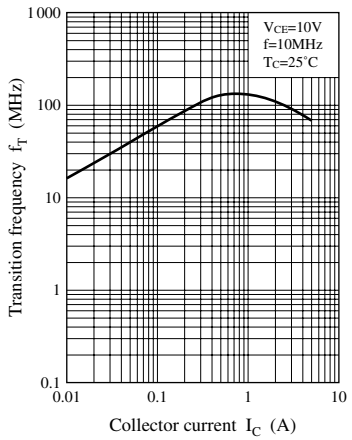
$V_{BE(sat)}$ — I_C



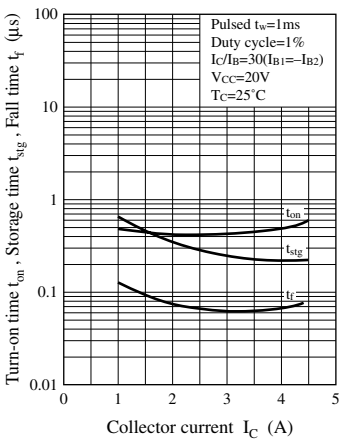
h_{FE} — I_C



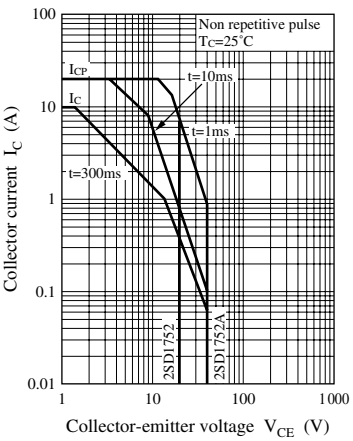
f_T — I_C

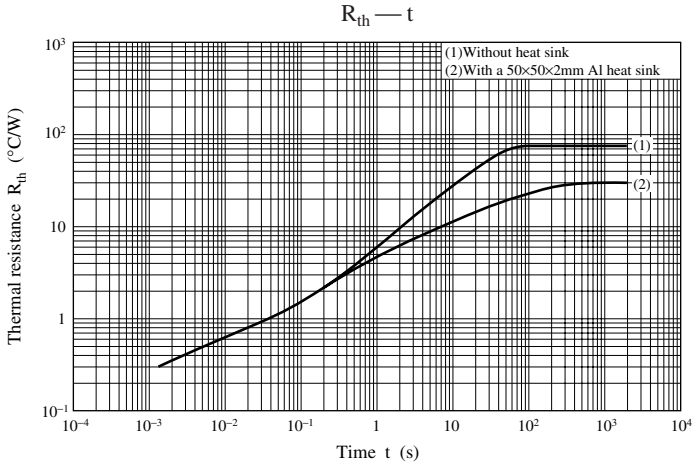


t_{on} , t_{stg} , t_f — I_C



Safe operation area




R_{th} — t
(1)Without heat sink
(2)With a 50×50×2mm Al heat sink
(1)
(2)
Thermal resistance R_{th} (°C/W)
10^3
10^2
10
1
10^{-1}
10^{-4}
10^{-3}
10^{-2}
10^{-1}
1
10
10^2
10^3
10^4
Time t (s)

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