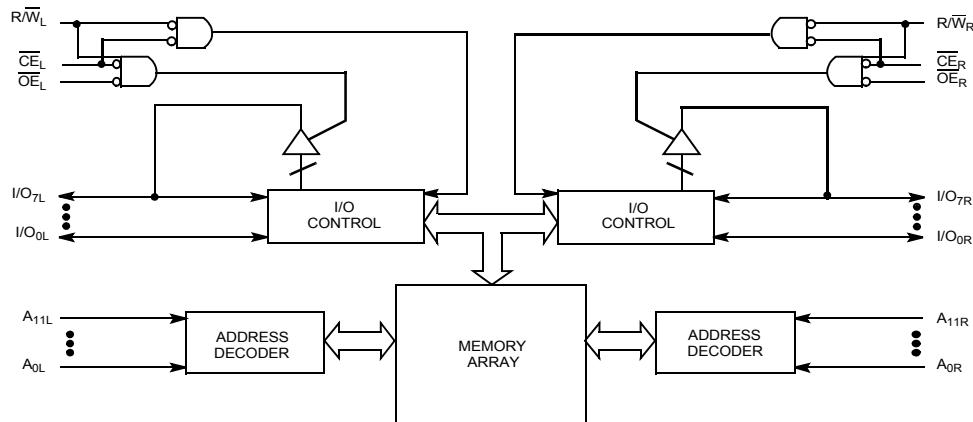


## Features

- True dual-ported memory cells, which allow simultaneous reads of the same memory location
- 4 K × 8 organization
- 0.65 micron CMOS for optimum speed and power
- High speed access: 15 ns
- Low operating power:  $I_{CC} = 180$  mA (max)
- Fully asynchronous operation
- Automatic power down
- Available in 52-pin plastic leaded chip carrier (PLCC)
- Pb-free packages available

## Logic Block Diagram



## Functional Description

The CY7C135 is a high speed CMOS 4K x 8 dual-port static RAMs. Two ports are provided permitting independent, asynchronous access for reads and writes to any location in memory. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: chip enable ( $\overline{CE}$ ), read or write enable ( $R/W$ ), and output enable ( $OE$ ). The CY7C135 is suited for those systems that do not require on-chip arbitration or are intolerant of wait states. Therefore, the user must be aware that simultaneous access to a location is possible. An automatic power down feature is controlled independently on each port by a chip enable ( $\overline{CE}$ ) pin.

The CY7C135 is available in 52-pin PLCC.

## Contents

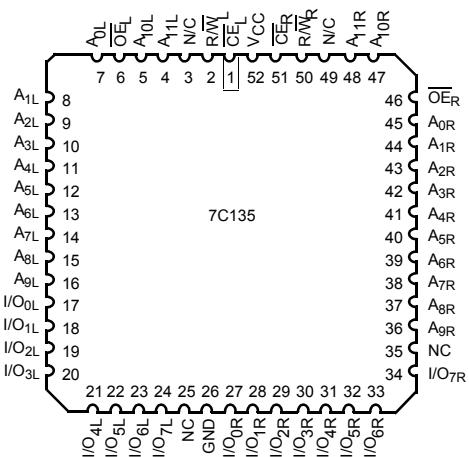
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## Selection Guide

Parameter	7C135-15	Unit
Maximum access time	15	ns
Maximum operating current	Commercial	220 mA
Maximum standby current for $I_{SB1}$	Commercial	60 mA

## Pin Configurations

Figure 1. 52-pin PLCC pinout (Top View)



## Pin Definitions

Left Port	Right Port	Description
$A_{0L}$ - $A_{11L}$	$A_{0R}$ - $A_{11R}$	Address lines
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$\overline{R/W}_L$	$\overline{R/W}_R$	Read/Write Enable

## Architecture

The CY7C135 consists of an array of 4K words of 8 bits each of dual-port RAM cells, I/O and address lines, and control signals (CE, OE, R/W).

## Functional Description

### Write Operation

Data must be set up for a duration of  $t_{SD}$  before the rising edge of R/W to guarantee a valid write. Because there is no on-chip arbitration, the user must be sure that a specific location is not accessed simultaneously by both ports or erroneous data could result. A write operation is controlled by either the  $\overline{OE}$  pin (see [Figure 6](#) on page 9) or the R/W pin (see [Figure 7](#) on page 9). Data can be written  $t_{HZOE}$  after the OE is deasserted or  $t_{HZWE}$  after the falling edge of R/W. Required inputs for write operations are summarized in [Table 1](#).

If a location is being written to by one port and the opposite port attempts to read the same location, a port-to-port flowthrough delay is met before the data is valid on the output. Data is valid

on the port wishing to read the location  $t_{DDD}$  after the data is presented on the writing port.

### Read Operation

When reading the device, the user must assert both the  $\overline{OE}$  and CE pins. Data is available  $t_{ACE}$  after CE or  $t_{DOE}$  after OE are asserted. Required inputs for read operations are summarized in [Table 1](#).

**Table 1. Non-Contending Read/Write**

Inputs			Outputs	Operation
CE	R/W	OE	$I/O_0-I/O_7$	
H	X	X	High Z	Power-down
X	X	H	High Z	I/O Lines disabled
L	H	L	Data out	Read
L	L	X	Data in	Write

## Maximum Ratings

Exceeding maximum ratings <sup>[1]</sup> may shorten the useful life of the device. User guidelines are not tested.

Storage temperature .....  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$

Ambient temperature with power applied .....  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

Supply voltage to ground potential (Pin 48 to Pin 24) .....  $-0.5\text{ V}$  to  $+7.0\text{ V}$

DC voltage applied to outputs in High Z state .....  $-0.5\text{ V}$  to  $+7.0\text{ V}$

DC input voltage <sup>[2]</sup> .....  $-3.0\text{ V}$  to  $+7.0\text{ V}$

Static discharge voltage (per MIL-STD-883, Method 3015) .....  $> 2001\text{ V}$

Latch up current .....  $> 200\text{ mA}$

## Operating Range

Range	Ambient Temperature	$V_{CC}$
Commercial	$0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$	$5\text{ V} \pm 10\%$
Industrial	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	$5\text{ V} \pm 10\%$

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	7C135-15		Unit
			Min	Max	
$V_{OH}$	Output HIGH voltage	$V_{CC} = \text{Min}$ , $I_{OH} = -4.0\text{ mA}$	2.4	—	V
$V_{OL}$	Output LOW voltage	$V_{CC} = \text{Min}$ , $I_{OL} = 4.0\text{ mA}$	—	0.4	V
$V_{IH}$	Input HIGH voltage		2.2	—	V
$V_{IL}$	Input LOW voltage		—	0.8	V
$I_{IX}$	Input load current	$\text{GND} \leq V_I \leq V_{CC}$	-10	+10	$\mu\text{A}$
$I_{OZ}$	Output leakage current	Outputs disabled, $\text{GND} \leq V_O \leq V_{CC}$	-10	+10	$\mu\text{A}$
$I_{CC}$	Operating current	$V_{CC} = \text{Max}$ , $I_{OUT} = 0\text{ mA}$	Commercial	220	mA
			Industrial	—	
$I_{SB1}$	Standby current (Both ports TTL levels)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$ , $f = f_{MAX}^{[3]}$	Commercial	60	mA
			Industrial	—	
$I_{SB2}$	Standby current (One port TTL level)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$ , $f = f_{MAX}^{[3]}$	Commercial	130	mA
			Industrial	—	
$I_{SB3}$	Standby current (Both ports CMOS levels)	Both ports $\overline{CE}$ and $\overline{CE}_R \geq V_{CC} - 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$ , $f = 0^{[3]}$	Commercial	15	mA
			Industrial	—	
$I_{SB4}$	Standby current (One port CMOS level)	One port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC} - 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$ , Active port outputs, $f = f_{MAX}^{[3]}$	Commercial	125	mA
			Industrial	—	

### Notes

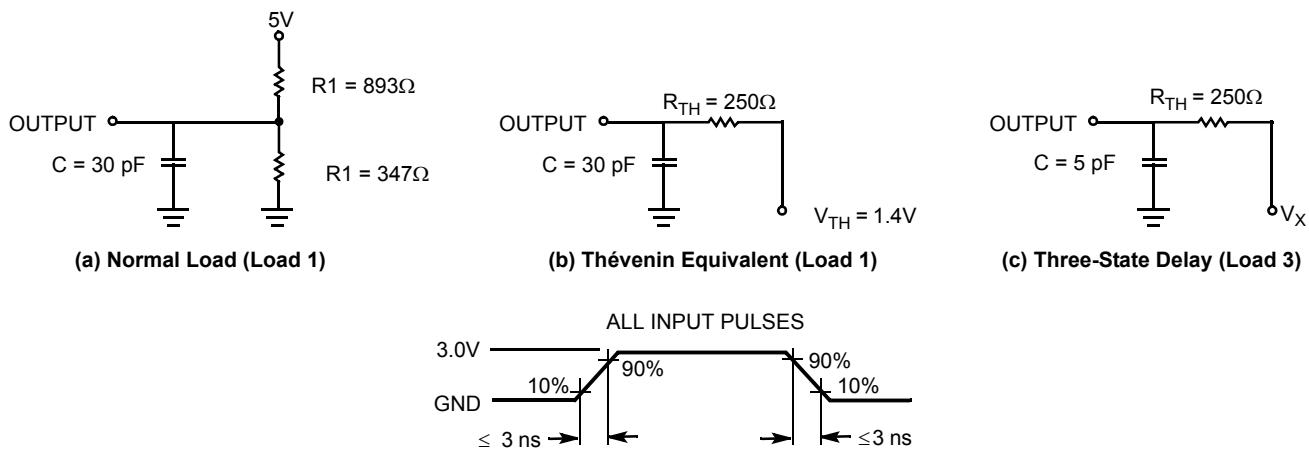
1. The voltage on any input or I/O pin cannot exceed the power pin during power up.
2. Pulse width  $< 20\text{ ns}$ .
3.  $f_{MAX} = 1/t_{RC}$  = All inputs cycling at  $f = 1/t_{RC}$  (except output enable).  $f = 0$  means no address or control lines change. This applies only to inputs at CMOS level standby  $I_{SB3}$ .

## Capacitance

Parameter <sup>[4]</sup>	Description	Test Conditions	Max	Unit
$C_{IN}$	Input capacitance	$T_A = 25^\circ C, f = 1 \text{ MHz}, V_{CC} = 5.0 \text{ V}$	10	pF
$C_{OUT}$	Output capacitance		10	pF

## AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



### Note

4. Tested initially and after any design or process changes that may affect these parameters.

## Switching Characteristics

Over the Operating Range

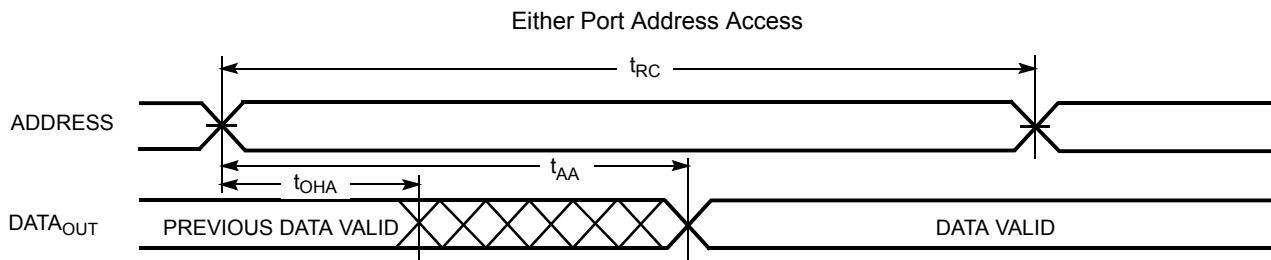
Parameter <sup>[5]</sup>	Description	7C135-15		Unit
		Min	Max	
<b>Read Cycle</b>				
$t_{RC}$	Read cycle time	15	—	ns
$t_{AA}$	Address to data valid	—	15	ns
$t_{OHA}$	Output hold from address change	3	—	ns
$t_{ACE}$	CE LOW to data valid	—	15	ns
$t_{DOE}$	OE LOW to data valid	—	10	ns
$t_{LZOE}^{[6, 7, 8]}$	OE Low to Low Z	3	—	ns
$t_{HZOE}^{[6, 7, 8]}$	OE HIGH to High Z	—	10	ns
$t_{LZCE}^{[6, 7, 8]}$	CE LOW to Low Z	3	—	ns
$t_{HZCE}^{[6, 7, 8]}$	CE HIGH to High Z	—	10	ns
$t_{PU}^{[8]}$	CE LOW to Power-up	0	—	ns
$t_{PD}^{[8]}$	CE HIGH to Power-down	—	15	ns
<b>Write Cycle</b>				
$t_{WC}$	Write cycle time	15	—	ns
$t_{SCE}$	CE LOW to Write End	12	—	ns
$t_{AW}$	Address setup to Write End	12	—	ns
$t_{HA}$	Address hold from Write End	2	—	ns
$t_{SA}$	Address setup to Write Start	0	—	ns
$t_{PWE}$	Write pulse width	12	—	ns
$t_{SD}$	Data setup to Write End	10	—	ns
$t_{HD}$	Data hold from Write End	0	—	ns
$t_{HZWE}^{[7, 8]}$	R/W LOW to High Z	—	10	ns
$t_{LZWE}^{[7, 8]}$	R/W HIGH to Low Z	3	—	ns
$t_{WDD}^{[9]}$	Write pulse to data delay	—	30	ns
$t_{DDD}^{[9]}$	Write data valid to read data valid	—	25	ns

### Notes

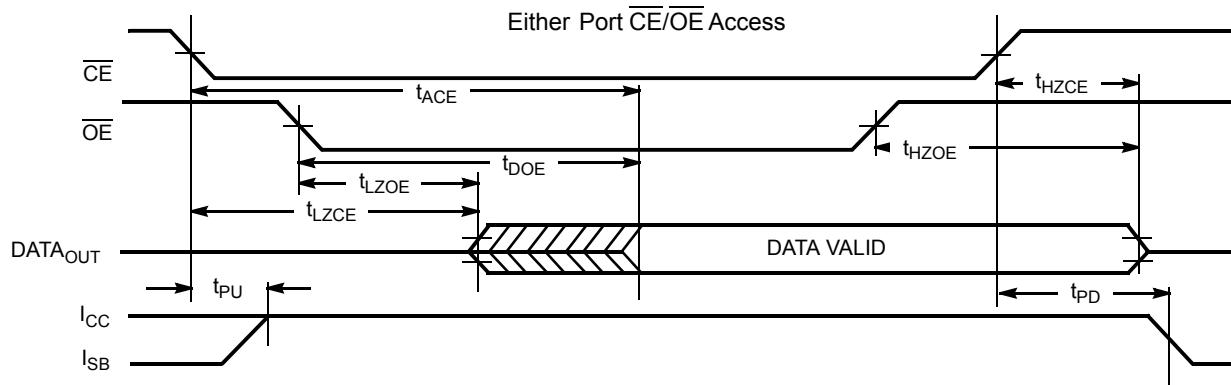
5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30 pF load capacitance.
6. At any given temperature and voltage condition for any given device,  $t_{HZCE}$  is less than  $t_{LZCE}$  and  $t_{HZOE}$  is less than  $t_{LZOE}$ .
7. Test conditions used are Load 3.
8. This parameter is guaranteed but not tested.
9. For information on port-to-port delay through RAM cells from writing port to reading port, refer to [Figure 5](#) on page 8.

## Switching Waveforms

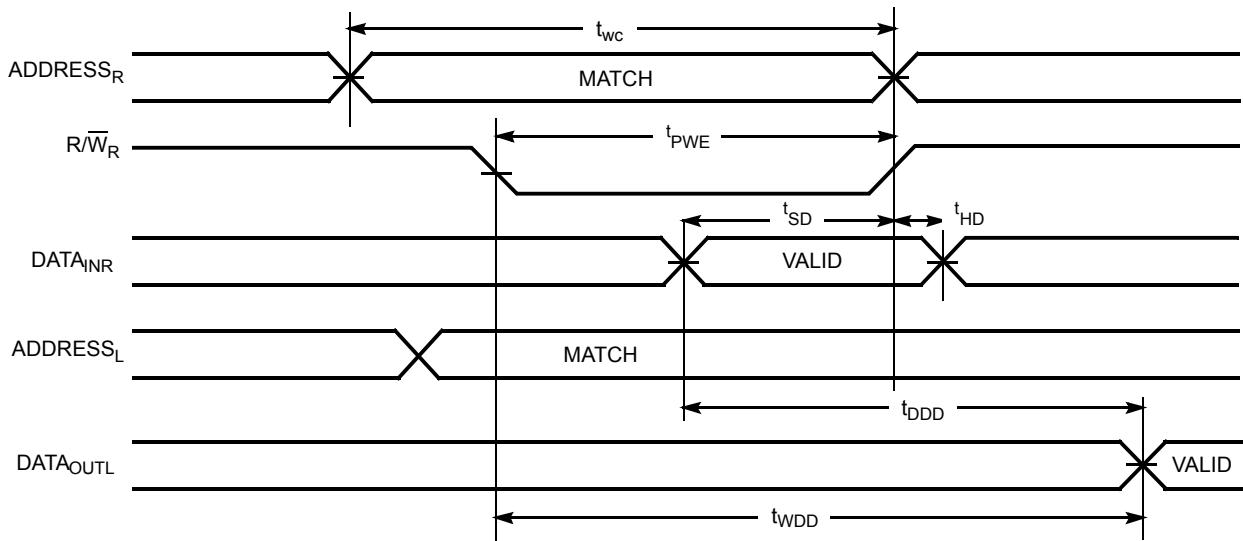
**Figure 3. Read Cycle No. 1** [10, 11]



**Figure 4. Read Cycle No. 2** [10, 12]



**Figure 5. Read Timing with Port-to-Port** [13]

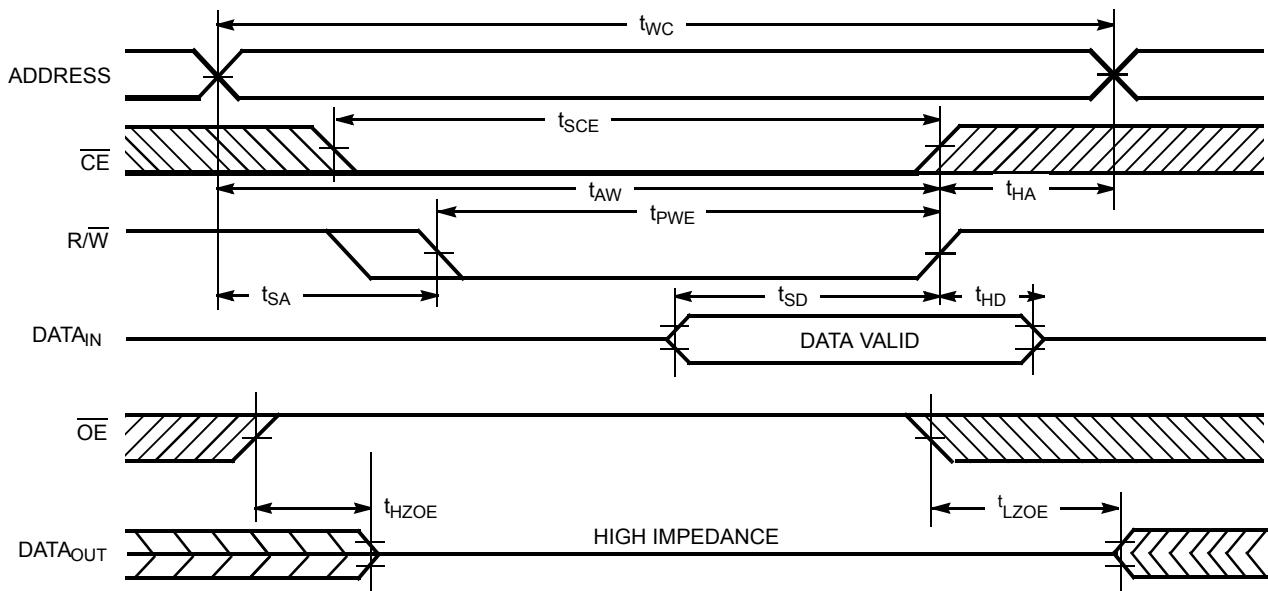


### Notes

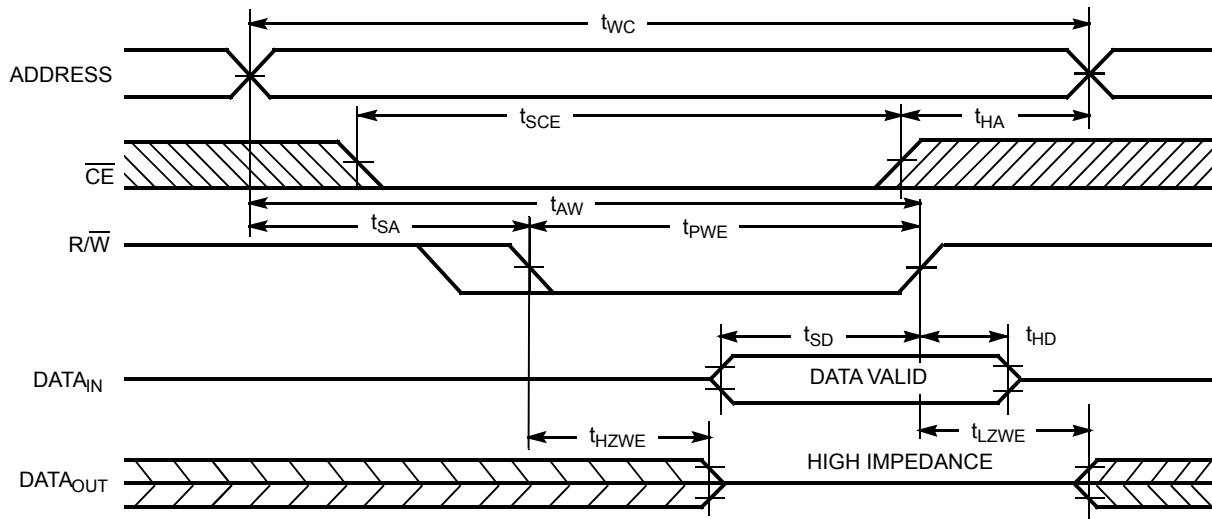
10. R/W is HIGH for read cycle.
11. Device is continuously selected,  $\overline{CE} = V_{IL}$  and  $\overline{OE} = V_{IL}$ .
12. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
13.  $\overline{CE}_L = \overline{CE}_R = \text{LOW}$ ;  $R/W_L = \text{HIGH}$ .

## Switching Waveforms (continued)

**Figure 6. Write Cycle No. 1:  $\overline{\text{OE}}$  Three-States Data I/Os (Either Port)** [14, 15, 16]



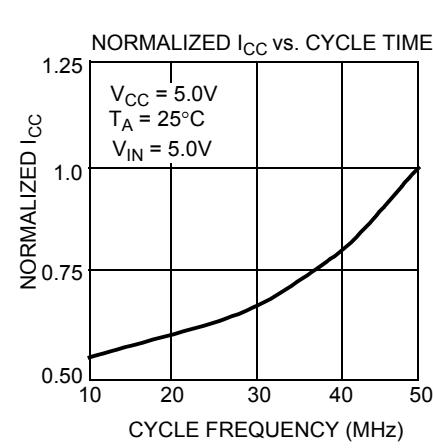
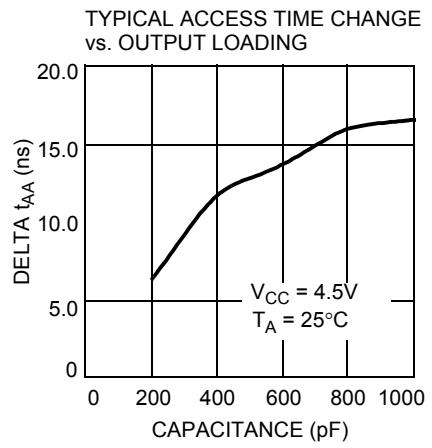
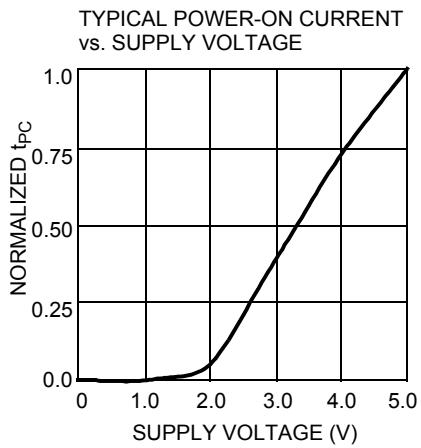
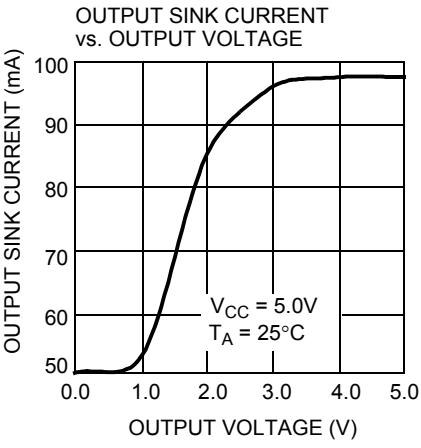
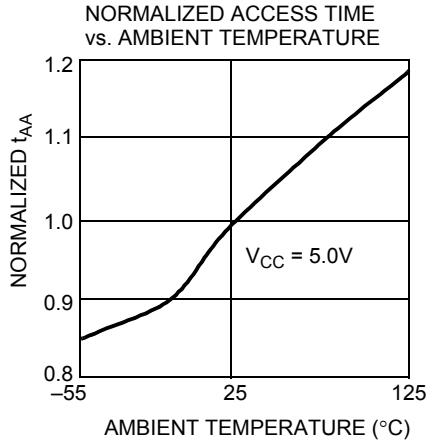
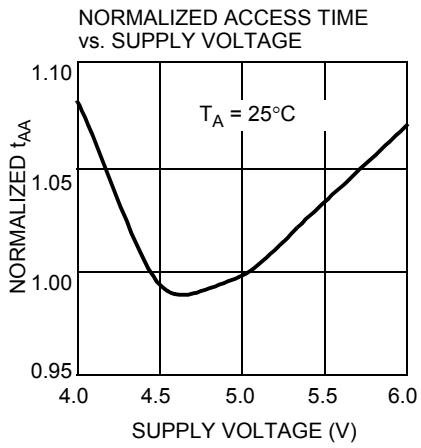
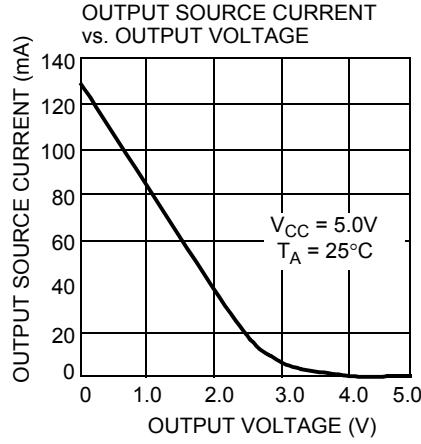
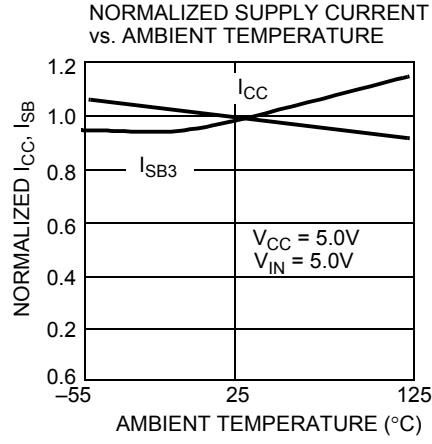
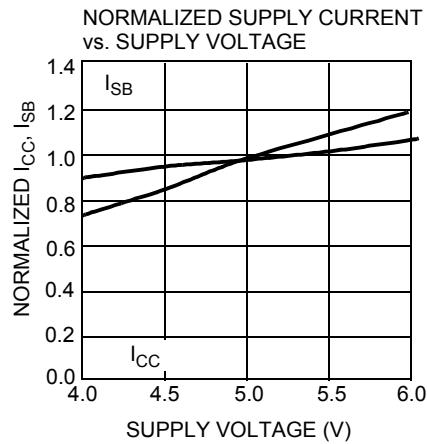
**Figure 7. Write Cycle No. 2:  $\overline{\text{R/W}}$  Three-States Data I/Os (Either Port)** [15, 17]



### Notes

14. The internal write time of the memory is defined by the overlap of  $\overline{\text{CE}}$  and  $\overline{\text{R/W}}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
15.  $\overline{\text{R/W}}$  must be HIGH during all address transactions.
16. If  $\overline{\text{OE}}$  is LOW during a  $\overline{\text{R/W}}$  controlled write cycle, the write pulse width must be the larger of  $t_{PWE}$  or  $(t_{HZWE} + t_{SP})$  to allow the I/O drivers to turn off and data to be placed on the bus for the required  $t_{SD}$ . If  $\overline{\text{OE}}$  is HIGH during a  $\overline{\text{R/W}}$  controlled write cycle (as in this example), this requirement does not apply and the write pulse can be as short as the specified  $t_{PWE}$ .
17. Data I/O pins enter high impedance when  $\overline{\text{OE}}$  is held LOW during write.

## Typical DC and AC Characteristics

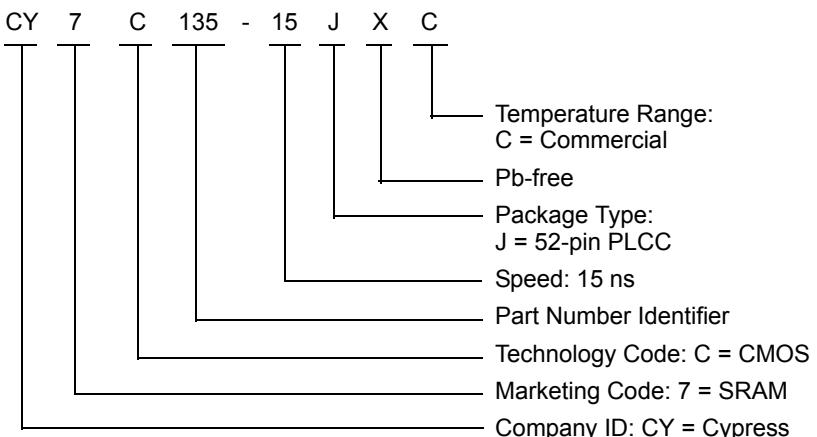


## Ordering Information

### 4 K × 8 Dual-Port SRAM

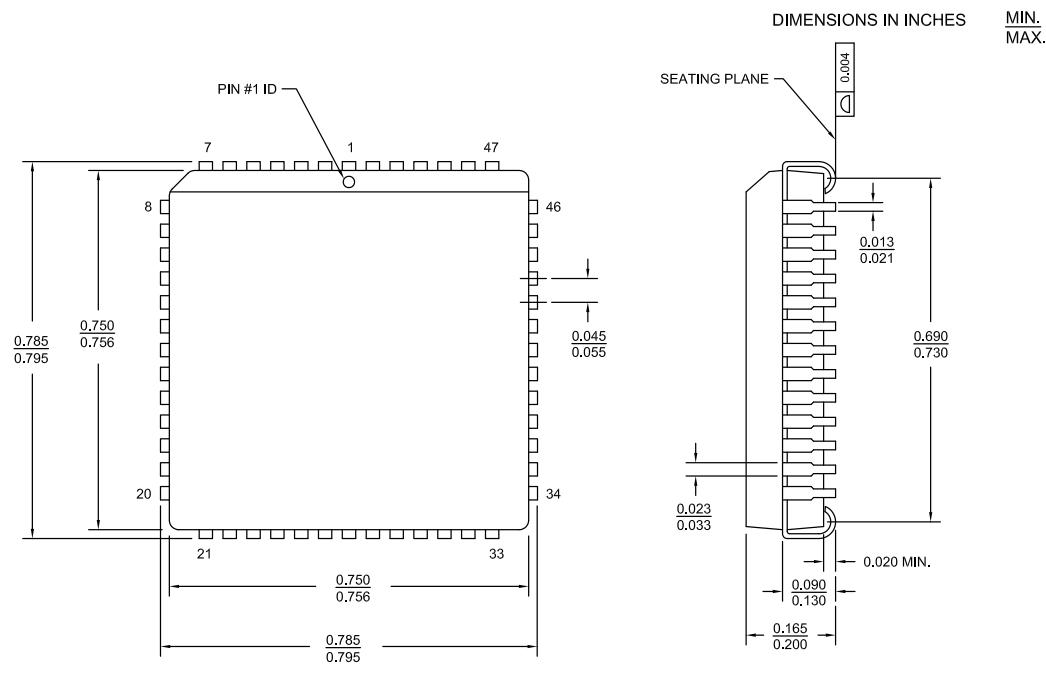
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C135-15JXC	J69	52-pin PLCC (Pb-free)	Commercial

### Ordering Code Definitions



## Package Diagram

Figure 8. 52-pin PLCC (0.756 x 0.756 Inches) J52 Package Outline, 51-85004



51-85004 \*D

## Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
PLCC	Plastic Leaded Chip Carrier
SRAM	Static Random Access Memory
TQFP	Thin Quad Flat Pack

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mV	millivolt
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY7C135, 4 K x 8 Dual-Port Static RAM Document Number: 38-06038				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	110181	SZV	10/21/01	Change from Spec number: 38-00541 to 38-06038
*A	122288	RBI	12/27/02	Updated <a href="#">Maximum Ratings</a> : Added Power up requirements (Added Note 1 and referred the same in maximum ratings).
*B	236763	YDT	SEE ECN	Updated <a href="#">Features</a> : Removed cross information from features section
*C	393413	YIM	See ECN	Added Pb-free Logo.  Updated <a href="#">Ordering Information</a> : Added Pb-free parts (CY7C135-15JXC, CY7C135-25JXC).
*D	2623540	VKN / PYRS	12/17/08	Updated <a href="#">Ordering Information</a> : Added CY7C135A parts. Removed CY7C1342 from the ordering information table.
*E	2897217	RAM	03/22/2010	Updated <a href="#">Ordering Information</a> . Updated <a href="#">Package Diagram</a> .
*F	3081925	ADMU	11/10/2010	Added <a href="#">Ordering Code Definitions</a> . Added <a href="#">Acronyms and Units of Measure</a> . Updated all the footnotes Updated the data sheet as per new template
*G	3805117	SMCH	11/07/2012	Updated Document Title to read as "CY7C135, 4 K x 8 Dual-Port Static RAM". Updated <a href="#">Features</a> (Changed value of $I_{CC}$ from 160 mA to 180 mA, removed CY7C1342 related information). Updated <a href="#">Functional Description</a> (Removed CY7C135A, CY7C1342 related information, removed the Note "CY7C135 and CY7C135A are functionally identical" and its reference). Updated <a href="#">Logic Block Diagram</a> (Removed Semaphore Arbitration (related to CY7C1342)). Updated <a href="#">Selection Guide</a> (Removed CY7C135A, CY7C1342 related information, removed 20 ns, 35 ns, 55 ns speed bins related information). Updated <a href="#">Pin Configurations</a> (Removed CY7C135A, CY7C1342 related information). Updated <a href="#">Pin Definitions</a> (Removed <u>SEM</u> (related to CY7C1342)). Updated <a href="#">Architecture</a> (Removed CY7C135A, CY7C1342 related information). Updated <a href="#">Functional Description</a> (Updated <a href="#">Read Operation</a> (Removed CY7C1342 related information), removed Semaphore Operation, updated <a href="#">Table 1</a> (Removed CY7C1342 related information), removed the table "Semaphore Operation Example"). Updated <a href="#">Electrical Characteristics</a> (Removed CY7C135A, CY7C1342 related information, removed 20 ns speed bin related information). Removed Electrical Characteristics (Corresponding to CY7C135 and CY7C1342 with 35 ns, 55 ns speed bins). Updated <a href="#">Switching Characteristics</a> (Removed CY7C135A, CY7C1342 related information, removed 20 ns, 35 ns, 55 ns speed bins related information, removed the Note "Semaphore timing applies only to CY7C1342." and its reference). Updated <a href="#">Switching Waveforms</a> (Removed CY7C135A, CY7C1342 related information). Updated <a href="#">Package Diagram</a> (spec 51-85004 (Changed revision from *B to *C)).

## Document History Page (continued)

<b>Document Title:</b> CY7C135, 4 K × 8 Dual-Port Static RAM <b>Document Number:</b> 38-06038				
<b>Rev.</b>	<b>ECN No.</b>	<b>Orig. of Change</b>	<b>Submission Date</b>	<b>Description of Change</b>
*H	4202909	SMCH	11/26/2013	<p>Updated <a href="#">Ordering Information</a> (Updated part numbers).</p> <p>Updated <a href="#">Package Diagram</a>: spec 51-85004 – Changed revision from *C to *D.</p> <p>Updated in new template.</p> <p>Completing Sunset Review.</p>
*I	4264122	SMCH	01/27/2014	Removed 25 ns speed bin related information across the document.

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