High Temperature, High Voltage, Latch-Up Proof, 8-Channel Multiplexer

Data Sheet

ADG5298

FEATURES

- **Extreme high temperature operation up to 210°C**
- **Latch-up proof**
- **JESD78D Class II rating**
- **Low leakage**
- **Ultralow capacitance and charge injection**
  - **Source capacitance, off: 2.9 pF at ±15 V dual supply**
  - **Drain capacitance, off: 34 pF at ±15 V dual supply**
  - **Charge injection: 0.2 pC at ±15 V dual supply and +12 V single supply**
- **Low on resistance: 290 Ω typical for dual supply at 210°C**
- **±9 V to ±22 V dual-supply operation**
- **9 V to 40 V single-supply operation**
- **48 V supply maximum rating**
- **Fully specified at ±15 V, ±20 V, +12 V, and +36 V**
- **V_{SS} to V_{DD} analog signal range**

APPLICATIONS

- **Downhole drilling and instrumentation**
- **Avionics**
- **Heavy industrial**
- **High temperature environments**

GENERAL DESCRIPTION

The ADG5298 is a latch-up proof, monolithic, complementary metal-oxide semiconductor (CMOS) analog multiplexer designed for operation up to 210°C. The ADG5298 switches one of eight inputs to a common output, as determined by the 3-bit binary address lines, A0, A1, and A2.

An EN input enables or disables the device. When EN is disabled, all channels switch off. The ultralow capacitance and charge injection of this switch makes it an ideal solution for data acquisition and sample-and-hold applications, where low glitch and fast settling are required.

The switch conducts equally well in both directions when on, and it has an input signal range that extends to the power supplies. In the off condition, signal levels up to the supplies are blocked.

This multiplexer is available in a 16-lead ceramic flat package (FLATPACK) and a 16-lead ceramic flat package with reverse formed gullwing leads (FLATPACK_RF). Both packages are designed for robustness at extreme temperatures and are qualified for up to 1000 hours of operation at the maximum temperature rating.

The ADG5298 is a member of a growing series of high temperature qualified products offered by Analog Devices, Inc. For a complete selection table of available high temperature products, see the high temperature product list and qualification data available at www.analog.com/hightemp.

FUNCTIONAL BLOCK DIAGRAM

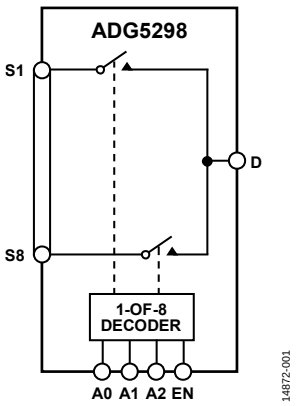

Figure 1.

PRODUCT HIGHLIGHTS

1. Trench Isolation Guards Against Latch-Up and Minimizes Parasitic Leakage.
   A dielectric trench separates the P channel and N channel transistors to prevent latch-up even under severe overvoltage conditions.
2. Achieved JESD78D Class II rating.
   The ADG5298 was stressed to ±500 mA with a 10 ms pulse at the maximum temperature of the device (210°C).
3. 0.2 pC Charge Injection.
4. Dual-Supply Operation.
   For applications where the analog signal is bipolar, the ADG5298 can operate from dual supplies of up to ±22 V.
5. Single-Supply Operation.
   For applications where the analog signal is unipolar, the ADG5298 can operate from a single rail power supply of up to 40 V.
6. 3 V Logic-Compatible Digital Inputs.
   V_{INH} = 2.0 V, V_{INL} = 0.8 V.
7. No Logic Power Supply (V_L) Required.

Rev. 0 **Document Feedback**

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
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- ADG5298 Evaluation Board

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Data Sheet

- ADG5298: High Temperature, High Voltage, Latch-Up Proof, 8-Channel Multiplexer Data Sheet

User Guides

- UG-1038: Evaluating the ADG5298, High Temperature, High Voltage, Latch-Up Proof, 8-Channel Multiplexer

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- ADG5298 IBIS Model

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REVISION HISTORY

9/2016—Revision 0: Initial Version

SPECIFICATIONS

±15 V DUAL-SUPPLY

V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, and −55°C ≤ T_A ≤ +210°C, unless otherwise noted.

Table 1.

Parameter	Symbol[1]	Test Conditions/Comments[1]	Min	Typ[2]	Max	Unit
ANALOG SWITCH						
Analog Signal Range			V_{SS}		V_{DD}	V
On Resistance	R_{ON}	Supply voltage (V_S) = ±10 V, drain source current (I_{DS}) = −1 mA, see Figure 31; for maximum R_{ON}, V_{DD} = +13.5 V, V_{SS} = −13.5 V		290	400	Ω
On-Resistance Match Between Channels	ΔR_{ON}	V_S = ±10 V, I_{DS} = −1 mA		2.0	10	Ω
On-Resistance Flatness	$R_{FLAT (ON)}$	V_S = ±10 V, I_{DS} = −1 mA		60	130	Ω
LEAKAGE CURRENTS		V_{DD} = +16.5 V, V_{SS} = −16.5 V				
Source Off Leakage	I_S (off)	V_S = ±10 V, V_D = ∓ 10 V, see Figure 32	−8	±0.005	+8	nA
Drain Off Leakage	I_D (off)	V_S = ±10 V, V_D = ∓ 10 V, see Figure 32	−60	±0.005	+60	nA
Channel On Leakage	I_D (on), I_S (on)	V_S = V_D = ±10 V, see Figure 30	−70	±0.01	+70	nA
DIGITAL INPUTS						
Input High Voltage	V_{INH}		2.0			V
Input Low Voltage	V_{INL}				0.8	V
Input Current	I_{INL} or I_{INH}	Input voltage (V_{IN}) = ground voltage (V_{GND}) or V_{DD}	−0.1	+0.002	+0.1	µA
Digital Input Capacitance	C_{IN}			3		pF
DYNAMIC CHARACTERISTICS[3]						
Transition Time	$t_{TRANSITION}$	Load resistance (R_L) = 300 Ω, load capacitance (C_L) = 35 pF, V_S = 10 V, see Figure 36		150	335	ns
On Time	t_{ON} (EN)	R_L = 300 Ω, C_L = 35 pF, V_S = 10 V, see Figure 38		125	275	ns
Off Time	t_{OFF} (EN)	R_L = 300 Ω, C_L = 35 pF, V_S = 10 V, see Figure 38		160	275	ns
Break-Before-Make Time Delay	t_D	R_L = 300 Ω, C_L = 35 pF, S1 voltage (V_{S1}) = S2 voltage (V_{S2}) = 10 V, see Figure 37	25	55		ns
Charge Injection	Q_{INJ}	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, see Figure 39		0.2		pC
Off Isolation		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 34		86		dB
Channel to Channel Crosstalk		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 33		−80		dB
−3 dB Bandwidth		R_L = 50 Ω, C_L = 5 pF, see Figure 35		110		MHz
Source Capacitance, Off	C_S (off)	V_S = 0 V, frequency (f) = 1 MHz		2.9		pF
Drain Capacitance, Off	C_D (off)	V_S = 0 V, f = 1 MHz		34		pF
Source/Drain Capacitance, On	C_D (on), C_S (on)	V_S = 0 V, f = 1 MHz		37		pF
POWER REQUIREMENTS		V_{DD} = +16.5 V, V_{SS} = −16.5 V				
Supply Current						
Positive	I_{DD}	Digital inputs = 0 V or 5 V, see Figure 28		60	80	µA
Negative	I_{SS}	Digital inputs = 0 V or 5 V, see Figure 29		10	20	µA
Ground Current	I_{GND}	Digital inputs = 0 V or 5 V		60	80	µA
Supply Range	V_{DD}/V_{SS}	GND = 0 V	±9		±22	V

[1] See the Terminology section.
[2] T_A = 25°C, except for the analog switch and power requirements values, where T_A = 210°C.
[3] Guaranteed by design, not subject to production test.

±20 V DUAL SUPPLY

V_{DD} = +20 V ± 10%, V_{SS} = −20 V ± 10%, GND = 0 V, and −55°C ≤ T_A ≤ +210°C, unless otherwise noted.

Table 2.

Parameter	Symbol[1]	Test Conditions/Comments[1]	Min	Typ[2]	Max	Unit
ANALOG SWITCH						
Analog Signal Range			V_{SS}		V_{DD}	V
On Resistance	R_{ON}	V_S = ±15 V, I_{DS} = −1 mA, see Figure 31; for maximum R_{ON}, V_{DD} = +18 V, V_{SS} = −18 V		240	350	Ω
On-Resistance Match Between Channels	ΔR_{ON}	V_S = ±15 V, I_{DS} = −1 mA		1.5	10	Ω
On-Resistance Flatness	$R_{FLAT (ON)}$	V_S = ±15 V, I_{DS} = −1 mA		55	110	Ω
LEAKAGE CURRENTS		V_{DD} = +22 V, V_{SS} = −22 V				
Source Off Leakage	I_S (off)	V_S = ±15 V, V_D = ∓15 V, see Figure 32	−8	±0.005	+8	nA
Drain Off Leakage	I_D (off)	V_S = ±15 V, V_D = ∓15 V, see Figure 32	−60	±0.005	+60	nA
Channel On Leakage	I_D (on), I_S (on)	V_S = V_D = ±15 V, see Figure 30	−70	±0.01	+70	nA
DIGITAL INPUTS						
Input High Voltage	V_{INH}		2.0			V
Input Low Voltage	V_{INL}				0.8	V
Input Current	I_{INL} or I_{INH}	V_{IN} = V_{GND} or V_{DD}	−0.1	+0.002	+0.1	µA
Digital Input Capacitance	C_{IN}			3		pF
DYNAMIC CHARACTERISTICS[3]						
Transition Time	$t_{TRANSITION}$	R_L = 300 Ω, C_L = 35 pF, V_S = 10 V, see Figure 36		140	305	ns
On Time	t_{ON} (EN)	R_L = 300 Ω, C_L = 35 pF, V_S = 10 V, see Figure 38		120	245	ns
Off Time	t_{OFF} (EN)	R_L = 300 Ω, C_L = 35 pF, V_S = 10 V, see Figure 38		160	260	ns
Break-Before-Make Time Delay	t_D	R_L = 300 Ω, C_L = 35 pF, V_{S1} = V_{S2} = 10 V, see Figure 37	20	45		ns
Charge Injection	Q_{INJ}	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, see Figure 39		0.4		pC
Off Isolation		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 34		86		dB
Channel to Channel Crosstalk		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 33		−80		dB
−3 dB Bandwidth		R_L = 50 Ω, C_L = 5 pF, see Figure 35		121		MHz
Source Capacitance, Off	C_S (off)	V_S = 0 V, f = 1 MHz		2.8		pF
Drain Capacitance, Off	C_D (off)	V_S = 0 V, f = 1 MHz		33		pF
Source/Drain Capacitance, On	C_D (on), C_S (on)	V_S = 0 V, f = 1 MHz		36		pF
POWER REQUIREMENTS		V_{DD} = +22 V, V_{SS} = −22 V				
Supply Current						
Positive	I_{DD}	Digital inputs = 0 V or 5 V, see Figure 28		60	120	µA
Negative	I_{SS}	Digital inputs = 0 V or 5 V, see Figure 29		10	20	µA
Ground Current	I_{GND}	Digital inputs = 0 V or 5 V		60	120	µA
Supply Range	V_{DD}/V_{SS}	GND = 0 V	±9		±22	V

[1] See the Terminology section.
[2] T_A = 25°C, except for the analog switch and power requirements values, where T_A = 210°C.
[3] Guaranteed by design, not subject to production test.

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, and −55°C ≤ T_A ≤ +210°C, unless otherwise noted.

Table 3.

Parameter	Symbol[1]	Test Conditions/Comments[1]	Min	Typ[2]	Max	Unit
ANALOG SWITCH						
Analog Signal Range			V_{SS}		V_{DD}	V
On Resistance	R_{ON}	V_S = 0 V to 10 V, I_{DS} = −1 mA, see Figure 31; for maximum R_{ON}, V_{DD} = 10.8 V, V_{SS} = 0 V		650	800	Ω
On-Resistance Match Between Channels	ΔR_{ON}	V_S = 0 V to 10 V, I_{DS} = −1 mA		3	24	Ω
On-Resistance Flatness	$R_{FLAT (ON)}$	V_S = 0 V to 10 V, I_{DS} = −1 mA		240	380	Ω
LEAKAGE CURRENTS		V_{DD} = 13.2 V, V_{SS} = 0 V				
Source Off Leakage	I_S (off)	V_S = 1 V/10 V, V_D = 10 V/1 V, see Figure 32	−8	±0.005	+8	nA
Drain Off Leakage	I_D (off)	V_S = 1 V/10 V, V_D = 10 V/1 V, see Figure 32	−60	±0.005	+60	nA
Channel On Leakage	I_D (on), I_S (on)	V_S = V_D = 1 V/10 V, see Figure 30	−70	±0.01	+70	nA
DIGITAL INPUTS						
Input High Voltage	V_{INH}		2.0			V
Input Low Voltage	V_{INL}				0.8	V
Input Current	I_{INL} or I_{INH}	V_{IN} = V_{GND} or V_{DD}	−0.1	+0.002	+0.1	µA
Digital Input Capacitance	C_{IN}			3		pF
DYNAMIC CHARACTERISTICS[3]						
Transition Time	$t_{TRANSITION}$	R_L = 300 Ω, C_L = 35 pF, V_S = 8 V, see Figure 36		200	490	ns
On Time	t_{ON} (EN)	R_L = 300 Ω, C_L = 35 pF, V_S = 8 V, see Figure 38		180	435	ns
Off Time	t_{OFF} (EN)	R_L = 300 Ω, C_L = 35 pF, V_S = 8 V, see Figure 38		165	305	ns
Break-Before-Make Time Delay	t_D	R_L = 300 Ω, C_L = 35 pF, V_{S1} = V_{S2} = 8 V, see Figure 37	40	95		ns
Charge Injection	Q_{INJ}	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF, see Figure 39		0.2		pC
Off Isolation		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 34		−86		dB
Channel to Channel Crosstalk		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 33		−80		dB
−3 dB Bandwidth		R_L = 50 Ω, C_L = 5 pF, see Figure 35		95		MHz
Source Capacitance, Off	C_S (off)	V_S = 6 V, f = 1 MHz		3.3		pF
Drain Capacitance, Off	C_D (off)	V_S = 6 V, f = 1 MHz		38		pF
Source/Drain Capacitance, On	C_D (on), C_S (on)	V_S = 6 V, f = 1 MHz		41		pF
POWER REQUIREMENTS		V_{DD} = 13.2 V				
Supply Current						
Positive	I_{DD}	Digital inputs = 0 V or 5 V, see Figure 28		50	75	µA
Negative	I_{SS}	Digital inputs = 0 V or 5 V, see Figure 29		7.5	15	µA
Ground Current	I_{GND}	Digital inputs = 0 V or 5 V		50	75	µA
Supply Range	V_{DD}/V_{SS}	GND = 0 V, V_{SS} = 0 V	9		40	V

[1] See the Terminology section.
[2] T_A = 25°C, except for the analog switch and power requirements values, where T_A = 210°C.
[3] Guaranteed by design, not subject to production test.

36 V SINGLE SUPPLY

V_{DD} = 36 V ± 10%, V_{SS} = 0 V, GND = 0 V, and −55°C ≤ T_A ≤ +210°C, unless otherwise noted.

Table 4.

Parameter	Symbol[1]	Test Conditions/ Comments[1]	Min	Typ[2]	Max	Unit
ANALOG SWITCH						
Analog Signal Range			V_{SS}		V_{DD}	V
On Resistance	R_{ON}	V_S = 0 V to 30 V, I_{DS} = −1 mA, see Figure 31; for maximum R_{ON}, V_{DD} = 32.4 V, V_{SS} = 0 V		260	350	Ω
On-Resistance Match Between Channels	ΔR_{ON}	V_S = 0 V to 30 V, I_{DS} = −1 mA		1.5	10	Ω
On-Resistance Flatness	$R_{FLAT (ON)}$	V_S = 0 V to 30 V, I_{DS} = −1 mA		55	110	Ω
LEAKAGE CURRENTS		V_{DD} = 13.2 V, V_{SS} = 0 V				
Source Off Leakage	I_S (off)	V_S = 1 V/10 V, V_D = 10 V/1 V, see Figure 32	−8	±0.005	+8	nA
Drain Off Leakage	I_D (off)	V_S = 1 V/10 V, V_D = 10 V/1 V, see Figure 32	−60	±0.005	+60	nA
Channel On Leakage	I_D (on), I_S (on)	V_S = V_D = 1 V/10 V, see Figure 30	−70	±0.01	+70	nA
DIGITAL INPUTS						
Input High Voltage	V_{INH}		2.0			V
Input Low Voltage	V_{INL}				0.8	V
Input Current	I_{INL} or I_{INH}	V_{IN} = V_{GND} or V_{DD}	−0.1	+0.002	+0.1	µA
Digital Input Capacitance	C_{IN}			3		pF
DYNAMIC CHARACTERISTICS[3]						
Transition Time	$t_{TRANSITION}$	R_L = 300 Ω, C_L = 35 pF, V_S = 18 V, see Figure 36		170	320	ns
On Time	t_{ON} (EN)	R_L = 300 Ω, C_L = 35 pF, V_S = 18 V, see Figure 38		150	265	ns
Off Time	t_{OFF} (EN)	R_L = 300 Ω, C_L = 35 pF, V_S = 18 V, see Figure 38		180	265	ns
Break-Before-Make Time Delay	t_D	R_L = 300 Ω, C_L = 35 pF, V_{S1} = V_{S2} = 18 V, see Figure 37	20	55		ns
Charge Injection	Q_{INJ}	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF, see Figure 39		0.3		pC
Off Isolation		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 34		−86		dB
Channel to Channel Crosstalk		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 33		−80		dB
−3 dB Bandwidth		R_L = 50 Ω, C_L = 5 pF, see Figure 35		105		MHz
Source Capacitance, Off	C_S (off)	V_S = 6 V, f = 1 MHz		2.7		pF
Drain Capacitance, Off	C_D (off)	V_S = 6 V, f = 1 MHz		32		pF
Source/Drain Capacitance, On	C_D (on), C_S (on)	V_S = 6 V, f = 1 MHz		35		pF
POWER REQUIREMENTS		V_{DD} = 13.2 V				
Supply Current						
Positive	I_{DD}	Digital inputs = 0 V or 5 V, see Figure 28		80	155	µA
Negative	I_{SS}	Digital inputs = 0 V or 5 V, see Figure 29		10	20	µA
Ground Current	I_{GND}	Digital inputs = 0 V or 5 V		80	155	µA
Supply Range	V_{DD}/V_{SS}	GND = 0 V, V_{SS} = 0 V	9		40	V

[1] See the Terminology section.
[2] T_A = 25°C, except for the analog switch and power requirements values, where T_A = 210°C.
[3] Guaranteed by design, not subject to production test.

CONTINUOUS CURRENT PER CHANNEL (Sx OR D)

Table 5.

Parameter	Test Conditions/Comments	175°C	210°C	Unit
CONTINUOUS CURRENT (Sx OR D)	θ_{JA} = 70 °C/W			
V_{DD} = +15 V, V_{SS} = −15 V		10	10	mA maximum
V_{DD} = +20 V, V_{SS} = −20 V		10	10	mA maximum
V_{DD} = 12 V, V_{SS} = 0 V		6	6	mA maximum
V_{DD} = 36 V, V_{SS} = 0 V		10	10	mA maximum

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to V_{SS}	48 V
V_{DD} to GND	−0.3 V to +48 V
V_{SS} to GND	+0.3 V to −48 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, Sx or D Pins	31 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx or D Pins[2]	Data + 5%
Temperature Range	−55°C to +210°C
Junction Temperature	212°C
Reflow Soldering Peak Temperature, Pb Free	260°C (+ 0°C/− 5°C)

[1] Overvoltages at the Ax, EN, Sx, or D pins are clamped by internal diodes. Limit the current to the maximum ratings given.
[2] See Table 5.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
F-16-1[1]	70	22	°C/W
FR-16-1[1]	70	10	°C/W

[1] Thermal impedance simulated values are based on JEDEC 2s2p thermal test board. See JEDEC JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

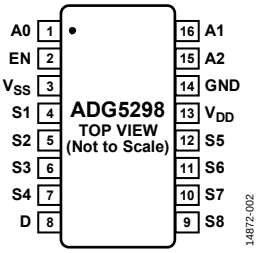

Figure 2. FLATPACK Pin Configuration

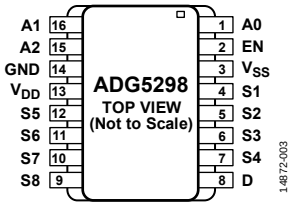

Figure 3. Reversed Formed FLATPACK Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	A0	Logic Control Input 0.
2	EN	Active High Digital Input. When low, the device is disabled and all switches are off. When high, the Ax logic inputs determine the on switches.
3	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
4	S1	Source Terminal 1. This pin can be an input or an output.
5	S2	Source Terminal 2. This pin can be an input or an output.
6	S3	Source Terminal 3. This pin can be an input or an output.
7	S4	Source Terminal 4. This pin can be an input or an output.
8	D	Drain Terminal. This pin can be an input or an output.
9	S8	Source Terminal 8. This pin can be an input or an output.
10	S7	Source Terminal 7. This pin can be an input or an output.
11	S6	Source Terminal 6. This pin can be an input or an output.
12	S5	Source Terminal 5. This pin can be an input or an output.
13	V_{DD}	Most Positive Power Supply Potential.
14	GND	Ground (0 V) Reference.
15	A2	Logic Control Input 2.
16	A1	Logic Control Input 1.

Table 9. Truth Table

A2	A1	A0	EN	On Switch
X[1]	X[1]	X[1]	0	None
0	0	0	1	S1
0	0	1	1	S2
0	1	0	1	S3
0	1	1	1	S4
1	0	0	1	S5
1	0	1	1	S6
1	1	0	1	S7
1	1	1	1	S8

[1] X is don't care.

TYPICAL PERFORMANCE CHARACTERISTICS

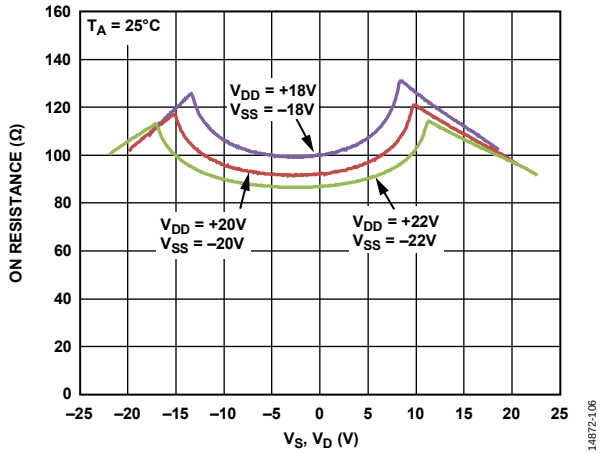

Figure 4. On Resistance (R_{ON}) as a Function of V_S, V_D (±20 V Dual Supply)

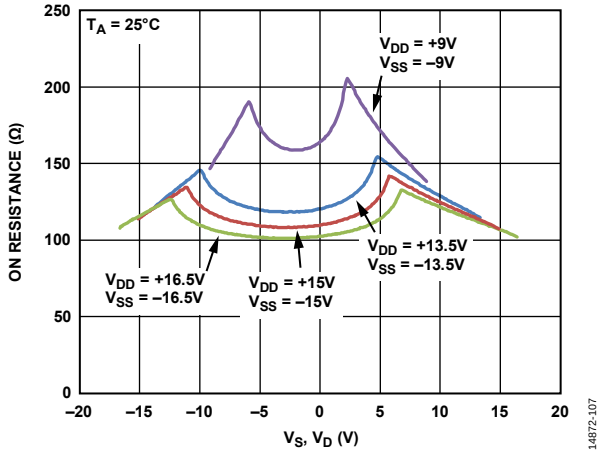

Figure 5. On Resistance (R_{ON}) as a Function of V_S, V_D (±15 V Dual Supply)

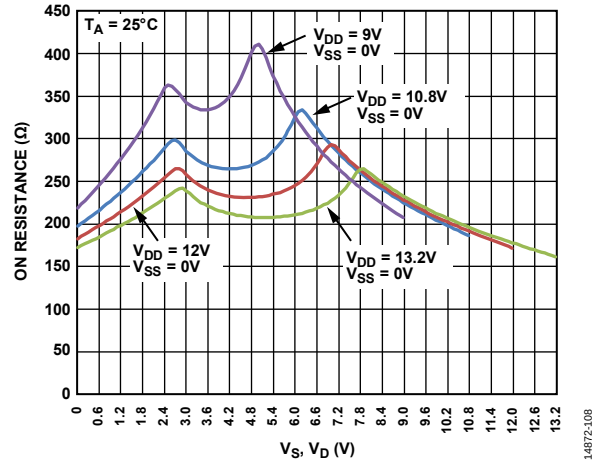

Figure 6. On Resistance (R_{ON}) as a Function of V_S, V_D (12 V Single Supply)

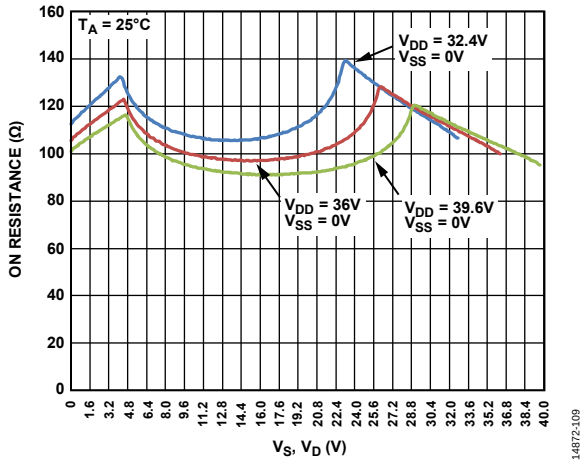

Figure 7. On Resistance (R_{ON}) as a Function of V_S, V_D (36 V Single Supply)

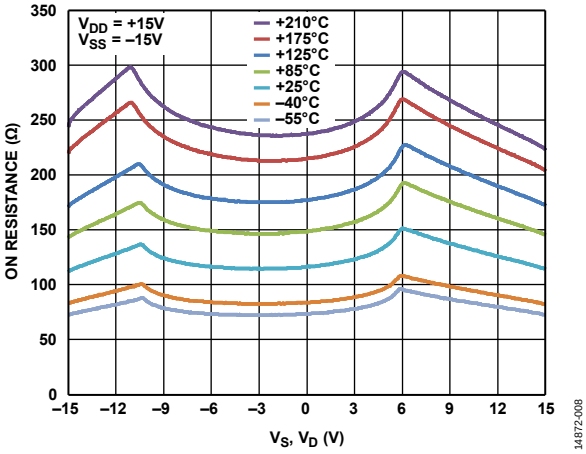

Figure 8. On Resistance (R_{ON}) as a Function of V_S, V_D for Various Temperatures, ±15 V Dual Supply

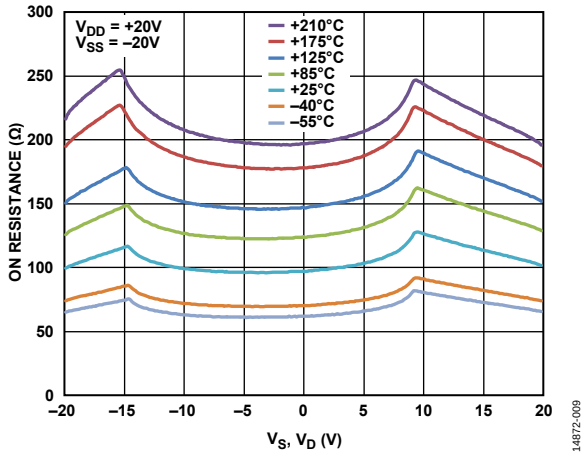

Figure 9. On Resistance (R_{ON}) as a Function of V_S, V_D for Various Temperatures, ±20 V Dual Supply

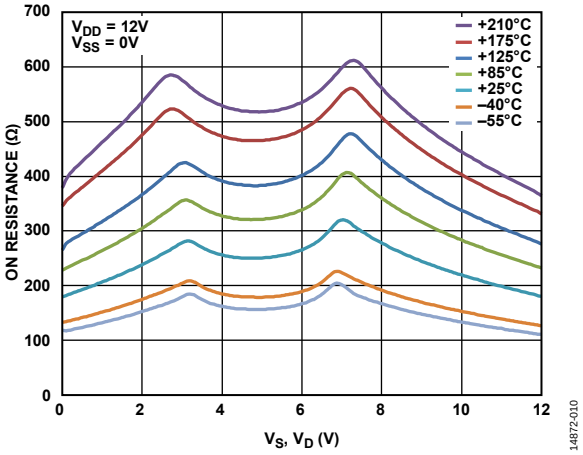

Figure 10. On Resistance (R_{ON}) as a Function of V_S, V_D for Various Temperatures, 12 V Single Supply

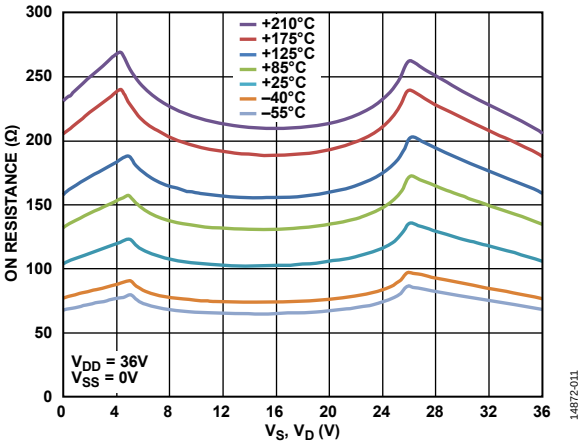

Figure 11. On Resistance (R_{ON}) as a Function of V_S, V_D for Various Temperatures, 36 V Single Supply

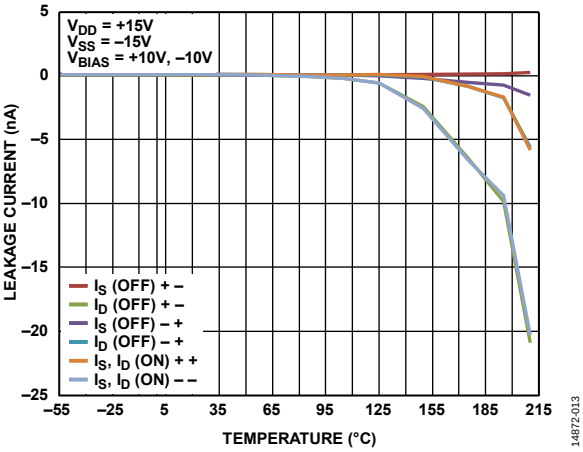

Figure 12. Leakage Currents vs. Temperature, ±15 V Dual Supply

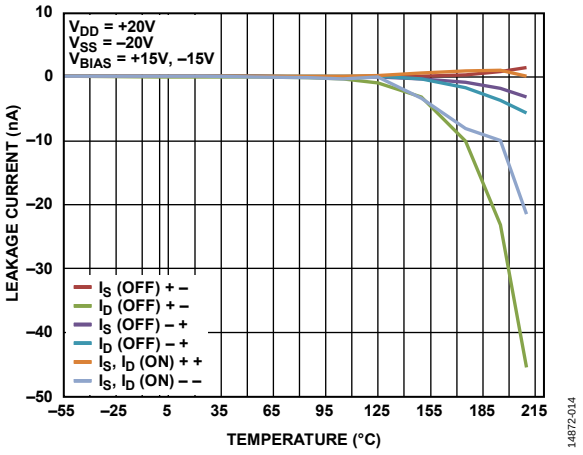

Figure 13. Leakage Current vs. Temperature, ±20 V Dual Supply

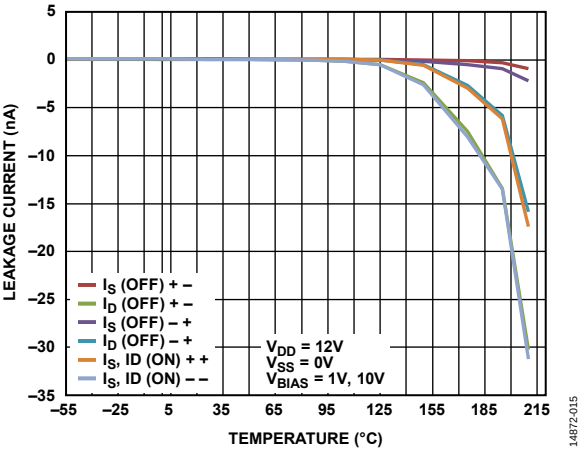

Figure 14. Leakage Current vs. Temperature, 12 V Single Supply

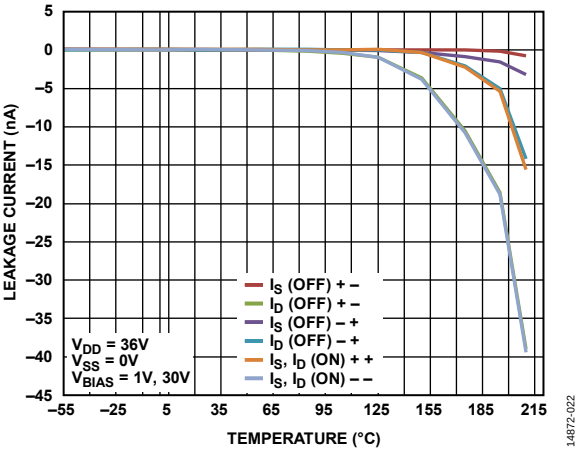

Figure 15. Leakage Current vs. Temperature, 36 V Single Supply

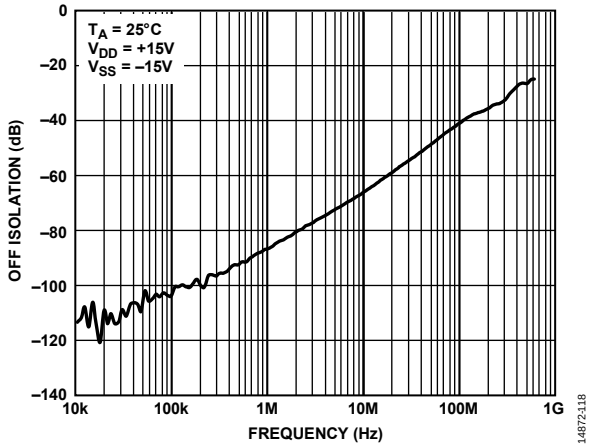

Figure 16. Off Isolation vs. Frequency, ±15 V Dual Supply

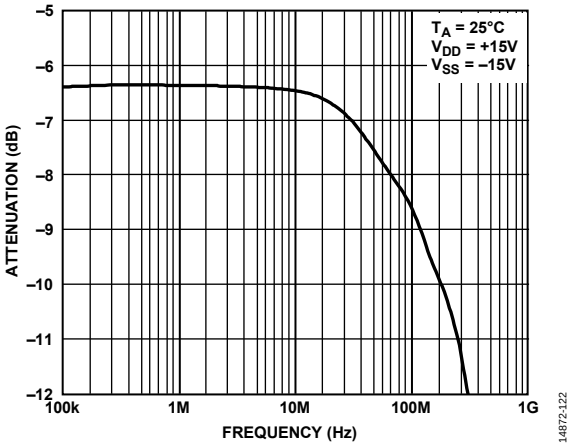

Figure 19. Attenuation vs. Frequency, ±15 V Dual Supply

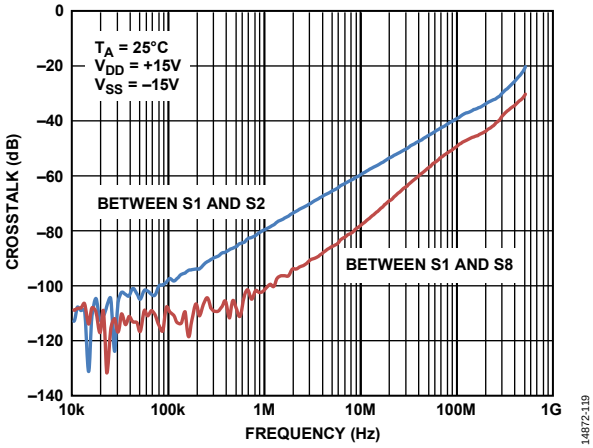

Figure 17. Crosstalk vs. Frequency, ±15 V Dual Supply

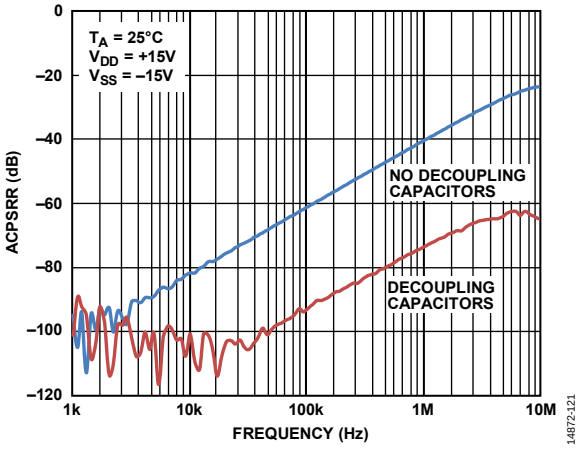

Figure 20. ACPSRR vs. Frequency, ±15 V Dual Supply

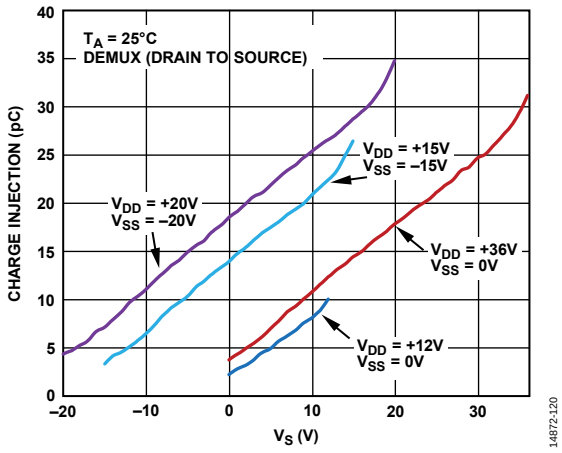

Figure 18. Charge Injection (Q_{INJ}) vs. Source Voltage (V_S), Drain to Source

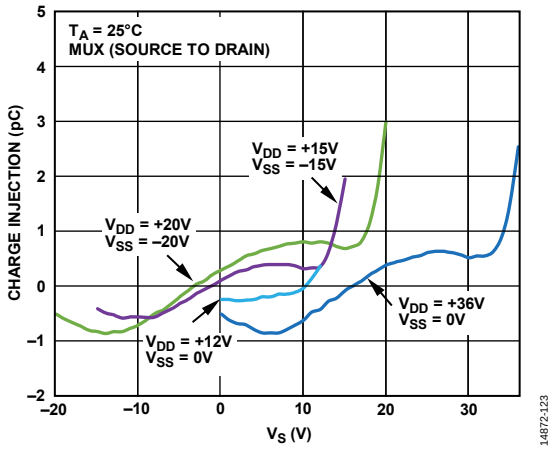

Figure 21. Charge Injection (Q_{INJ}) vs. Source Voltage (V_S), Source to Drain

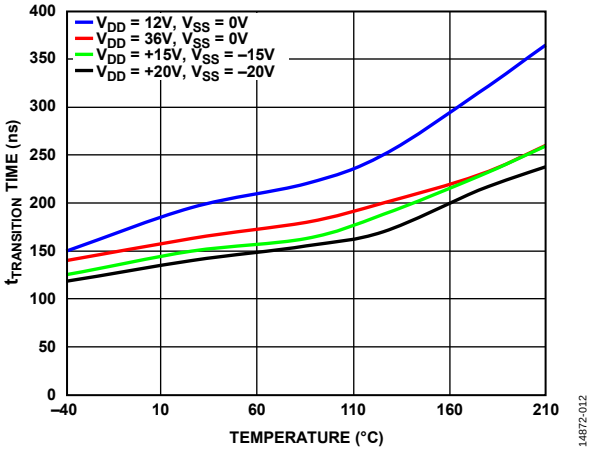

Figure 22. $t_{TRANSITION}$ Time vs. Temperature

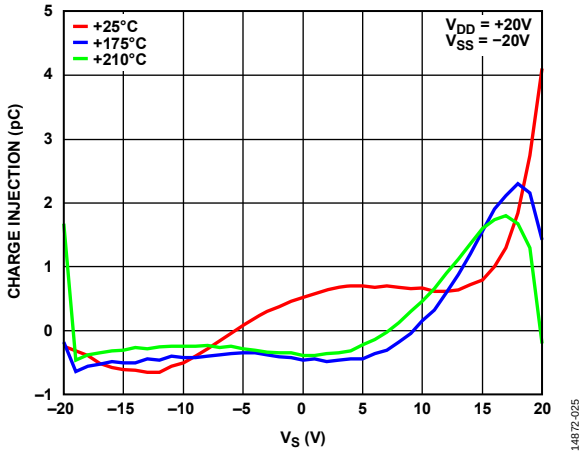

Figure 25. Charge Injection as a Function of V_S for Various Temperatures, ±20 V Dual Supply

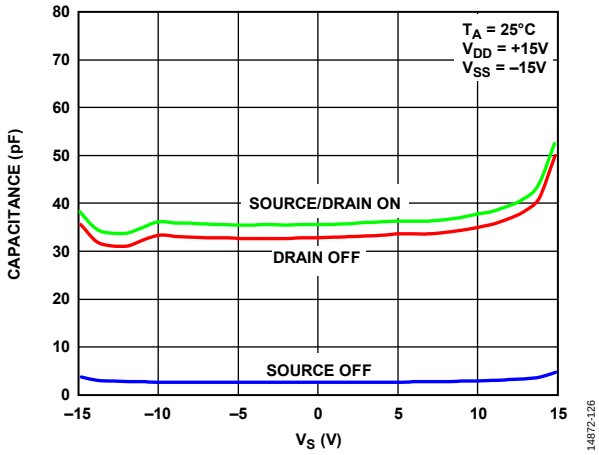

Figure 23. Capacitance vs. Source Voltage(V_S), ±15 V Dual Supply

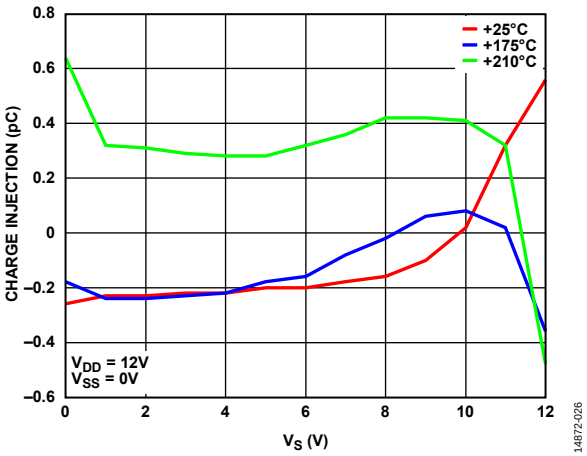

Figure 26. Charge Injection as a Function of V_S for Various Temperatures, 12 V Single Supply

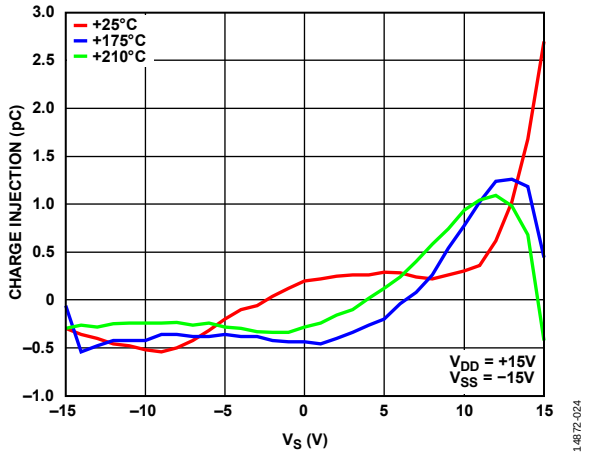

Figure 24. Charge Injection as a Function of V_S for Various Temperatures, ±15 V Dual Supply

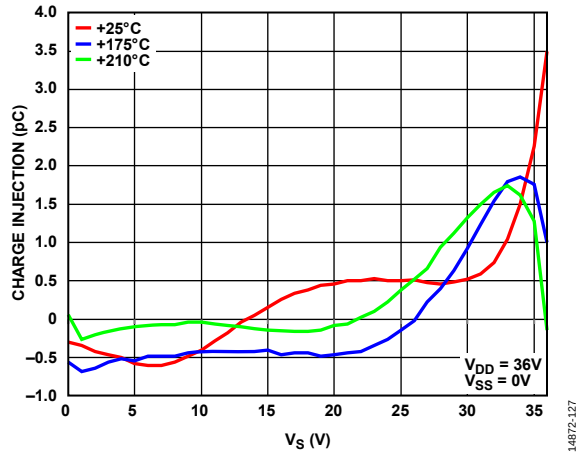

Figure 27. Charge Injection as a Function of V_S for Various Temperatures, 36 V Single Supply

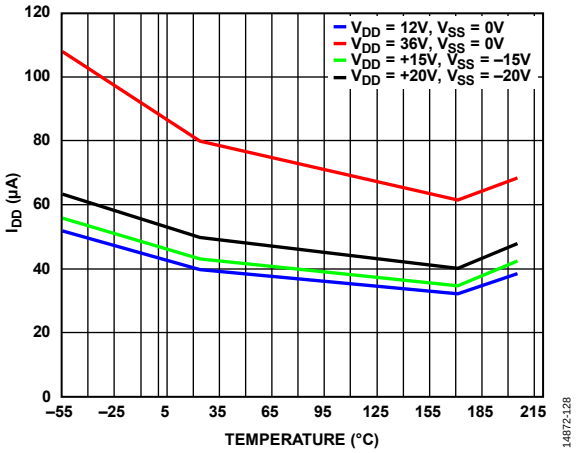

Figure 28. I_{DD} vs Temperature

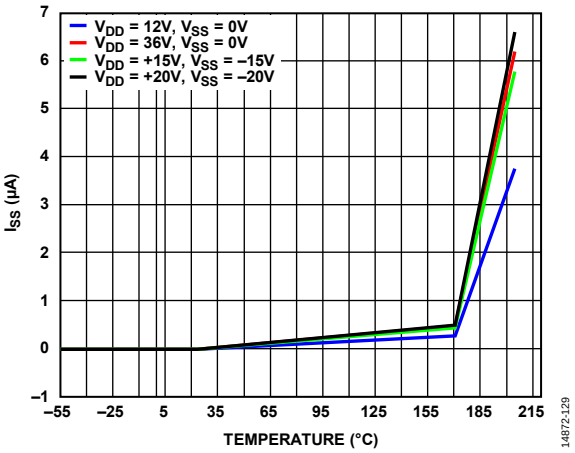

Figure 29. I_{SS} vs Temperature

TEST CIRCUITS

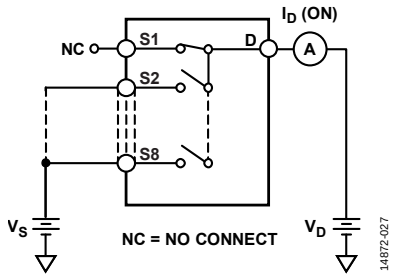

Figure 30. On Leakage

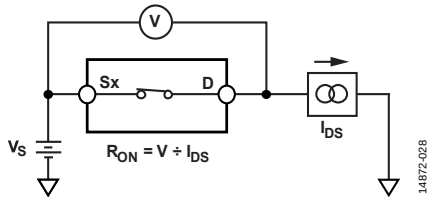

Figure 31. On Resistance

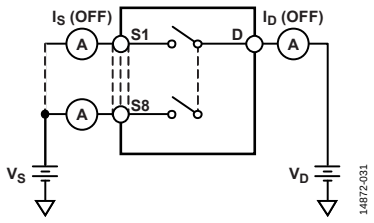

Figure 32. Off Leakage

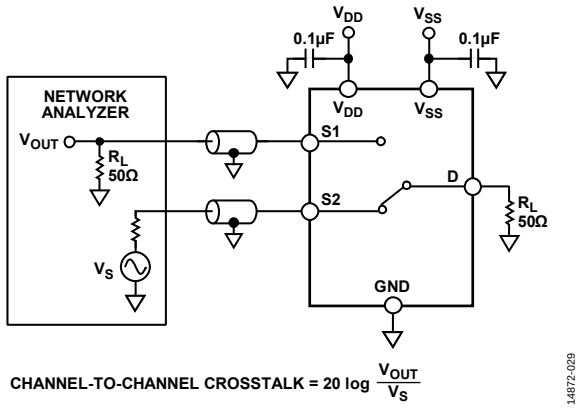

Figure 33. Channel-to-Channel Crosstalk

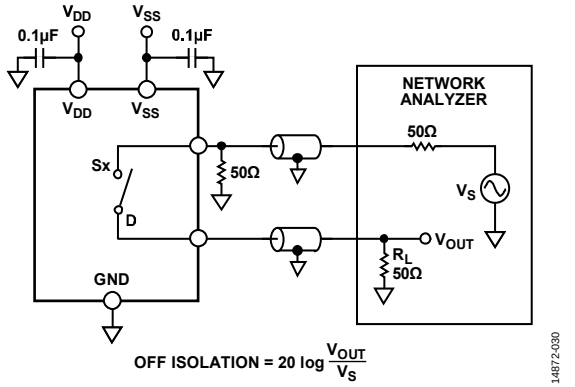

Figure 34. Off Isolation

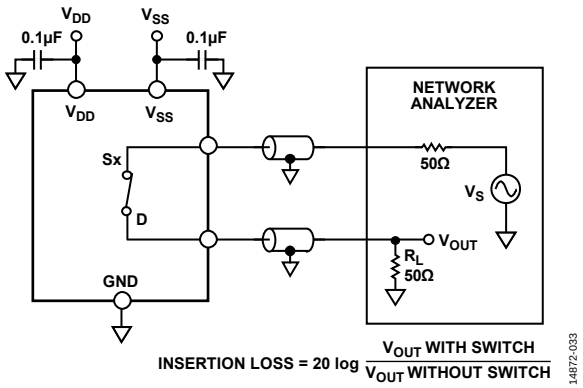

Figure 35. –3 dB Bandwidth

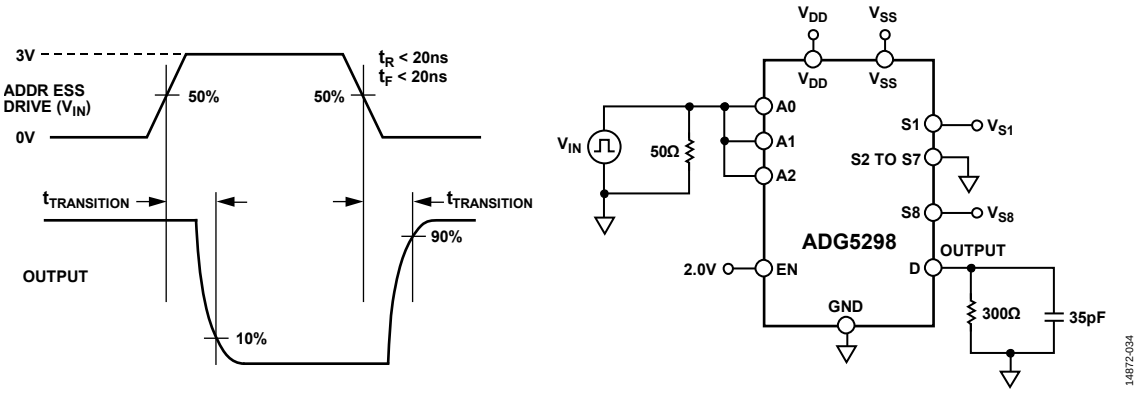

Figure 36. Address to Output Switching Times, $t_{TRANSITION}$

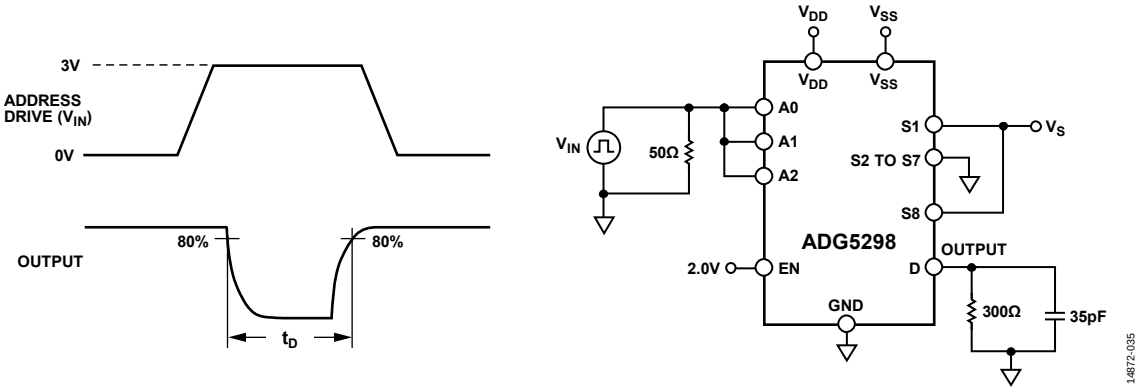

Figure 37. Break-Before-Make Time Delay, t_D

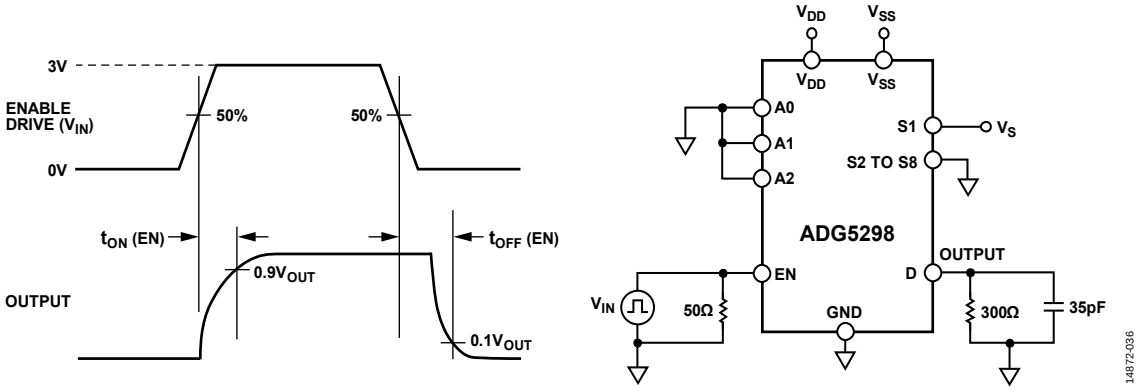

Figure 38. Enable Delay, t_{ON} (EN), t_{OFF} (EN)

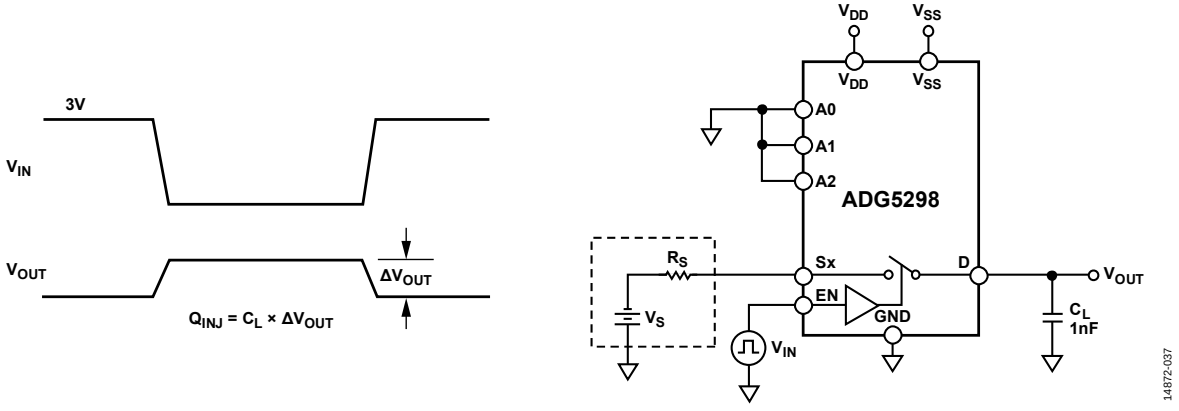

Figure 39. Charge Injection, Q_{INJ}

TERMINOLOGY

I_{DD}
I_{DD} represents the positive supply current.

I_{SS}
I_{SS} represents the negative supply current.

V_D, V_S
V_D and V_S represent the analog voltage on Terminal D and Terminal Sx, respectively.

R_{ON}
R_{ON} is the ohmic resistance between Terminal D and Terminal Sx.

ΔR_{ON}
ΔR_{ON} represents the difference between the R_{ON} of any two channels.

$R_{FLAT (ON)}$
Flatness that is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range is represented by $R_{FLAT (ON)}$.

I_S (Off)
I_S (off) is the source leakage current with the switch off.

I_D (Off)
I_D (off) is the drain leakage current with the switch off.

I_D (On), I_S (On)
I_D (on) and I_S (on) represent the channel leakage currents with the switch on.

V_{INL}
V_{INL} is the maximum input voltage for Logic 0.

V_{INH}
V_{INH} is the minimum input voltage for Logic 1.

I_{INL}, I_{INH}
I_{INL} and I_{INH} represent the low and high input currents of the digital inputs.

C_D (Off)
C_D (off) represents the off switch drain capacitance, which is measured with reference to ground.

C_S (Off)
C_S (off) represents the off switch source capacitance, which is measured with reference to ground.

C_D (On), C_S (On)
C_D (on) and C_S (on) represent on switch capacitances, which are measured with reference to ground.

C_{IN}
C_{IN} represents the digital input capacitance.

t_{ON} (EN)
t_{ON} (EN) represents the delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF} (EN)
t_{OFF} (EN) represents the delay time between the 50% and 90% points of the digital input and switch off condition.

$t_{TRANSITION}$
$t_{TRANSITION}$ represents the delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

Break-Before-Make Time Delay (t_D)
t_D represents the off time measured between the 80% point of both switches when switching from one address state to another.

Off Isolation
Off isolation is a measure of unwanted signal coupling through an off channel.

Charge Injection
Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

Crosstalk
Crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth
Bandwidth is the frequency at which the output is attenuated by −3 dB.

On Response
On response is the frequency response of the on switch.

AC Power Supply Rejection Ratio (ACPSRR)
ACPSRR is a measure of the ability of a device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of signal on the output to the amplitude of the modulation is the ACPSRR.

THEORY OF OPERATION

The ADG5298 is a latch-up proof, bidirectional, 8:1 CMOS multiplexer that is designed to operate at very high temperatures. The device is controlled by four parallel digital inputs (EN, A0, A1, and A2). The EN input allows for the ADG5298 to be enabled or disabled. When the ADG5298 is disabled, the source pins (S1 to S8) disconnect from the drain pin (D). When the ADG5298 is enabled, the address lines (A0, A1, and A2) can determine which source pin (S1 to S8) is connected to the drain pin (D).

TRENCH ISOLATION

In the ADG5298, an insulating oxide layer (trench) is placed between the negative channel metal-oxide semiconductor (NMOS) and the positive channel metal-oxide semiconductor (PMOS) transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in junction isolated switches, are eliminated, and the result is a completely latch-up proof switch that has minimal leakage over temperature.

In junction isolation, the N well and P well of the PMOS and NMOS transistors form a diode that is reverse biased under normal operation. However, during overvoltage conditions, this diode can become forward-biased. A silicon controlled rectifier (SCR) type circuit is formed by the two transistors, causing a significant amplification of the current that, in turn, leads to latch-up. With trench isolation, this diode is removed, and the result is a latch-up proof switch.

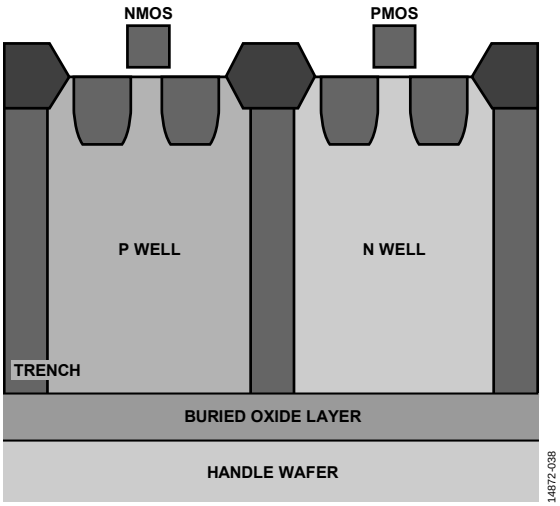

Figure 40. Trench Isolation

APPLICATIONS INFORMATION

The ultralow capacitance and charge injection of this switch makes it an ideal solution for data acquisition and sample-and-hold applications, where low glitch and fast settling are required.

The ADG5298 can operate in a wide ambient temperature range from −55°C to +210°C. Its wide range coupled with its latch-up immune and low leakage features makes the ADG5298 perfect for use in harsh environments, such as downhole drilling and avionics. The ADG5298 has achieved a JESD78D Class II rating, handling stresses to ±500 mA with a 10 ms pulse at the maximum operating temperature of the device (210°C).

OUTLINE DIMENSIONS

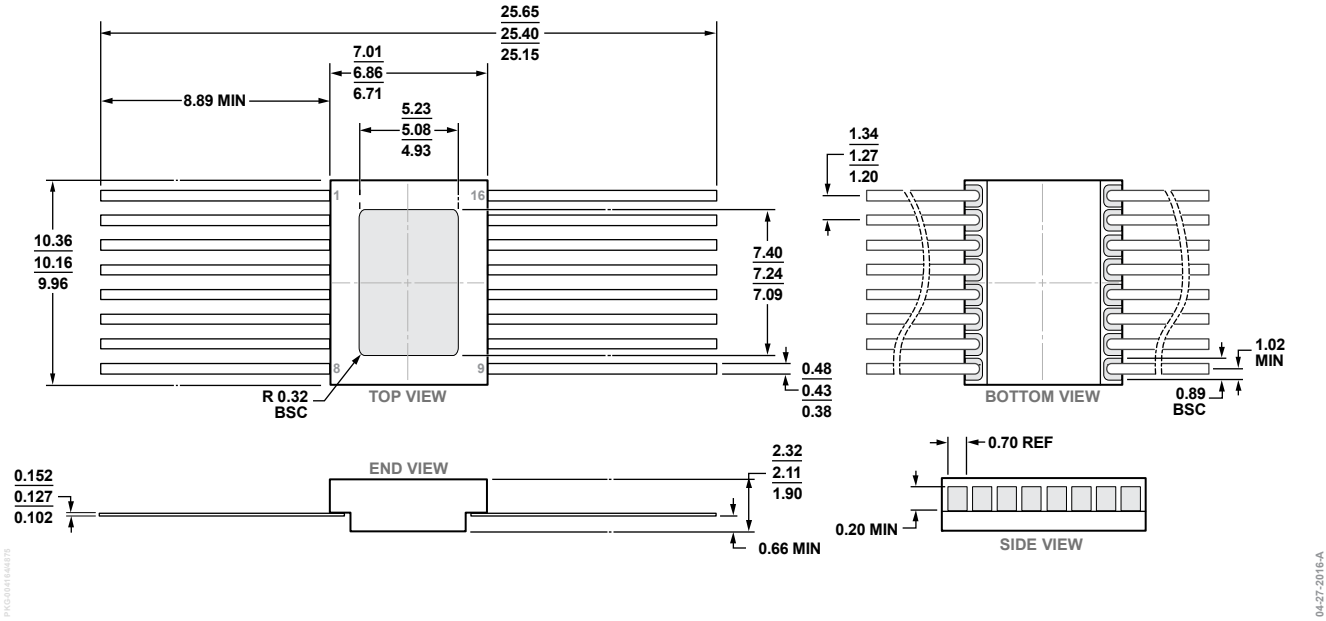

Figure 41. 16-Lead Ceramic Flat Package [FLATPACK]
(F-16-1)
Dimensions shown in millimeters

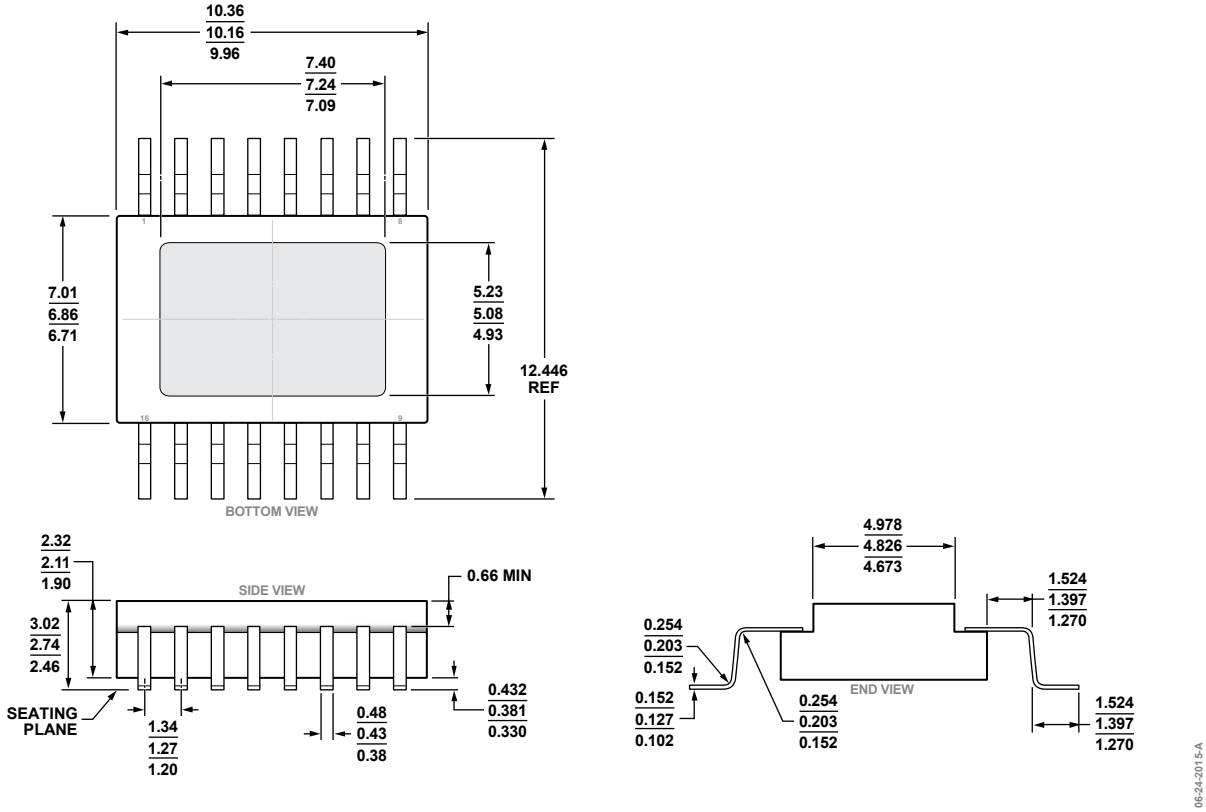

Figure 42. 16-Lead Ceramic Flat Package with Reverse Formed Gullwing Leads [FLATPACK_RF]
Cavity Down
(FR-16-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADG5298HFZ	−55°C to +210°C	16-Lead Ceramic Flat Package [FLATPACK]	F-16-1
ADG5298HFRZ	−55°C to +210°C	16-Lead Ceramic Flat Package with Reverse Formed Gullwing Leads [FLATPACK_RF]	FR-16-1
EVAL-ADG5298EB1Z		Evaluation Board	

[1] Z = RoHS Compliant Part.

D14872-0-9/16(0)