

To our customers,

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## Old Company Name in Catalogs and Other Documents

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On April 1<sup>st</sup>, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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Not recommended  
for new design

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# M62023L/P/FP

## System Reset IC with Switch for 3V Memory Back-up

REJ03D0528-0200

Rev.2.00

Jun 15, 2007

### General Description

The M62023L/P/FP is a system reset IC that controls the memory backup function of an SRAM and an embedded RAM of a microcontroller.

The IC outputs reset signals ( $\overline{\text{RES}}/\overline{\text{RES}}$ ) to a microcontroller at power-down and power failure. It also shifts the power supply to RAMs from main to backup, outputs a signal ( $\overline{\text{CS}}$ ) that invokes standby mode, and alters RAMs to backup circuit mode.

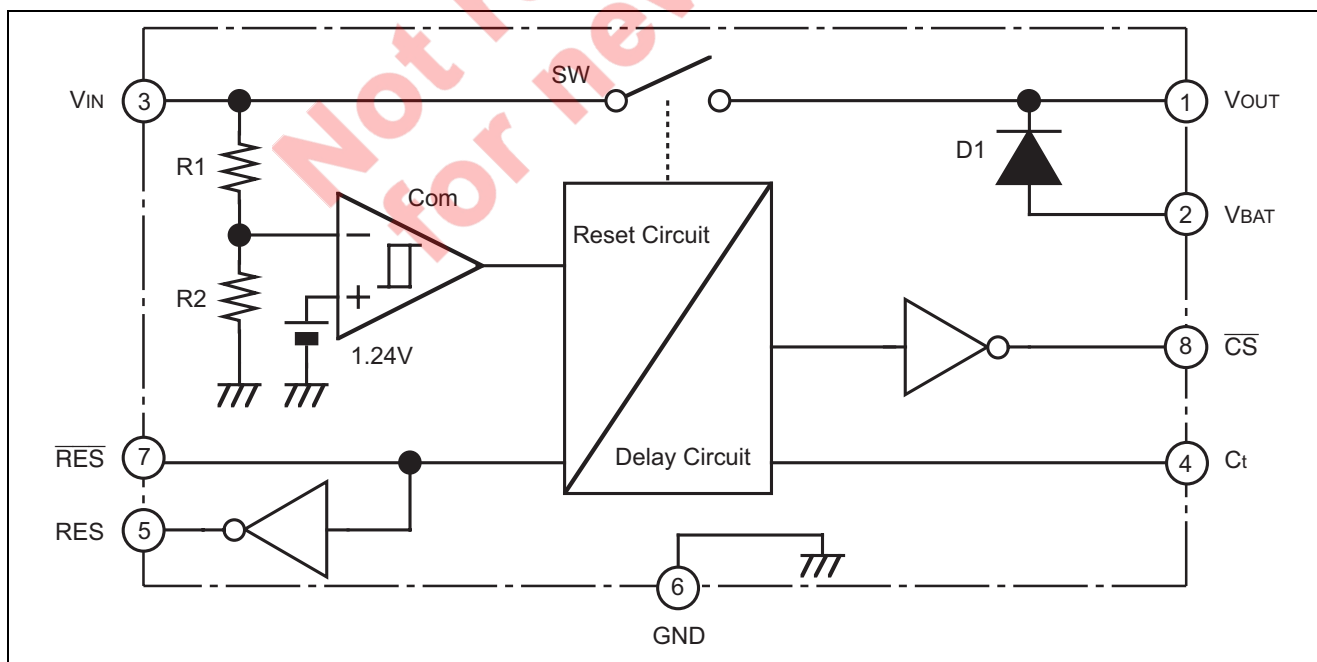
### Features

- Built-in switch for selection between main power supply and backup power supply to RAMs
- Small difference between input and output voltages ( $I_{\text{OUT}} = 80\text{mA}$ ,  $V_{\text{IN}} = 3\text{V}$ ):  $0.15\text{V}$  typ.
- Detection voltage (power supply monitor voltage):  $2.57\text{V}$  typ.
- Chip select signal output ( $\overline{\text{CS}}$ )
- Two channels of reset outputs ( $\overline{\text{RES}}/\overline{\text{RES}}$ )
- Power on reset circuit.

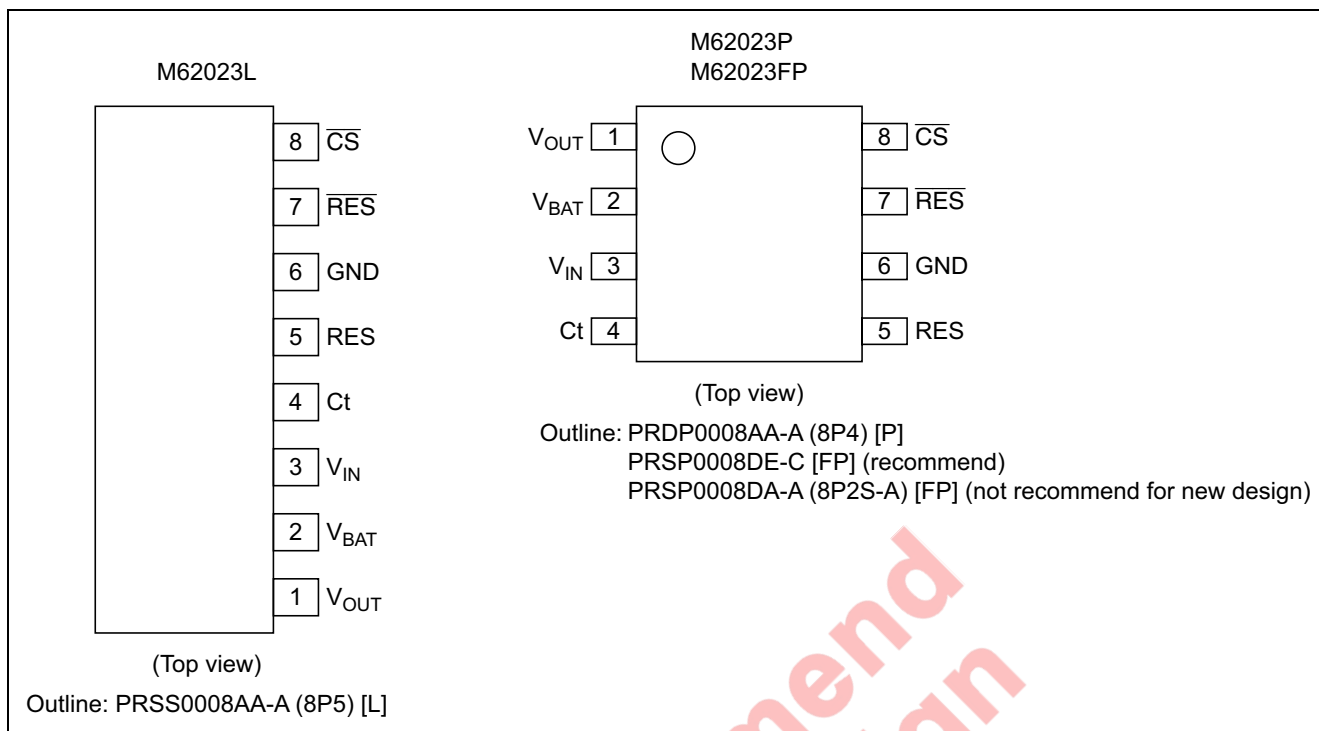
### Application

Power supply control systems for memory of microcontroller systems in electronic equipment such as OA equipment, industrial equipment, and home-use electronic appliances and SRAM boards with built-in backup function that require switching between external power supply and battery.

### Block Diagram



## Pin Arrangement



## Pin Description

Pin No.	Symbol	Name	Function
1	$\text{V}_{\text{OUT}}$	Power supply output	$\text{V}_{\text{IN}}$ and $\text{V}_{\text{BAT}}$ are controlled by means of an internal switch and output through $\text{V}_{\text{OUT}}$ . The pin is capable of outputting up to 100mA. Use it as $\text{V}_{\text{DD}}$ of CMOS RAM and the like.
2	$\text{V}_{\text{BAT}}$	Backup power supply input	Backup power supply is connected to this pin. If a lithium battery is used, insert a resistor in series for safety purposes.
3	$\text{V}_{\text{IN}}$	Power supply input	+3V input pin. Connect to a logic power supply.
4	$\text{Ct}$	Delay capacitor connection pin	A delay capacitor is connected to this pin. By connecting a capacitor, it is possible to delay each output.
5	RES	Positive reset output	Connect to the positive reset input of a microcontroller. The pin is capable of flowing 1mA sink current.
6	GND	Ground	Reference for all signals.
7	$\overline{\text{RES}}$	Negative reset output	Connect to the negative reset input of a microcontroller. The pin is capable of flowing 1mA sink current.
8	$\overline{\text{CS}}$	Chip select output	Connect to the $\overline{\text{Chip Select}}$ of RAM. The CS output is at low level in normal state thereby letting RAM be active. Under failure or backup condition, the CS output is set to high level, then RAM enters standby state disabling read/write function. The pin is capable of flowing a 1mA sink current.

## Absolute Maximum Ratings

(Ta = 25°C, unless otherwise noted.)

Item	Symbol	Ratings	Unit	Conditions
Input voltage	V <sub>IN</sub>	7	V	
Output current	I <sub>OUT</sub>	100	mA	
Power dissipation	P <sub>d</sub>	800 (L) / 625 (P) / 440 (FP)	mW	
Thermal derating	K <sub>θ</sub>	8 (L) / 6.25 (P) / 4.4 (FP)	mW/°C	Ta ≥ 25°C
Operating temperature	Topr	−20 to +75	°C	
Storage temperature	Tstg	−40 to +125	°C	

## Electrical Characteristics

(Ta = 25°C, unless otherwise noted.)

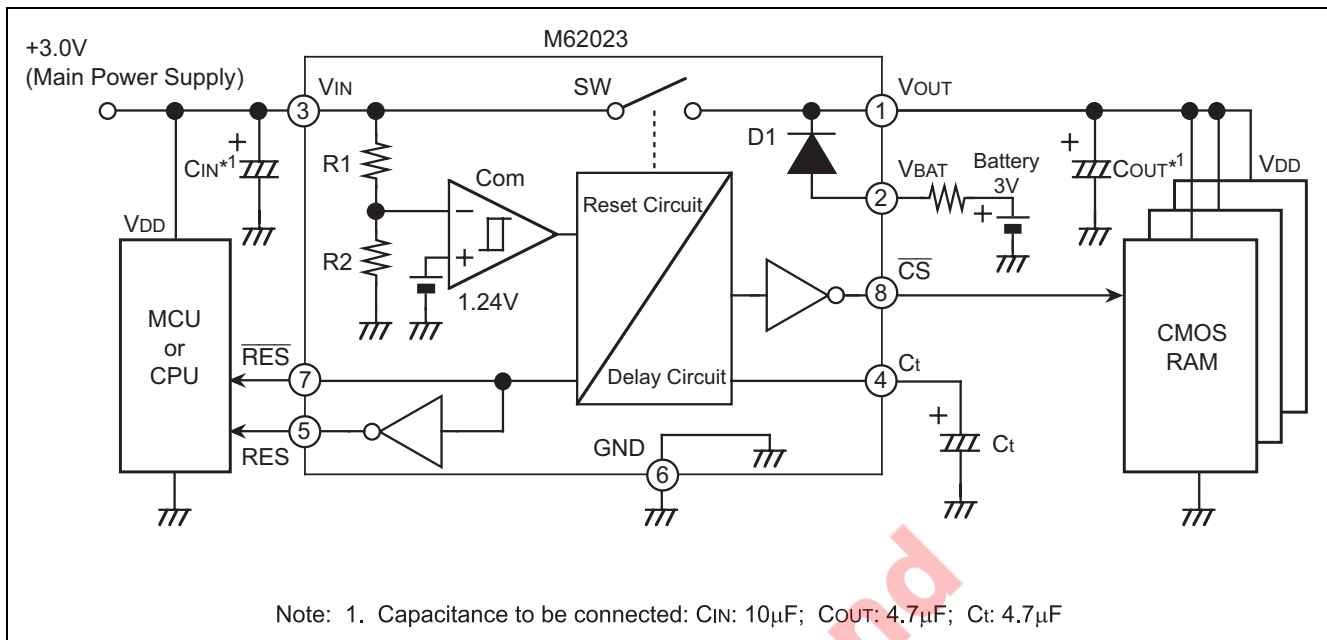
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Detection voltage	V <sub>S</sub>	2.44	2.57	2.70	V	V <sub>IN</sub> (At change from H→L)
Hysteresis voltage	ΔV <sub>S</sub>	50	100	200	mV	ΔV <sub>S</sub> = V <sub>SH</sub> − V <sub>SL</sub>
Circuit current	I <sub>CC</sub>	—	1.5	3.0	mA	I <sub>OUT</sub> = 0mA, V <sub>IN</sub> = 2V
		—	6.5	10		V <sub>IN</sub> = 3V
Difference between input and output voltage	V <sub>DROP</sub>	—	0.1	0.2	V	V <sub>IN</sub> = 3V, I <sub>OUT</sub> = 50mA
		—	0.15	0.3		I <sub>OUT</sub> = 80mA
Ct output voltage (high level)	V <sub>OH(Ct)</sub>	2.0	2.4	—	V	V <sub>IN</sub> = 3V *1
Ct output voltage (low level)	V <sub>OL(Ct)</sub>	—	0.02	0.1	V	V <sub>IN</sub> = 2V *1
RES output voltage (high level)	V <sub>OH(RES)</sub>	1.5	2.0	—	V	V <sub>IN</sub> = 2V *1
RES output voltage (low level)	V <sub>OL(RES)</sub>	—	0.02	—	V	V <sub>IN</sub> = 3V *1
		—	0.04	0.2		V <sub>IN</sub> = 3V, I <sub>sink</sub> = 1mA
RES output voltage (high level)	V <sub>OH(RES)</sub>	2.5	3.0	—	V	V <sub>IN</sub> = 3V *1
RES output voltage (low level)	V <sub>OL(RES)</sub>	—	0.02	—	V	V <sub>IN</sub> = 2V *1
		—	0.04	0.2		V <sub>IN</sub> = 2V, I <sub>sink</sub> = 1mA
CS output voltage (high level)	V <sub>OH(CS)</sub>	1.3	1.6	—	V	V <sub>IN</sub> = 2V *2
		2.40	2.47	—		V <sub>IN</sub> = 0V, V <sub>BAT</sub> = 3V *2
CS output voltage (low level)	V <sub>OL(CS)</sub>	—	0.07	—	V	V <sub>IN</sub> = 3V *1
		—	0.08	0.3		V <sub>IN</sub> = 3V, I <sub>sink</sub> = 1mA
Backup Di leak current	I <sub>R</sub>	—	—	±0.5	μA	V <sub>BAT</sub> = 3V, V <sub>IN</sub> = 3V
		—	—	±0.5		V <sub>IN</sub> = 0V
Backup Di forward direction voltage	V <sub>F</sub>	—	0.54	0.6	V	I <sub>F</sub> = 10μA
Delay time	tpd	10	27	55	ms	V <sub>IN</sub> = 0V→3V, Ct = 4.7μF
Response time	td	—	5.0	25.0	μs	V <sub>IN</sub> = 3V→2V
RES limit voltage of operation	V <sub>OPL(RES)</sub>	—	0.65	—	V	*3

Notes: 1. Regarding conditions to measure V<sub>OH</sub> and V<sub>OL</sub>, voltage values are generated by internal resistance only and no external resistor is used.

2. These values are produced inserting an external resistor, R<sub>C<sub>S</sub></sub> = 1MΩ, between the CS pin and GND.

3. With no external resistor (10kΩ internal resistance only).

## Application Example



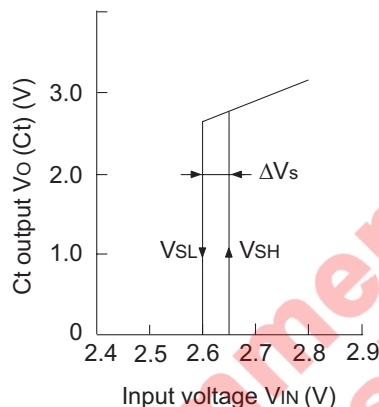
## Configuration

### <Power supply detector>

The internal reference voltage  $V_{ref}$  is compared by means of a comparator with resistor divided voltage  $V_R$  (resistor-divided voltage produced by  $R_1$  and  $R_2$  from  $V_{IN}$ ).

If the input voltage is 3V,  $V_R$  is set to 1.24V or higher, so the comparator output is at low level and the  $C_t$  output (Q1 collector output) is set to high level. If the input voltage drops to below 2.57V in an abnormal condition,  $V_R$  becomes below 1.24V, so the comparator output goes from low to high level and the  $C_t$  output, from high to low. The input voltage at this point is called  $V_{SL}$ . Next, when the input voltage, restored from abnormal state, has a rise, the comparator output goes from high to low level and the  $C_t$  output, from low to high.

The comparator used for detection has 100mV hysteresis ( $\Delta V_s$ ), so that malfunctioning is prevented in case that the input voltage slowly drops or  $V_R$  nearly equals  $V_{ref}$ .



### <Delay Circuit>

Connecting an external capacitor to the  $C_t$  pin lets  $\overline{RES}$ ,  $\overline{RES}$ ,  $\overline{CS}$ , and  $V_{OUT}$  be delayed due to RC transient phenomenon (electric charge).

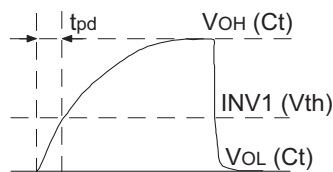
Delay time is determined as follows.

$$\begin{aligned} \text{Delay time (tpd)} &= C_t \times R_3 \times \ln \frac{[V_{OH}(C_t) - V_{OL}(C_t)]}{[V_{OH}(C_t) - INV1(V_{TH})]} \\ &= C_t \times 22k\Omega \times 0.2389 \\ &\cong 5.26 \times 10^{-3} \times C_t \end{aligned}$$

Note:  $C_t$  is an external capacitance.

Taking into consideration the time taken by the oscillator of microcomputer to be stable, connect a 4.7 $\mu$ F capacitor to the  $C_t$  pin.

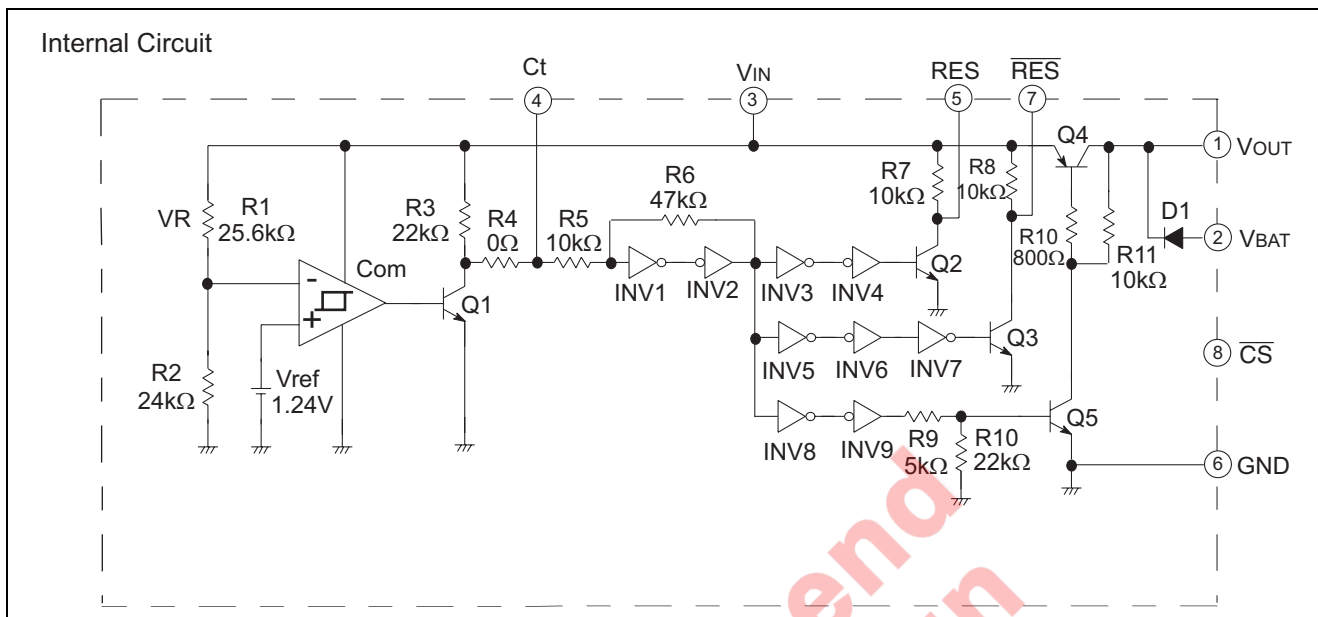
(As the response time of detection can be slowed due to internal structure depending on the rising rate of power supply, avoid connecting a too large capacitance.)



Delayed output waveforms of  $C_t$

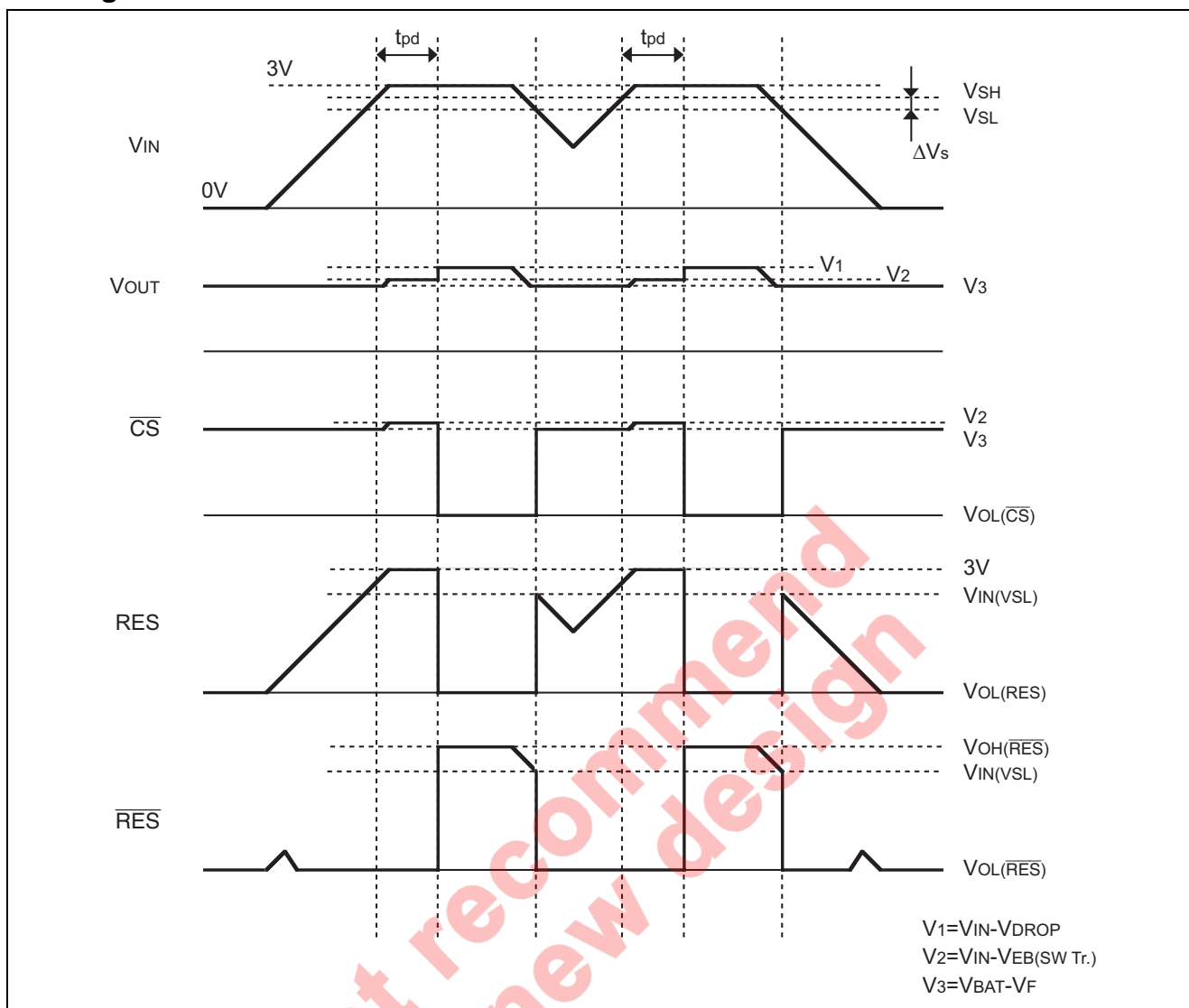
## &lt;Schmitt trigger circuit&gt;

Since waveforms show a gentle rise due to the RC delay circuit, INV1, INV2, and R6 constitute a Schmitt trigger circuit to produce hysteresis so as to prevent each output from chattering.



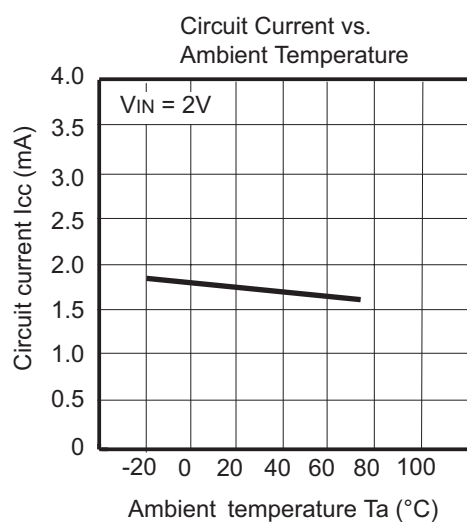
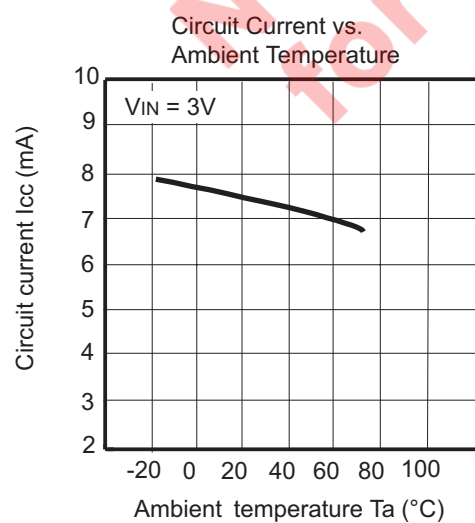
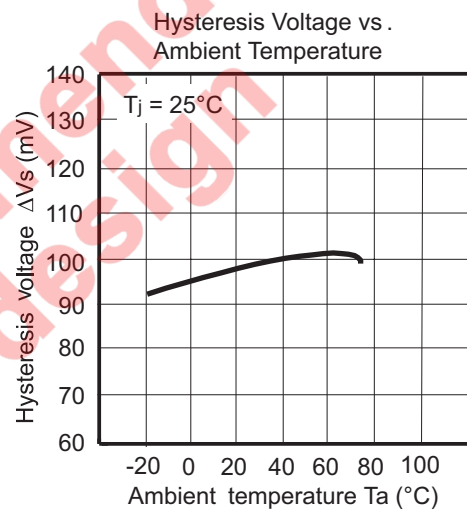
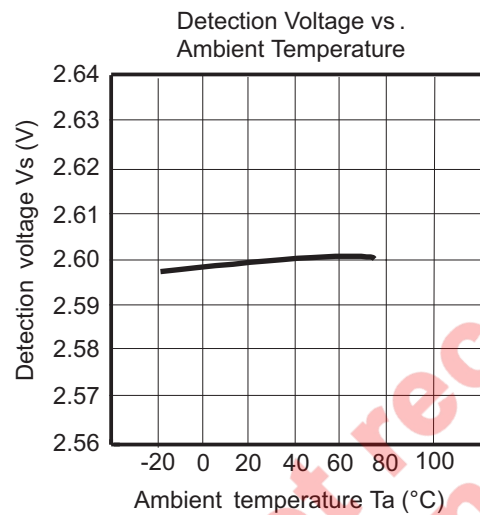
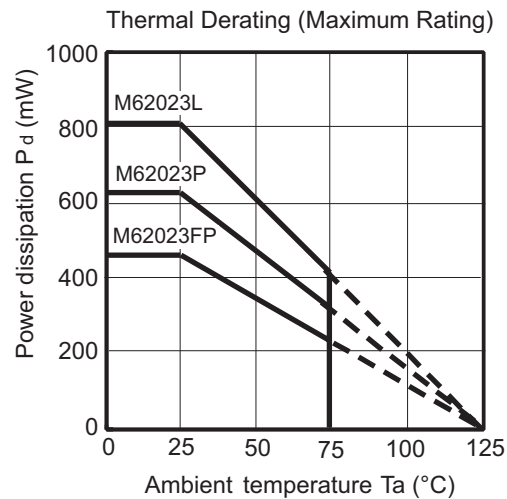


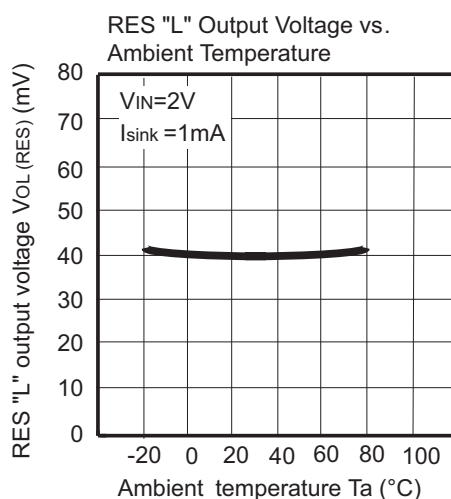
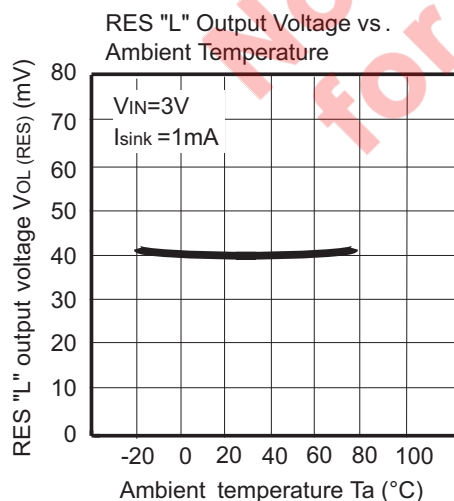
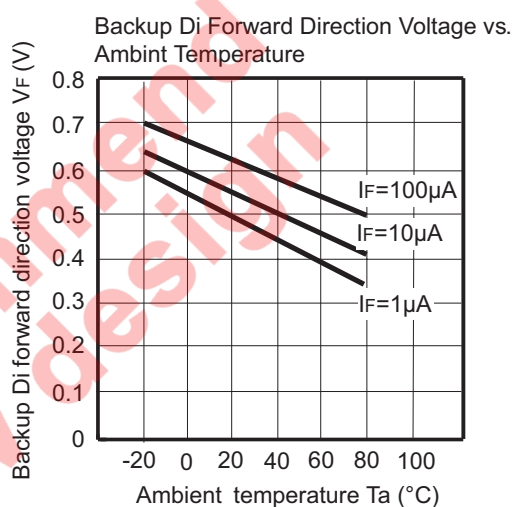
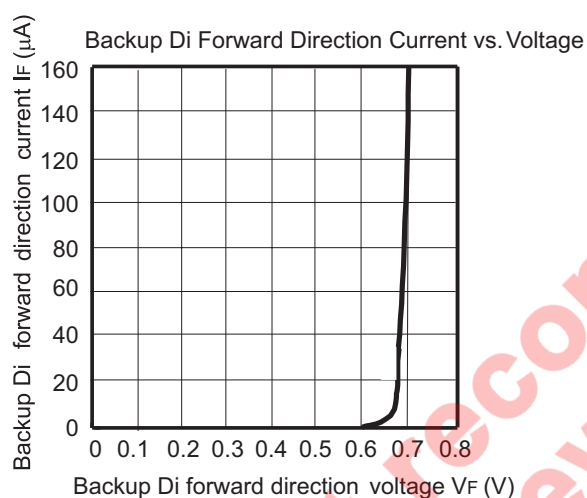
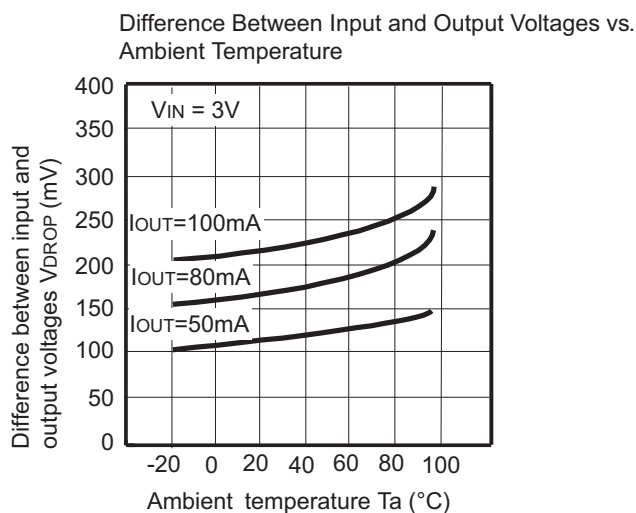
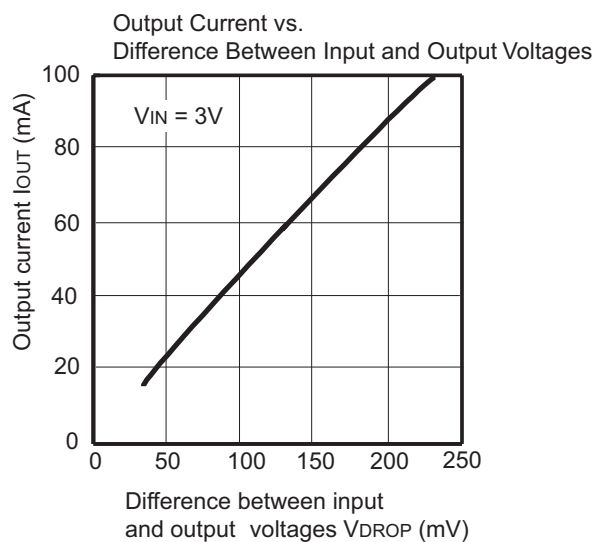
## Timing Chart

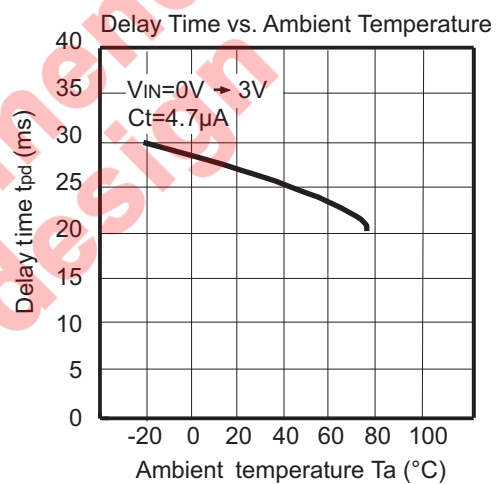
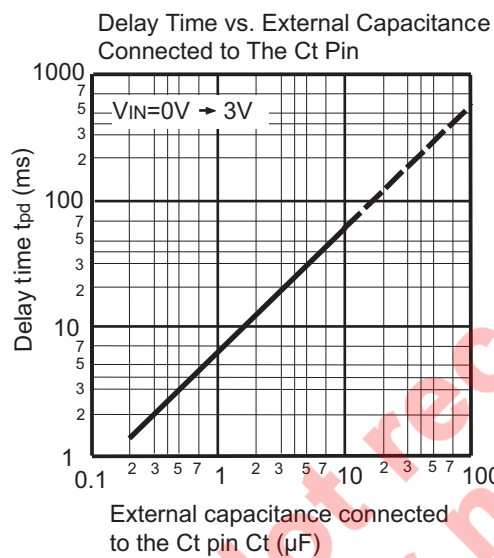
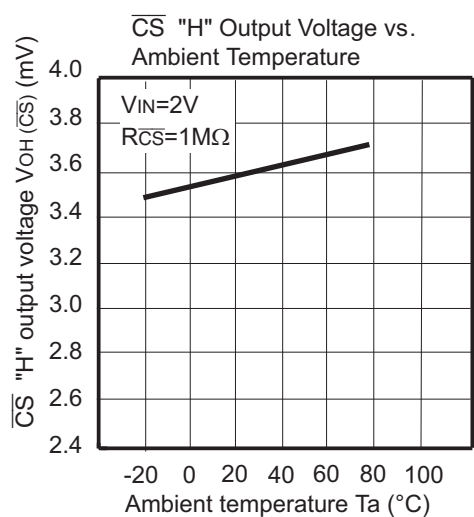
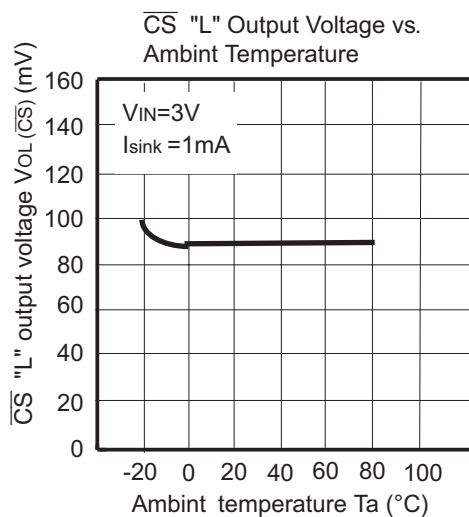


Output pin	Input voltage			
	In normal operation	In failure (instantaneous drop)	Restoration from failure (instantaneous drop)	In backup state
	Input voltage: 3V	Input voltage: 3V→2V Each output varies if the input voltage drops to $V_{SL}$ or under	Input voltage: 2V→3V If the input voltage goes higher than $V_{SL}$ by 100mV, each output varies after delay produced by the delay circuit.	Input voltage: 0V Backup voltage: 3V
V <sub>OUT</sub>	With SW Tr. set to ON, a voltage ( $V_{IN} - V_{DROP}$ ) is output.	SW Tr. is turned OFF. A voltage ( $V_{IN} - V_{EB}$ ) is output by the diode between E and B of SW Tr.	SW Tr. is turned ON after delay and a voltage ( $V_{IN} - V_{DROP}$ ) is output.	$V_{BAT} - V_F$
RES	The output level is $V_{OL(RES)}$ with a logic low.	As the state shifts from a logic low to logic high, the output level becomes approximately equal to the input voltage.	A logic high is maintained, and then shifts to a logic low.	_____
RES	The output level is $V_{OH(RES)}$ with a logic high.	As the state shifts from a logic high to logic low, the output level becomes $V_{OL(RES)}$	A logic low is maintained, and then shifts to a logic high.	_____
CS	The output level is $V_{OL(CS)}$ with a logic low.	As the state shifts from a logic low to logic high, the output level becomes the voltage $V_{IN} - V_{EB}$ .	A logic high is maintained, and then shifts to a logic low.	The output is a logic high and the output level is $V_{BAT} - V_F$

## Typical Characteristics

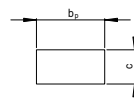
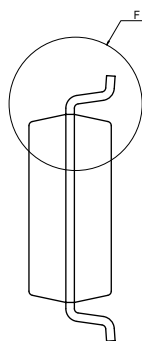
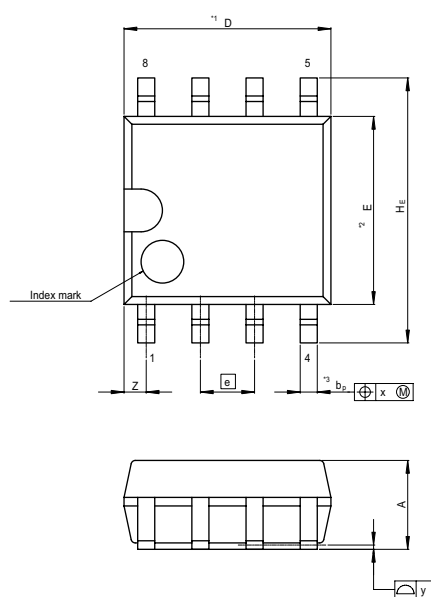




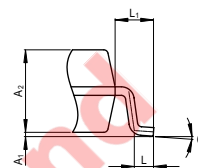




JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP8-4.4x4.85-1.27	PRSP0008DE-C	—	0.1g



Terminal cross section  
( Ni/Pd/Au plating )

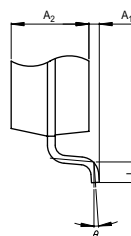
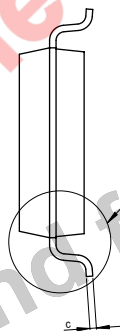
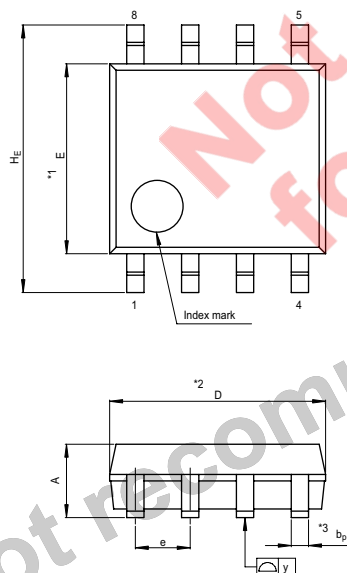


Detail F

NOTE)  
1. DIMENSIONS \*\*1 (Nom)\*\* AND \*\*2\*  
DO NOT INCLUDE MOLD FLASH.  
2. DIMENSION \*\*3\* DOES NOT  
INCLUDE TRIM OFFSET.

Reference Symbol	Min	Nom	Max
D	4.65	4.85	5.05
E	4.2	4.4	4.6
A <sub>2</sub>	—	1.85	—
A <sub>1</sub>	0.00	0.1	0.20
A	—	—	2.03
b <sub>p</sub>	0.34	0.4	0.46
b <sub>1</sub>	—	—	—
c	0.15	0.20	0.25
c <sub>1</sub>	—	—	—
θ	0°	—	8°
H <sub>E</sub>	5.7	6.2	6.5
e	1.12	1.27	1.42
x	—	—	0.12
y	—	—	0.10
z	—	—	0.75
L	0.25	0.45	0.65
L <sub>1</sub>	—	0.90	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP8-4.4x5-1.27	PRSP0008DA-A	8P2S-A	0.07g



Detail F

NOTE)  
1. DIMENSIONS \*\*1\* AND \*\*2\*  
DO NOT INCLUDE MOLD FLASH.  
2. DIMENSION \*\*3\* DOES NOT  
INCLUDE TRIM OFFSET.

Reference Symbol	Min	Nom	Max
D	4.8	5.0	5.2
E	4.2	4.4	4.6
A <sub>2</sub>	—	1.5	—
A <sub>1</sub>	0.05	—	—
A	—	—	1.9
b <sub>p</sub>	0.35	0.4	0.5
c	0.13	0.15	0.2
θ	0°	—	10°
H <sub>E</sub>	5.9	6.2	6.5
e	1.12	1.27	1.42
y	—	—	0.1
L	0.2	0.4	0.6

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