

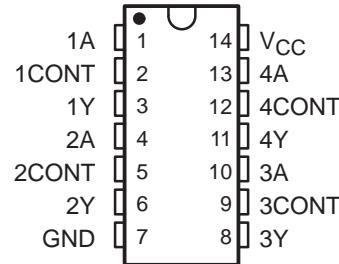
- **Input Resistance . . . 3 k Ω to 7 k Ω**
- **Input Signal Range . . . ± 30 V**
- **Operate From Single 5-V Supply**
- **Built-In Input Hysteresis (Double Thresholds)**
- **Response Control that Provides:**
 - Input Threshold Shifting**
 - Input Noise Filtering**
- **Meet or Exceed the Requirements of TIA/EIA-232-F and ITU Recommendation V.28**
- **Fully Interchangeable With MotorolaTM MC1489 and MC1489A**

description

These devices are monolithic low-power Schottky quadruple line receivers designed to satisfy the requirements of the standard interface between data-terminal equipment and data-communication equipment as defined by TIA/EIA-232-F. A separate response-control (CONT) terminal is provided for each receiver. A resistor or a resistor and bias-voltage source can be connected between this terminal and ground to shift the input threshold levels. An external capacitor can be connected between this terminal and ground to provide input noise filtering.

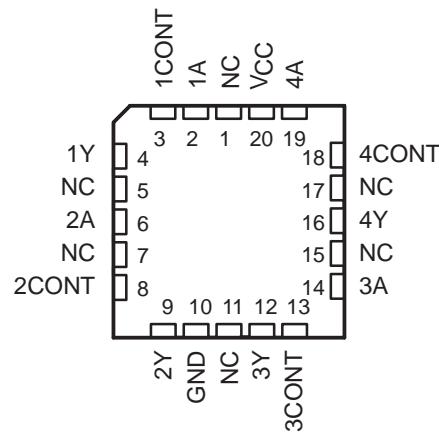
The SN55189 and SN55189A are characterized for operation over the full military temperature range of -55°C to 125°C . The MC1489, MC1489A, SN75189, and SN75189A are characterized for operation from 0°C to 70°C .

SN55189, SN55189A . . . J OR W PACKAGE
MC1489, MC1489A, SN75189, SN75189A
D, N, OR NS[†] PACKAGE
(TOP VIEW)



[†] The NS package is only available left-end taped and reeled. For SN75189, order SN75189NSR.

SN55189, SN55189A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



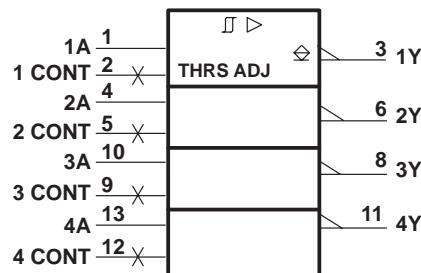
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

MC1489, MC1489A, SN55189, SN55189A, SN75189, SN75189A QUADRUPLE LINE RECEIVERS

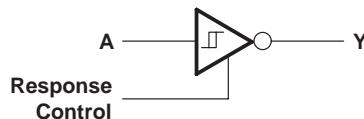
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logic symbol†

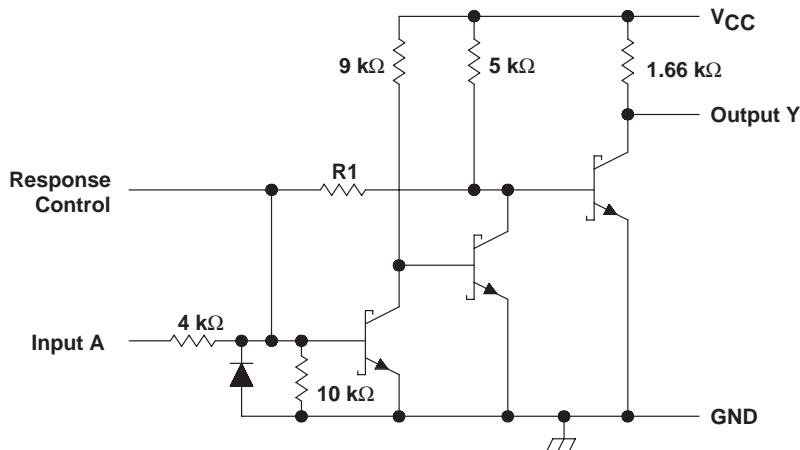


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, NS, and W packages.

logic diagram (positive logic)



schematic (each receiver)



	MC1489 SN55189 SN75189	MC1489A SN55189A SN75189A
R1	8.4 kΩ	1.84 kΩ

Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	10 V
Input voltage, V_I	± 30 V
Output voltage, I_O	20 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : SN55189, SN55189A	-55°C to 125°C
MC1489, MC1489A, SN75189, SN75189A	0°C to 70°C
Storage temperature range, T_{STG}	-65°C to 150°C
Case temperature for 60 seconds, FK package	260°C
Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds: J or W package	300°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds: D, N, or NS package	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ C$	$T_A = 70^\circ C$ POWER RATING	$T_A = 125^\circ C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J‡	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	N/A
NS	625 mW	4.0 mW/°C	445 mW	N/A
W	1000 mW	8.0 mW/°C	640 mW	200 mW

‡ In the J package, SN55189 and SN55189A chips are either silver glass or alloy mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Input voltage, V_I	-25		25	V
High-level output current, I_{OH}			-0.5	mA
Low-level output current, I_{OL}			10	mA
Operating free-air temperature, T_A	0		70	°C

MC1489, MC1489A, SN55189, SN55189A, SN75189, SN75189A QUADRUPLE LINE RECEIVERS

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electrical characteristics over operating free-air temperature range, $V_{CC} = 5 \text{ V} \pm 1\%$ (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS [†]	SN55189 SN55189A			MC1489, MC1489A SN75189 SN75189A			UNIT	
			MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX		
V _{IT+} Positive-going input threshold voltage	1	'89	$T_A = 25^\circ\text{C}$	1	1.3	1.5	1	1.3	1.5	V
			$T_A = 0^\circ\text{C}$ to 70°C				0.9		1.6	
			$T_A = -55^\circ\text{C}$ to 125°C	0.6		1.9				
		'89A	$T_A = 25^\circ\text{C}$	1.75	1.9	2.25	1.75	1.9	2.25	
			$T_A = 0^\circ\text{C}$ to 70°C				1.55		2.25	
			$T_A = -55^\circ\text{C}$ to 125°C	1.30		2.65				
V _{IT-} Negative-going input threshold voltage	1	'89, '89A	$T_A = 25^\circ\text{C}$	0.75	1.0	1.25	0.75	1.0	1.25	V
			$T_A = 0^\circ\text{C}$ to 70°C				0.65		1.25	
			$T_A = -55^\circ\text{C}$ to 125°C	0.35		1.6				
V _{OH} High-level output voltage	1	$V_I = 0.75 \text{ V}$, $I_{OH} = -0.5 \text{ mA}$			2.6	4	5	2.6	4	V
		Input open, $I_{OH} = -0.5 \text{ mA}$			2.6	4	5	2.6	4	
V _{OL} Low-level output voltage	1	$V_I = 3 \text{ V}$, $I_{OL} = 10 \text{ mA}$			0.2	0.45		0.2	0.45	V
I _{IH} High-level input current	2	$V_I = 25 \text{ V}$			3.6	8.3	3.6	8.3		mA
		$V_I = 3 \text{ V}$			0.43		0.43			
I _{IL} Low-level input current	2	$V_I = -25 \text{ V}$			-3.6	-8.3	-3.6	-8.3		mA
		$V_I = -3 \text{ V}$			-0.43		-0.43			
I _{OS} Short-circuit output current	3				-3			-3		mA
I _{CC} Supply current	2	$V_I = 5 \text{ V}$, Outputs open			20	26		20	26	mA

[†] All characteristics are measured with the response-control terminal open.

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}$, $C_L = 15 \text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH} Propagation delay time, low- to high-level output	4	$R_L = 3.9 \text{ k}\Omega$		25	85	ns
t _{PHL} Propagation delay time, high- to low-level output		$R_L = 390 \Omega$		25	50	
t _{T LH} Transition time, low- to high-level output		$R_L = 3.9 \text{ k}\Omega$		120	175	ns
t _{THL} Transition time, high- to low-level output		$R_L = 390 \Omega$		10	20	

PARAMETER MEASUREMENT INFORMATION[†]

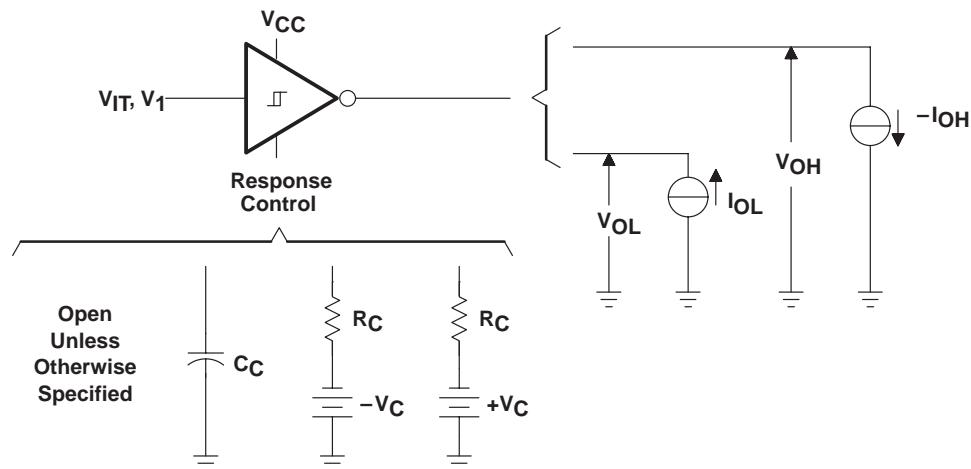
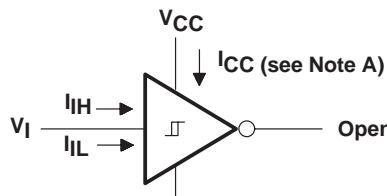


Figure 1. V_{IT+} , V_{IT-} , V_{OH} , V_{OL}



NOTE A: I_{CC} is tested for all four receivers simultaneously.

Figure 2. I_{IH} , I_{IL} , I_{CC}

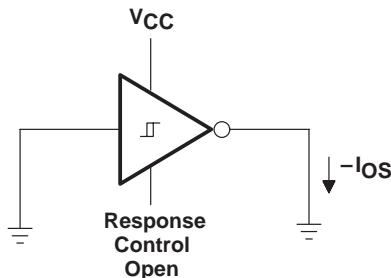


Figure 3. I_{OS}

[†] Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

MC1489, MC1489A, SN55189, SN55189A, SN75189, SN75189A QUADRUPLE LINE RECEIVERS

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PARAMETER MEASUREMENT INFORMATION

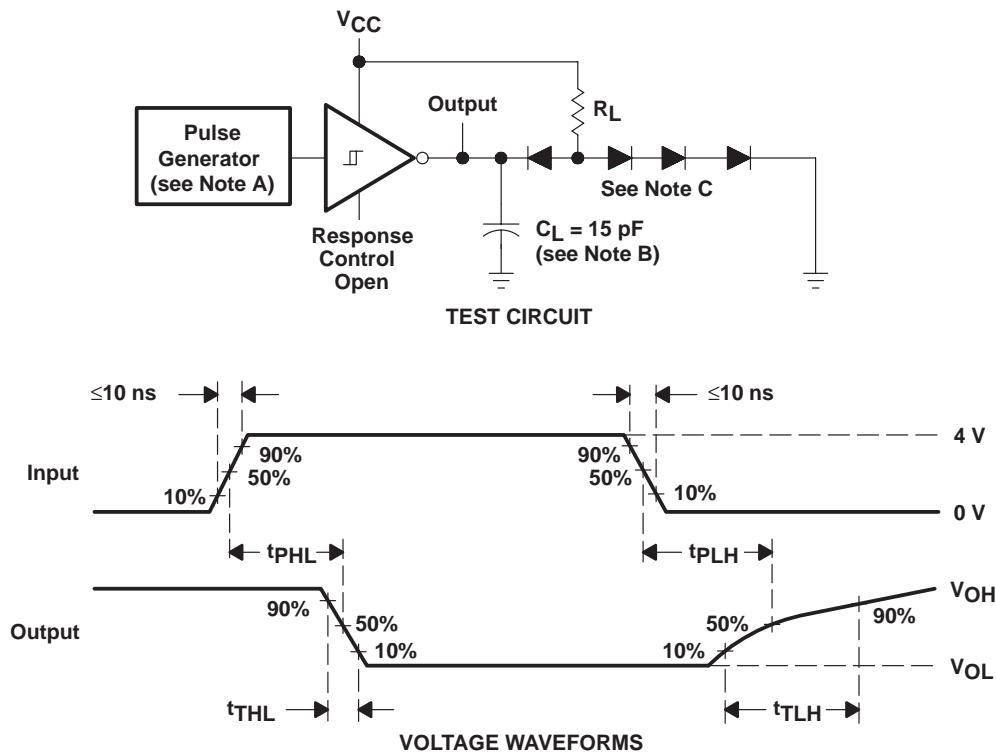


Figure 4. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

SN65189, SN75189
OUTPUT VOLTAGE
vs
INPUT VOLTAGE

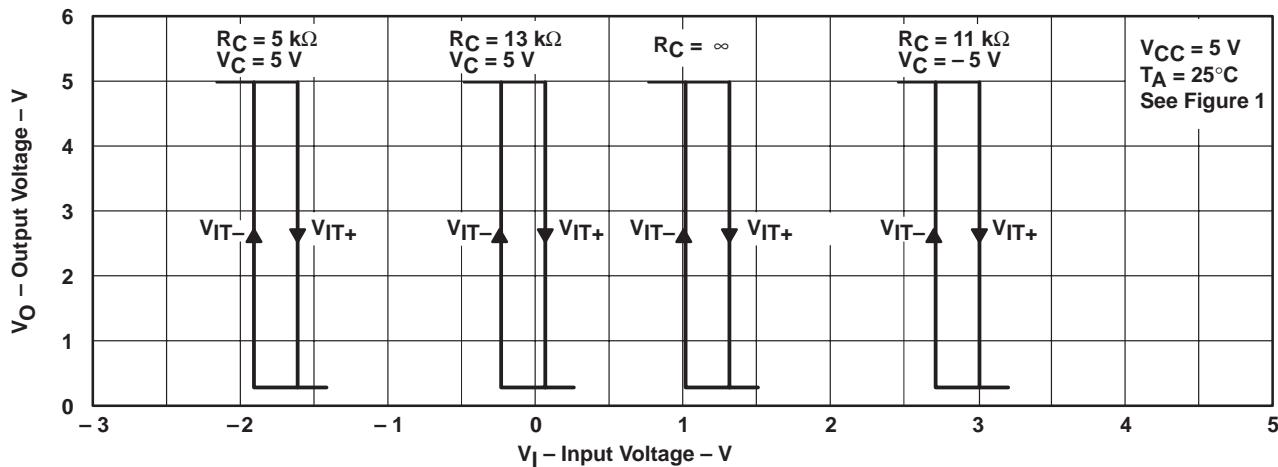


Figure 5

SN65189A, SN75189A
OUTPUT VOLTAGE
vs
INPUT VOLTAGE

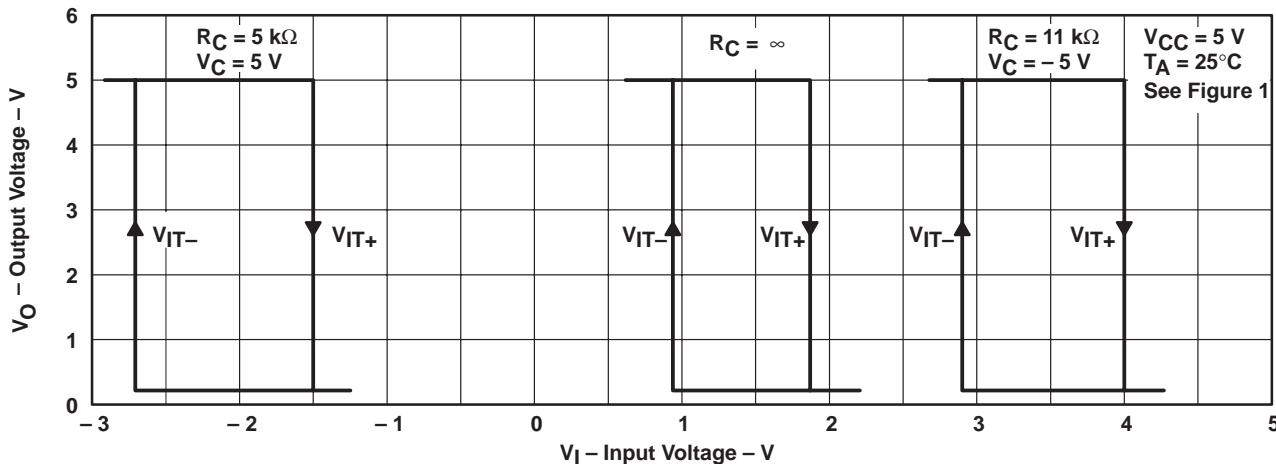
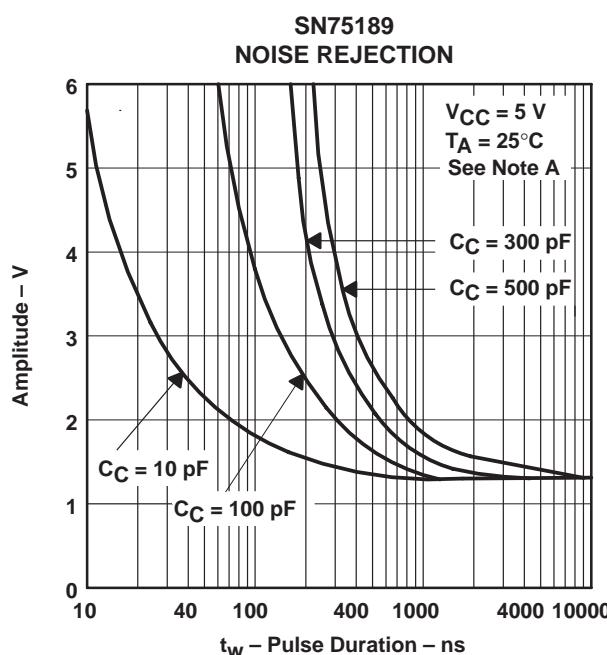
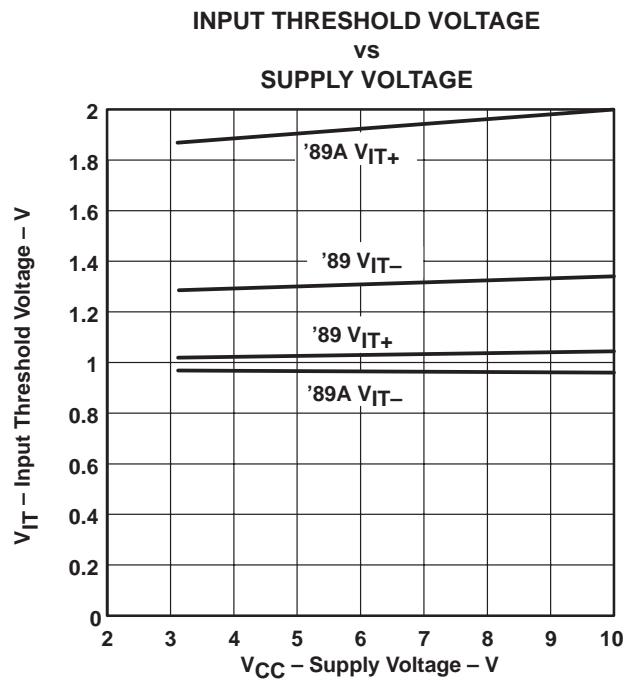
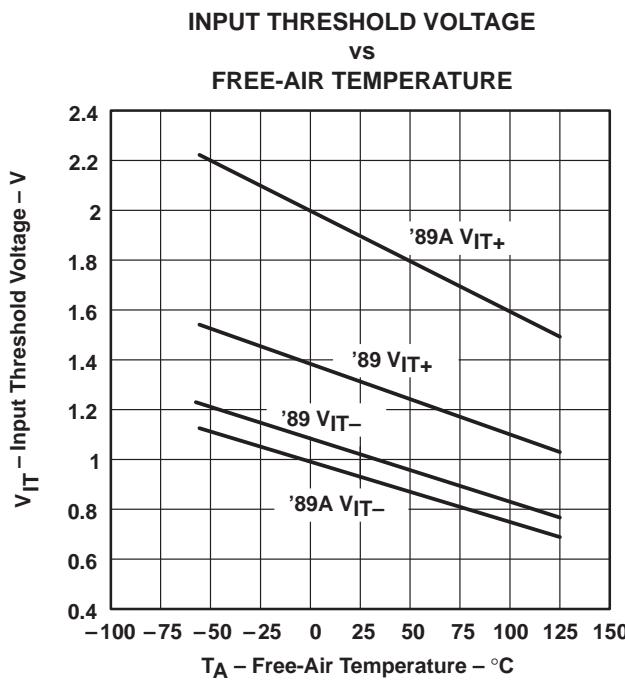


Figure 6

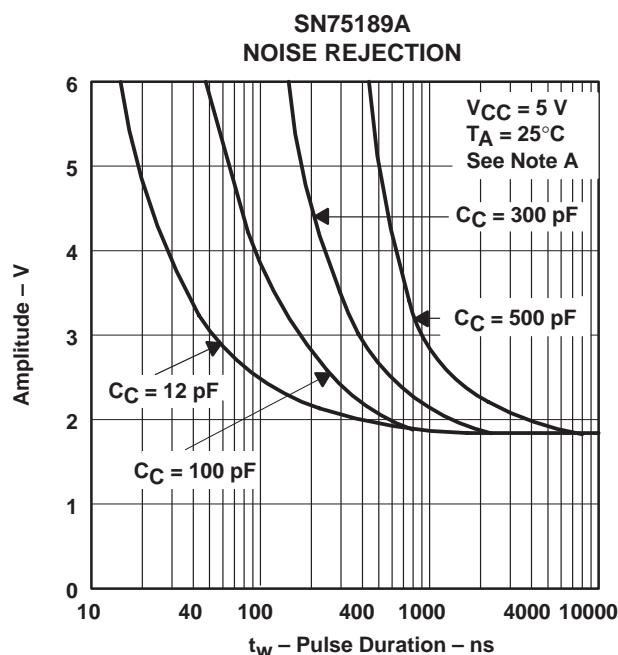
MC1489, MC1489A, SN55189, SN55189A, SN75189, SN75189A QUADRUPLE LINE RECEIVERS

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TYPICAL CHARACTERISTICS[†]



NOTE A: Maximum amplitude of a positive-going pulse that, starting from 0 V, will not cause a change in the output level.



NOTE A: Maximum amplitude of a positive-going pulse that, starting from 0 V, will not cause a change in the output level.

[†] Data for free-air temperatures below 0°C and above 70°C are applicable to SN55189 and SN55189A circuits only.

TYPICAL CHARACTERISTICS

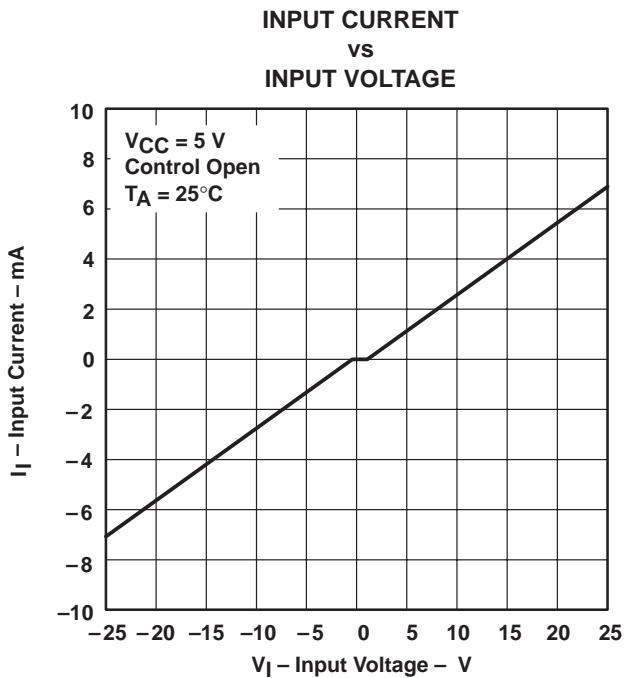


Figure 11

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-86888022A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-86888022A SNJ55189AFK	Samples
5962-8688802CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8688802CA SNJ55189AJ	Samples
5962-8688802DA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8688802DA SNJ55189AW	Samples
MC1489AN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	MC1489AN	Samples
MC1489ANE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	MC1489AN	Samples
MC1489N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	MC1489N	Samples
MC1489NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	MC1489N	Samples
SN55189AJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN55189AJ	Samples
SN55189J	OBsolete	CDIP	J	14		TBD	Call TI	Call TI	-55 to 125		
SN75189AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75189A	Samples
SN75189ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75189A	Samples
SN75189ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75189A	Samples
SN75189ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75189A	Samples
SN75189AN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75189AN	Samples
SN75189ANE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75189AN	Samples
SN75189ANSLE	OBsolete	SO	NS	14		TBD	Call TI	Call TI	0 to 70		
SN75189ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75189A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75189ANSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75189A	Samples
SN75189D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75189	Samples
SN75189DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75189	Samples
SN75189DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75189	Samples
SN75189N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75189N	Samples
SN75189NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75189N	Samples
SN75189NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75189	Samples
SNJ55189AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-86888022A SNJ55189AFK	Samples
SNJ55189AJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8688802CA SNJ55189AJ	Samples
SNJ55189AW	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8688802DA SNJ55189AW	Samples
SNJ55189FK	OBsolete	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
SNJ55189J	OBsolete	CDIP	J	14		TBD	Call TI	Call TI	-55 to 125		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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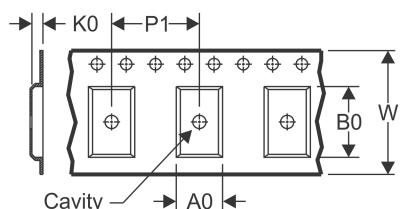
OTHER QUALIFIED VERSIONS OF SN55189, SN55189A, SN75189, SN75189A :

- Catalog: [SN75189](#), [SN75189A](#)
- Military: [SN55189](#), [SN55189A](#)

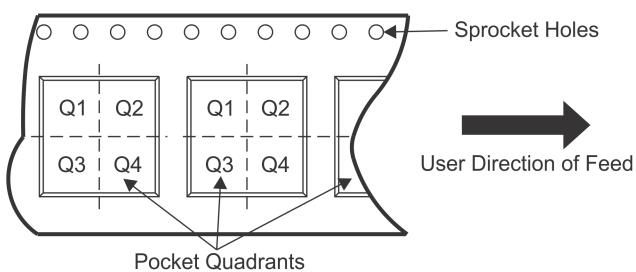
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

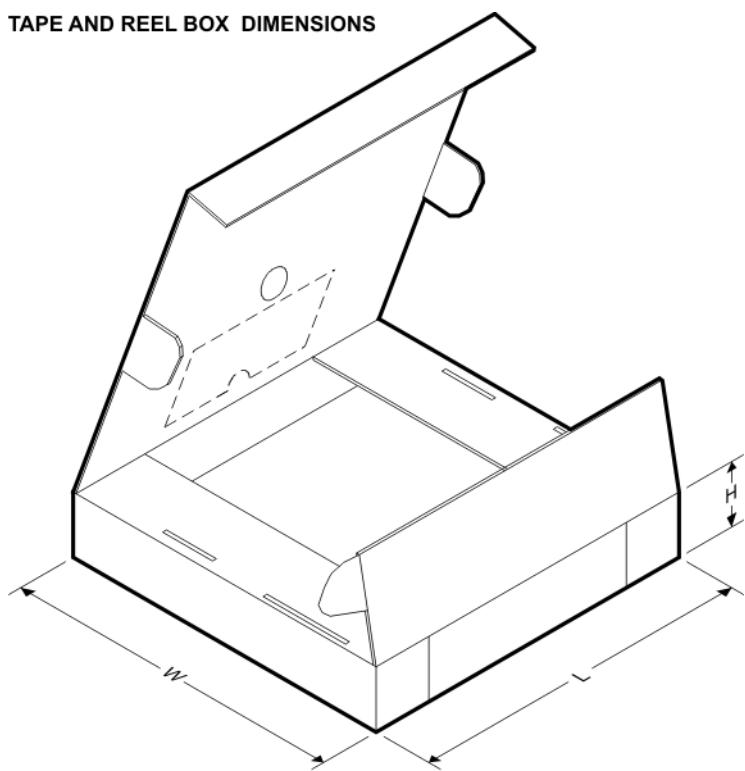
TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75189ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN75189ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN75189DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN75189NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


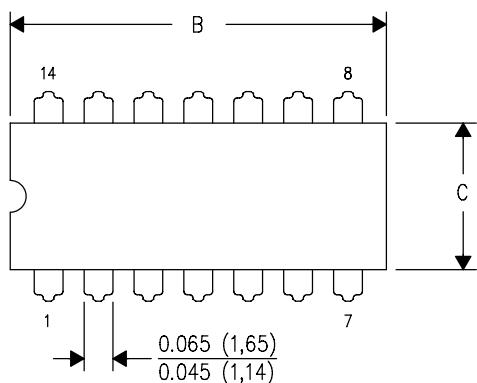
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75189ADR	SOIC	D	14	2500	333.2	345.9	28.6
SN75189ADR	SOIC	D	14	2500	367.0	367.0	38.0
SN75189DR	SOIC	D	14	2500	367.0	367.0	38.0
SN75189NSR	SO	NS	14	2000	367.0	367.0	38.0

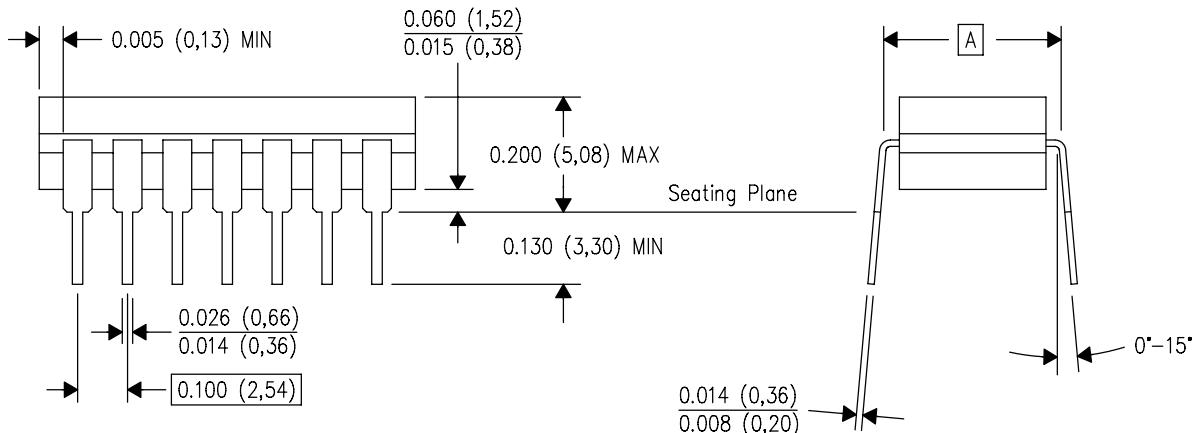
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

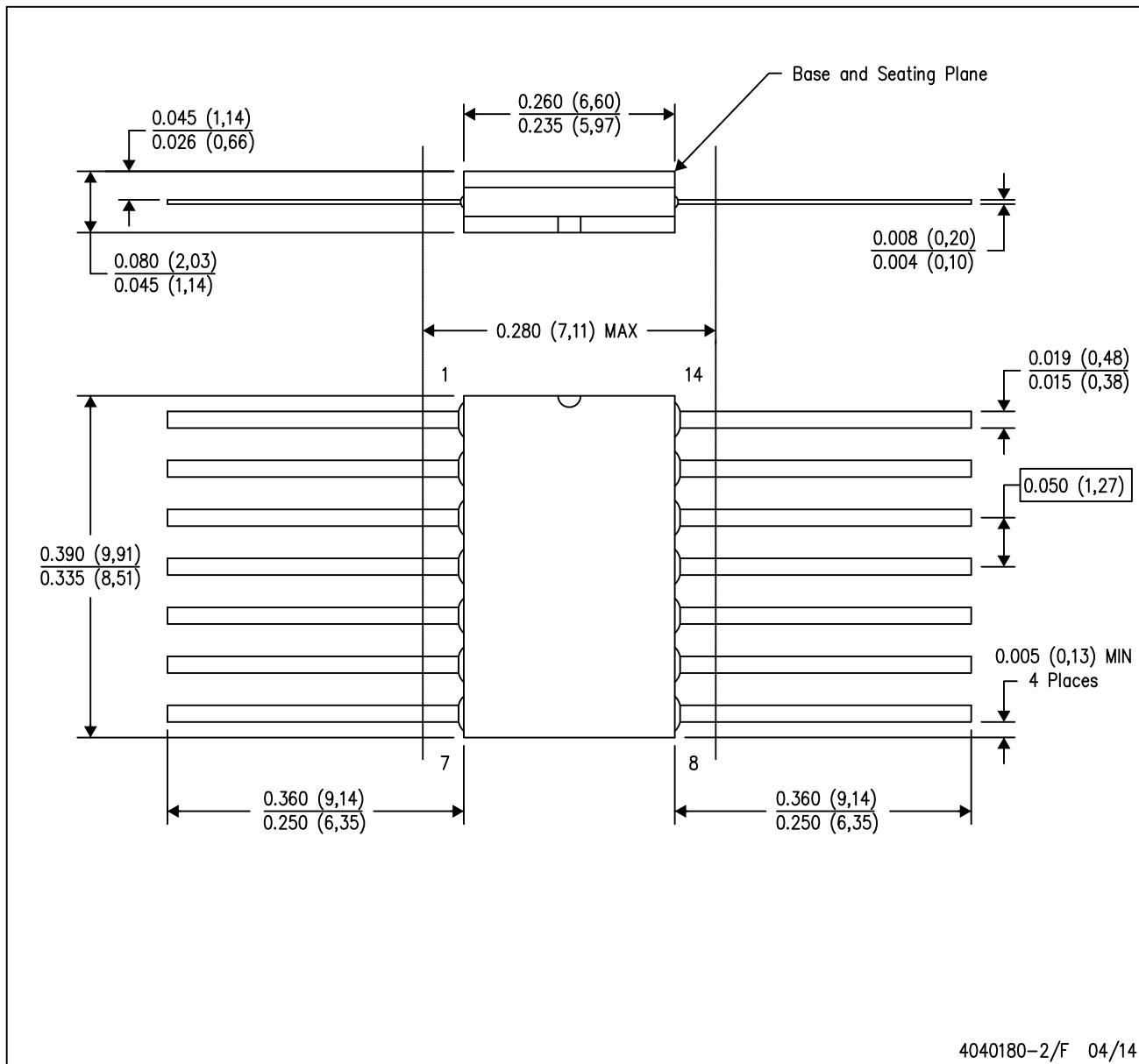


4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



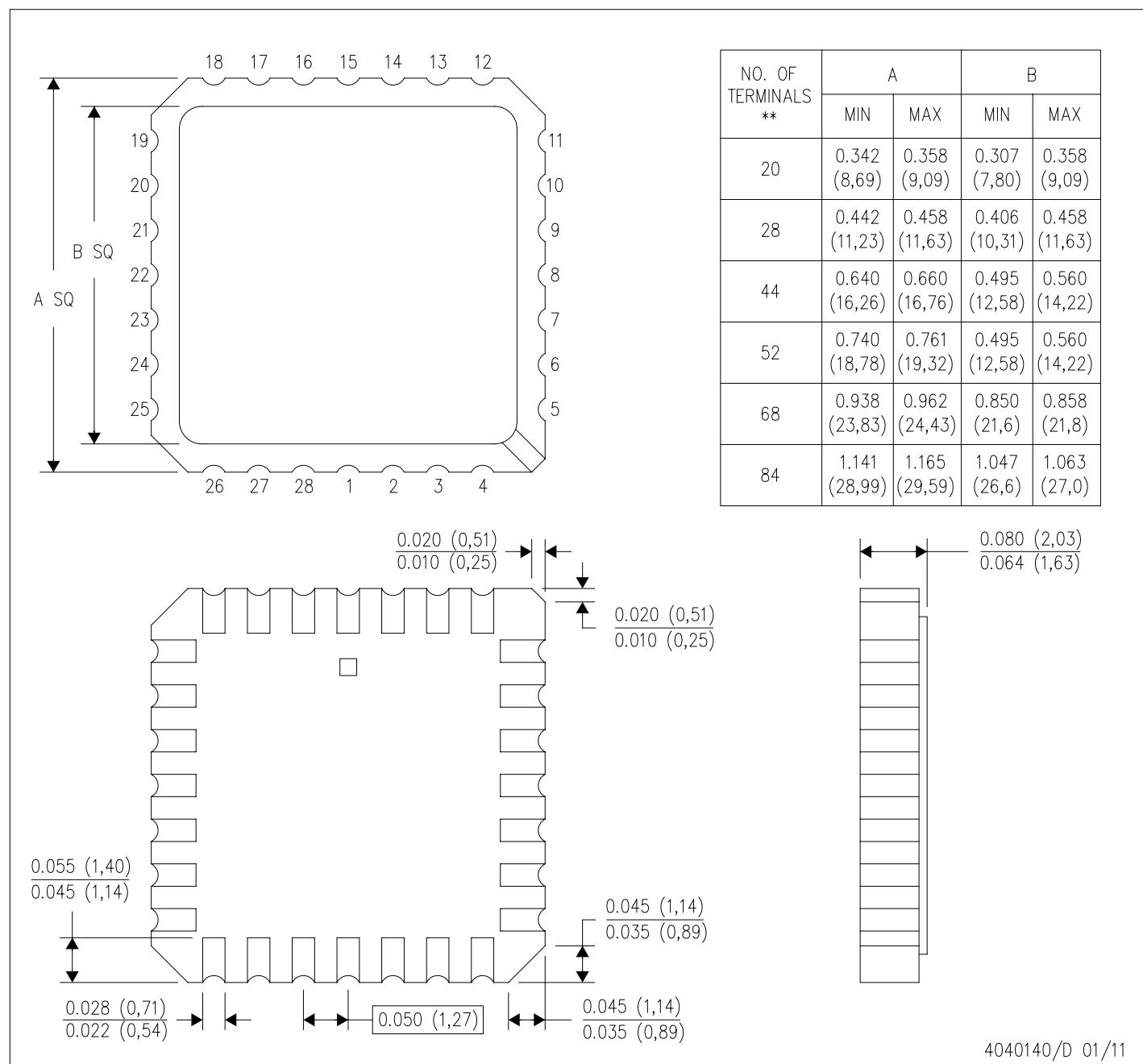
NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- This package can be hermetically sealed with a ceramic lid using glass frit.
- Index point is provided on cap for terminal identification only.
- Falls within MIL-STD 1835 GDFP1-F14

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES:

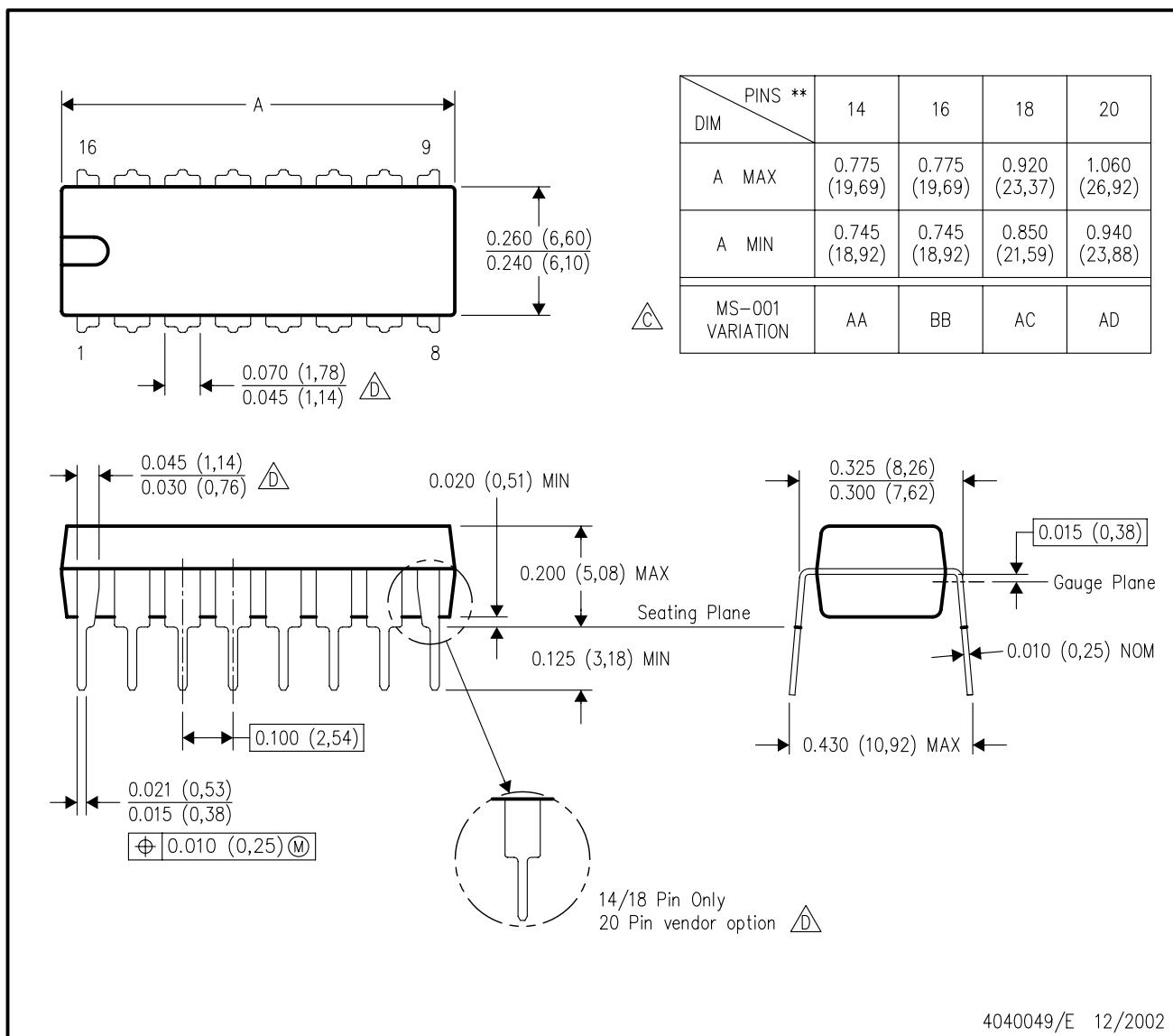
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004

4040140/D 01/11

N (R-PDIP-T**)

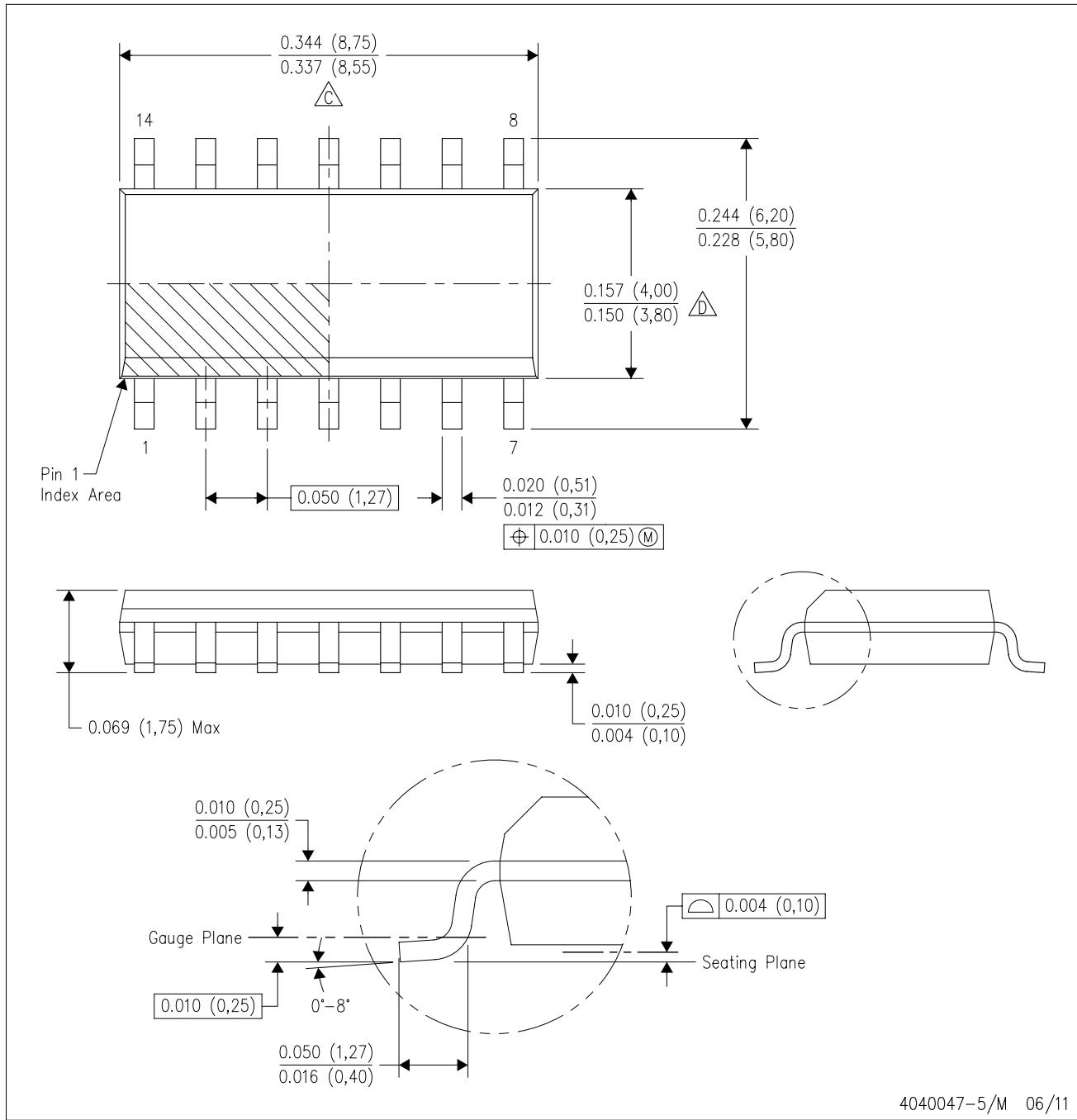
16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

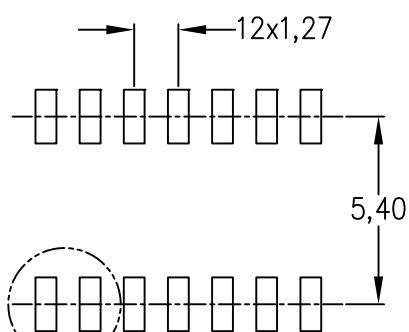
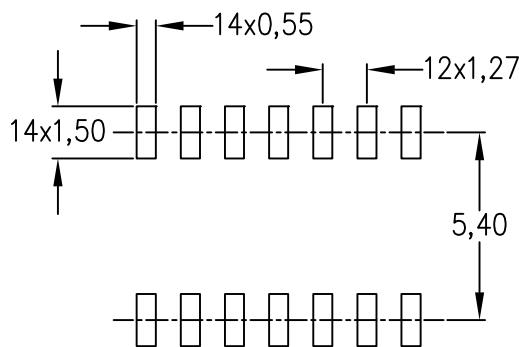
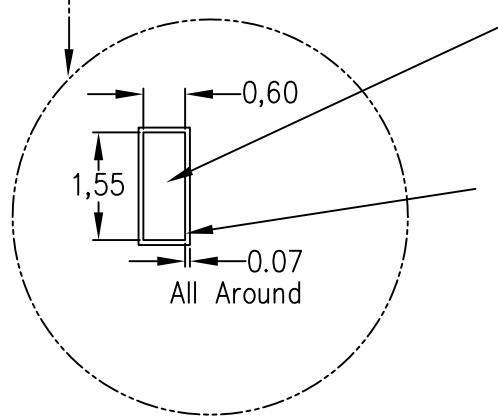
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Solder Mask Opening
(See Note E)

4211283-3/E 08/12

NOTES:

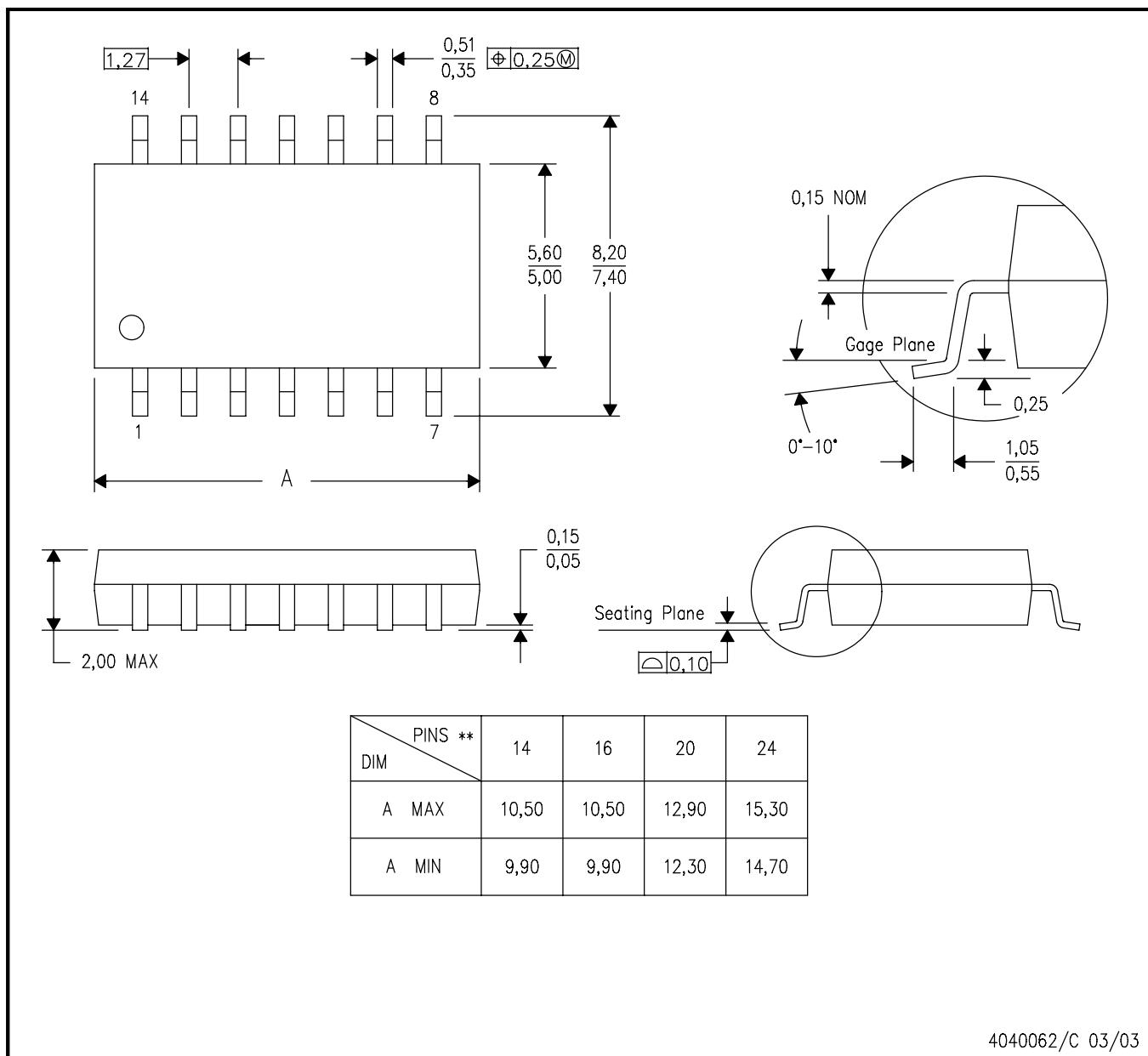
- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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