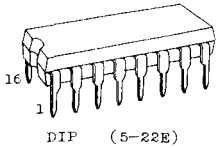
## TC74HC75P 4-BIT D-TYPE LATCH

The TC74HC75 is a high speed CMOS 4-BIT D-TYPE LATCH fabricated with silicon gate $C^2MOS$ technology.

It achieves the high speed operation similar to equivalent LS TTL while maintaining the CMOS low power dissipation.

It contains two groups of 2-bit latches controled by a enable input (G1·2 or G3·4). And those two latch groups can be used in the different circuits.

Each latch has Q and $\overline{Q}$ outputs (1Q thru 4Q and $1\overline{Q}$ thru $4\overline{Q}$). The data applied to the data input is transfered to the Q and $\overline{Q}$ outputs when the enable input is taken high and the outputs will follow the data input as long as the enable input is kept high. When the enable input is taken low, the information data applied to the data input at a time is retained at the outputs. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

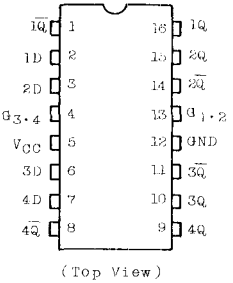


DIP (5-22E)

FEATURES:

- High Speed.....$t_{pd}$=16ns(Typ.) at $V_{CC}$=5V
- Low Power Dissipation.....$I_{CC}$=2μA(Max.) at Ta=25°C
- High Noise Immunity.....$V_{NIH}$=$V_{HIL}$=28% $V_{CC}$(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=$I_{OL}$=4mA
- Balanced Propagation Delays...$t_{pLH}$≒$t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V~6V
- Pin and Function Compatible with 74LS75

PIN ASSIGNMENT



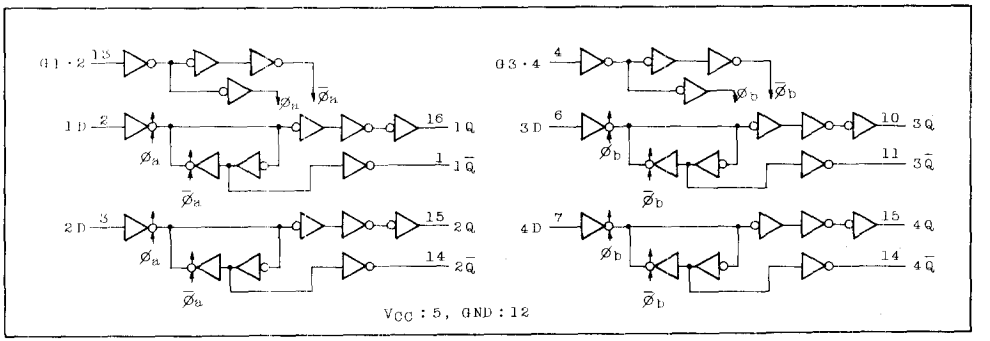
(Top View)

TRUTH TABLE

| INPUTS | | OUTPUTS | | FUNCTION |
|---|---|---|---|---|
| D | G | Q | $\overline{Q}$ | |
| L | H | L | H | - |
| H | H | H | L | - |
| X | L | $Q_n$ | $\overline{Q}_n$ | LATCH |

X : Don't care

LOGIC DIAGRAM

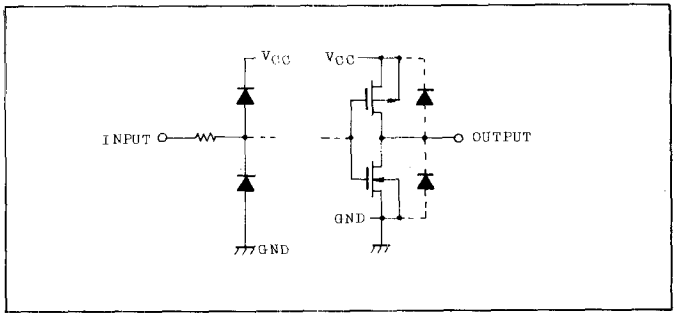



ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | VALUE | UNIT |
|---|---|---|---|
| Supply Voltage Range | $V_{CC}$ | -0.5 ~ 7 | V |
| DC Input Voltage | $V_{IN}$ | -0.5 ~ $V_{CC}$+0.5 | V |
| DC Output Voltage | $V_{OUT}$ | -0.5 ~ $V_{CC}$+0.5 | V |
| Input Diode Current | $I_{IK}$ | ±20 | mA |
| Output Diode Current | $I_{OK}$ | ±20 | mA |
| DC Output Current | $I_{OUT}$ | ±25 | mA |
| DC $V_{CC}$/Ground Current | $I_{CC}$ | ±50 | mA |
| Power Dissipation | $P_D$ | 500* | mW |
| Storage Temperature | $T_{stg}$ | -65 ~ 150 | °C |
| Lead Temperature 10sec | $T_L$ | 300 | °C |

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

INPUT and OUTPUT EQUIVALENT CIRCUIT



RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | LIMIT | UNIT |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 2 ~ 6 | V |
| Input Voltage | $V_{IN}$ | 0 ~ $V_{CC}$ | V |
| Output Voltage | $V_{OUT}$ | 0 ~ $V_{CC}$ | V |
| Operating Temperature | $T_{opr}$ | -40 ~ 85 | °C |
| Input Rise and Fall Time | $t_r$, $t_f$ | 0 ~ 1000 ($V_{CC}$=2.0V)<br>0 ~ 500 ($V_{CC}$=4.5V)<br>0 ~ 400 ($V_{CC}$=6.0V) | ns |

DC ELECTRICAL CHARACTERISTICS

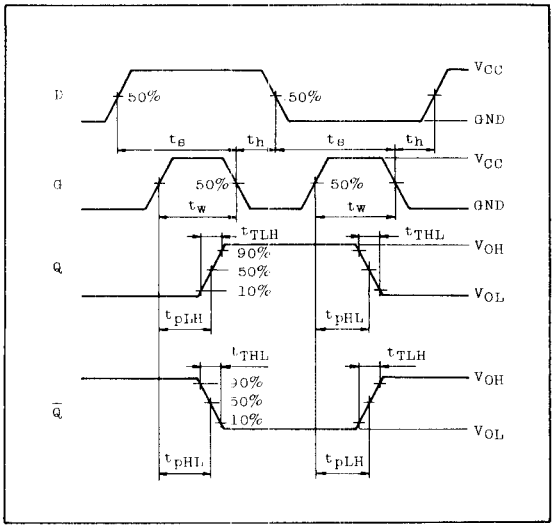
| PARAMETER | SYMBOL | TEST CONDITION | | | Ta=25°C | | | Ta=-40~85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{CC}$ | MIN. | TYP. | MAX. | MIN. | MAX. | |
| High-Level Input Voltage | $V_{IH}$ | | | 2.0 | 1.5 | - | - | 1.5 | - | V |
| | | | | 4.5 | 3.15 | - | - | 3.15 | - | |
| | | | | 6.0 | 4.2 | - | - | 4.2 | - | |
| Low-Level Input Voltage | $V_{IL}$ | | | 2.0 | - | - | 0.5 | - | 0.5 | V |
| | | | | 4.5 | - | - | 1.35 | - | 1.35 | |
| | | | | 6.0 | - | - | 1.8 | - | 1.8 | |
| High-Level Output Voltage | $V_{OH}$ | $V_{IN}$= $V_{IH}$ or $V_{IL}$ | $I_{OH}$=-20μA | 2.0 | 1.9 | 2.0 | - | 1.9 | - | V |
| | | | | 4.5 | 4.4 | 4.5 | - | 4.4 | - | |
| | | | | 6.0 | 5.9 | 6.0 | - | 5.9 | - | |
| | | | $I_{OH}$=-4mA | 4.5 | 4.18 | 4.31 | - | 4.13 | - | |
| | | | $I_{OH}$=-5.2mA | 6.0 | 5.68 | 5.80 | - | 5.63 | - | |
| Low-Level Output Voltage | $V_{OL}$ | $V_{IN}$= $V_{IH}$ or $V_{IL}$ | $I_{OL}$=20μA | 2.0 | - | 0.0 | 0.1 | - | 0.1 | V |
| | | | | 4.5 | - | 0.0 | 0.1 | - | 0.1 | |
| | | | | 6.0 | - | 0.0 | 0.1 | - | 0.1 | |
| | | | $I_{OL}$=4mA | 4.5 | - | 0.17 | 0.32 | - | 0.37 | |
| | | | $I_{OL}$=5.2mA | 6.0 | - | 0.18 | 0.32 | - | 0.37 | |
| Input Leakage Current | $I_{IN}$ | $V_{IN}$=$V_{CC}$ or GND | | 6.0 | - | - | ±0.1 | - | ±1.0 | μA |
| Quiescent Supply Current | $I_{CC}$ | $V_{IN}$=$V_{CC}$ or GND | | 6.0 | - | - | 2.0 | - | 20.0 | |

AC ELECTRICAL CHARACTERISTICS ($C_L$=50pF, Input $t_r=t_f$=6ns)

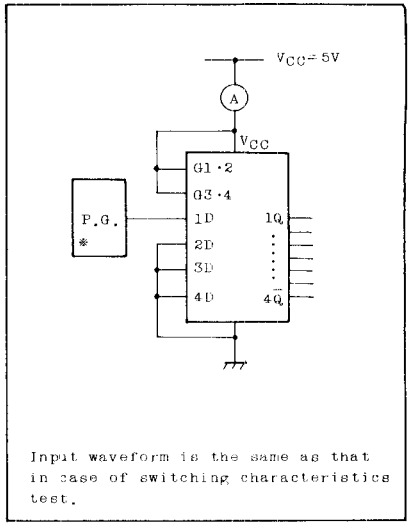
| PARAMETER | SYMBOL | TEST CONDITION | | Ta=25°C | | | Ta=-40~85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ | MIN. | TYP. | MAX. | MIN. | MAX. | |
| Output Transition Time | $t_{TLH}$ $t_{THL}$ | | 2.0 | - | 30 | 75 | - | 90 | ns |
| | | | 4.5 | - | 8 | 15 | - | 18 | |
| | | | 6.0 | - | 7 | 13 | - | 16 | |
| Propagation Delay Time (DATA - Q, $\overline{Q}$) | $t_{pLH}$ $t_{pHL}$ | | 2.0 | - | 60 | 145 | - | 175 | |
| | | | 4.5 | - | 18 | 29 | - | 35 | |
| | | | 6.0 | - | 16 | 25 | - | 30 | |
| Propagation Delay Time (G - Q, $\overline{Q}$) | $t_{pLH}$ $t_{pHL}$ | | 2.0 | - | 75 | 160 | - | 195 | |
| | | | 4.5 | - | 20 | 32 | - | 39 | |
| | | | 6.0 | - | 17 | 28 | - | 34 | |
| Minimum Pulse Width (G) | $t_{w(H)}$ | | 2.0 | - | 30 | 75 | - | 90 | |
| | | | 4.5 | - | 8 | 15 | - | 18 | |
| | | | 6.0 | - | 7 | 13 | - | 16 | |
| Minimum Set-up Time | $t_s$ | | 2.0 | - | 5 | 50 | - | 60 | |
| | | | 4.5 | - | 2 | 10 | - | 12 | |
| | | | 6.0 | - | 2 | 9 | - | 11 | |
| Minimum Hold Time | $t_h$ | | 2.0 | - | - | 25 | - | 30 | |
| | | | 4.5 | - | - | 5 | - | 6 | |
| | | | 6.0 | - | - | 4 | - | 5 | |
| Input Capacitance | $C_{IN}$ | | | - | 5 | 10 | - | 10 | pF |
| Power Dissipation Capacitance | $C_{PD}$(1) | | | - | 48 | - | - | - | |

Note (1) $C_{PD}$ is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}/4$ (per Latch)

SWITCHING CHARACTERISTICS TEST WAVEFORM

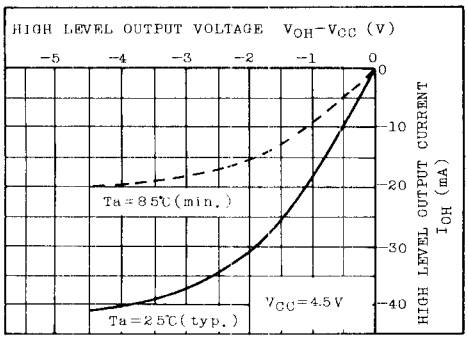



$I_{CC}$(opr) TEST CIRCUIT

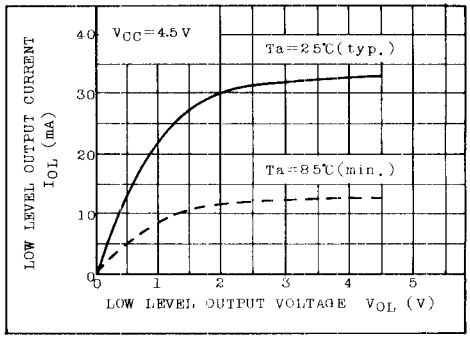



Input waveform is the same as that in case of switching characteristics test.

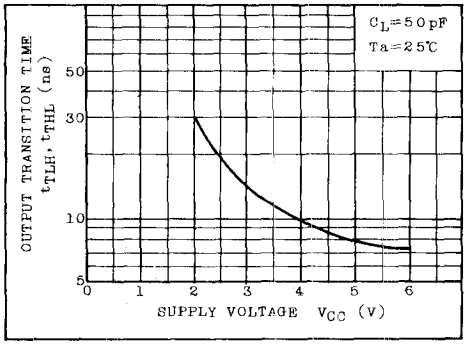
$I_{OH}$ CHARACTERISTICS



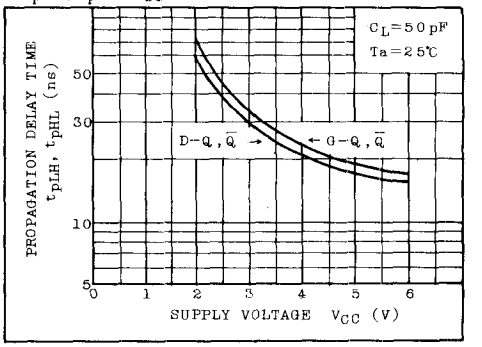

$I_{OL}$ CHARACTERISTICS



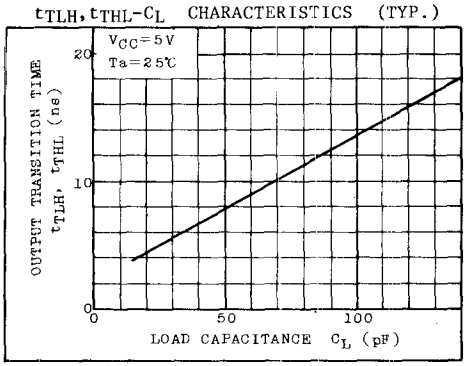
$t_{TLH}, t_{THL}$-$V_{CC}$ CHARACTERISTICS (TYP.)




$t_{pLH}, t_{pHL}$-$V_{CC}$ CHARACTERISTICS (TYP.)




$t_{TLH}, t_{THL}$-$C_L$ CHARACTERISTICS (TYP.)




$t_{pLH}, t_{pHL}$-$C_L$ CHARACTERISTICS (TYP.)