

MN101C93K

Type	MN101C93K	MN101CF93K
Internal ROM type	Mask ROM, FLASH	Mask ROM
ROM (byte)	224K	
RAM (byte)	6K	
Package (Lead-free)	LQFP100-P-1414	
Minimum Instruction Execution Time	0.125 μ s (at 3.0 V to 3.6 V, 8 MHz) 62.5 μ s (at 3.0 V to 3.6 V, 32 kHz), 0.167 μ s (at 3.0 V to 3.6 V, 6 MHz) 62.5 μ s (at 3.0 V to 3.6 V, 32 kHz)	0.125 μ s (at 3.0 V to 3.6 V, 8 MHz) 62.5 μ s (at 3.0 V to 3.6 V, 32 kHz)

■ Interrupts

RESET, Watchdog, External 0 to 5, External 6 (key interrupt dedicated), Timer 0 to 3, Timer 6, Timer 7 (2 systems), Timer 8 (2 systems), Time base, Serial 0 (2 systems), Serial 1 (2 systems), Serial 3, A/D conversion finish, Automatic transfer finish, USB interrupts

■ Timer Counter

Timer counter 0 : 8-bit $\times$ 1

(square-wave/8-bit PWM output, event count, generation of remote control carrier, simple pulse width measurement, added pluse (2-bit) system PWM output)

(square-wave/PWM output to large current terminal PC3 possible)

Clock source..... 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input

Interrupt source coincidence with compare register 0

Timer counter 1 : 8-bit $\times$ 1 (square-wave output, event count, serial transfer clock output, synchronous output event)

Clock source..... 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input

Interrupt source coincidence with compare register 1

Timer counter 0, 1 can be cascade-connected.

Timer counter 2 : 8-bit $\times$ 1

(square-wave output, added pluse (2-bit) system PWM output, PWM output, serial transfer clock output, event count, synchronous output event, simple pulse width measurement)

(square-wave/PWM output to large current terminal PC5 possible)

Clock source..... 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input

Interrupt source coincidence with compare register 2

Timer counter 3 : 8-bit $\times$ 1 (square-wave output, event count, generation of remote control carrier, serial transfer clock)

Clock source..... 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input

Interrupt source coincidence with compare register 3

Timer counter 2, 3 can be cascade-connected.

Timer counter 6 : 8-bit freerun timer

Clock source..... 1/1 of system clock frequency; 1/1, 1/128, 1/8192 of OSC oscillation clock frequency; 1/1, 1/128, 1/8192 of XI oscillation clock frequency

Interrupt source coincidence with compare register 6

Timer counter 7 : 16-bit $\times$ 1

(square-wave output, 16-bit PWM output (cycle / duty continuous variable), event count, synchronous output event, pulse width measurement, input capture, real time output control, high performance IGBT output (Cycle/Duty can be changed constantly))

(square-wave/PWM output to large current terminal PC4 possible)

Clock source..... 1/1, 1/2, 1/4, 1/16 of system clock frequency; 1/1, 1/2, 1/4, 1/16 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency

Interrupt source coincidence with compare register 7 (2 lines), input capture register

Timer counter 8 : 16 bit × 1

(square-wave/16-bit PWM output [duty continuous variable], event count, pulse width measurement, input capture)

(square-wave/PWM output to large current terminal PC6 possible)

Clock source..... 1/1, 1/2, 1/4, 1/16 of system clock frequency; 1/1, 1/2, 1/4, 1/16 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency

Interrupt source coincidence with compare register 8 (2 lines), input capture register

Timer counters 7, 8 can be cascade-connected. (square-wave output, PWM is possible as a 32-bit timer.)

Time base timer (one-minute count setting)

Clock source..... 1/1 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency

Interrupt source 1/128, 1/256, 1/512, 1/1024, 1/4096, 1/8192, 1/16384, 1/32768 of clock source frequency

Watchdog timer

Interrupt source 1/65536, 1/262144, 1/1048576 of system clock frequency

■ Serial interface**Serial 0 : synchronous type/UART (full-duplex) × 1**

Clock source..... 1/2, 1/4 of system clock frequency; pulse output of timer counter 1 or 2; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency, external clock

Serial 1 : synchronous type/UART (full-duplex) × 1

Clock source..... 1/2, 1/4 of system clock frequency; pulse output of timer counter 1 or 2; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency, external clock

Serial 3 : synchronous type/single-master I²C × 1

Clock source..... 1/2, 1/4 of system clock frequency; pulse output of timer counter 2 or 3; 1/2, 1/4, 1/16, 1/32 of OSC oscillation clock frequency, external clock

■ DMA controller

Max. Transfer cycles : 255

Starting factor : external request, various types of interrupt, software

Transfer mode : 1-byte transfer, word transfer, burst transfer

■ USB Functions

Conforms to USB1.1.

USB transceiver built-in

Full-speed (12 Mbps) supported.

5 end points (FIFO built-in independently)

FIFO size

(EP0, 1, 2, 3, 4) : 16, 128, 128, 64, 64 bytes

• EP0

Control transfer

IN/OUT (two ways)

• EP1 to EP4

Interrupt/Bulk/Isochronous transfer supported.

Settable to IN or OUT.

Double Buffering function supported.

When the MAXP size is set to a half or less of the MAXFIFO size for each EP, the Double Buffering function is made valid automatically.

■ I/O Pins

I/O	84	Common use , Specified pull-up resistor available, Input/output selectable (bit unit)
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■ A/D converter

10-bit × 12-ch. (with S/H)

■ Display control function

LCD

47 segments × 4 commons (static, 1/2, 1/3, or 1/4 duty)

LCD power supply separated from VDD (usable if $VDD = VLCD \leq 3.6\text{ V}$)

LCD power shunt resistance contained

■ Special Ports

USB ports (D+, D-), buzzer output, remote control carrier signal output, high-current drive port, clock output

■ ROM Correction

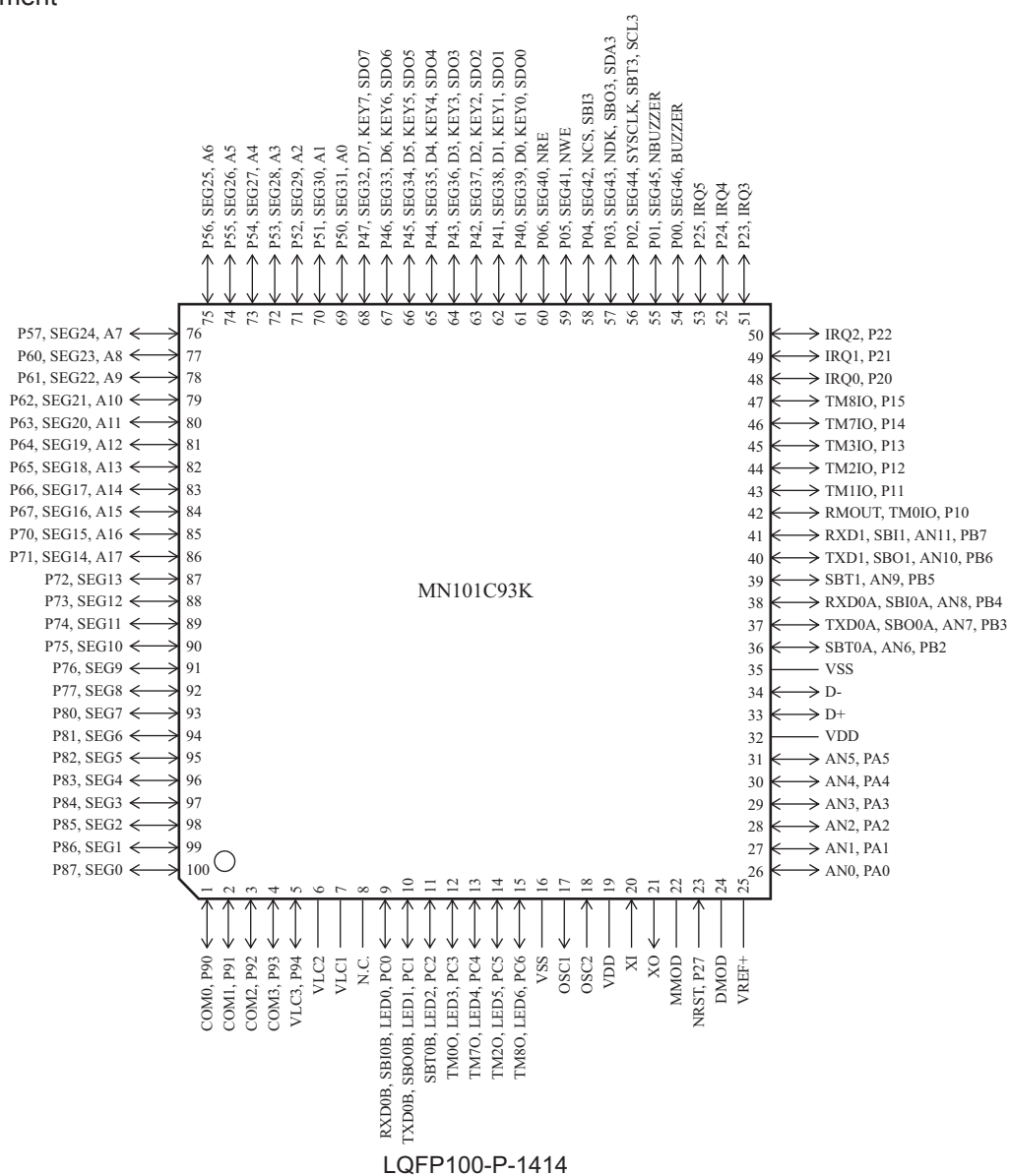
Correcting address designation : up to 7 addresses possible

■ Development tools

In-circuit Emulator

PX-ICE101C/D+PX-PRB101C93-LQFP100-P-1414-M (Under development)

■ Pin Assignment



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