

5 - 20GHz MMIC Amplifier with Integrated Bias

Features

- Excellent performance 5-18GHz:
 - High, flat gain ($15 \pm 0.5\text{dB}$)
 - Good return loss (15dB)
 - 17.5dBm P1dB, 20dBm Psat
- Mixed-signal 3.3V operation:
 - Similar small-signal performance
 - Good power (16.5dBm Psat)
- Quick and easy to use:
 - Self-biasing (5V or 3.3V supply)
 - Integrated blocking capacitors
- Very high isolation (-36dB)
- 100% DC, RF, and visually tested
- Size: 920x920um (36.2x36.2mil)
- Typically self-biased for low-cost Class-A operation
- Requires only a single 5V supply
- Both drain and both gate pads are available for higher-efficiency operation
- The device is AC coupled with integrated blocking capacitors

Description

The MMA021AA is a two-stage PHEMT high gain amplifier designed to be insensitive to process or temperature changes. Its high isolation makes it ideal for applications requiring both gain and isolation. The device can be operated at 5V 135mA, or 3.3V 108mA for integration with mixed-signal circuitry.

Application

The MMA021AA MMIC Amplifier with Integrated Bias is designed for digital radio, spread spectrum, electronic warfare, and broadband communication systems. It can be used as a LO or mixer isolation amplifier, a transmit amplifier in a radio system, or as a general isolation and gain block amplifier.

Key Characteristics: Vdd1 = Vdd2 = 5.0V, Vg1 = Vg2 = N/C, Idd1 = 65mA, Idd2 = 90mA, Zo=50Ω
Specifications pertain to wafer measurements with RF probes and DC bias cards @ 25°C

		5 - 18GHz			4.5 - 20GHz		
Parameter	Description	Min	Typ	Max	Min	Typ	Max
S21 (dB)	Small Signal Gain	14	15	-	12.5	14.5	-
Flatness ($\pm\text{dB}$)	Gain Flatness	-	0.5	0.8	-	1.0	2.0
S11 (dB)	Input Match	-	-15	-13	-	-15	-13
S22 (dB)	Output Match	-	-17	-11.5	-	-17	-12
S12 (dB)	Reverse Isolation	-	-36	-32	-	-36	-32
P1dB (dBm)	1dB Compressed Output Power	17	18	-	-	18	-
Psat (dBm)	Saturated Output Power	19	20	-	18.5	20	-
NF (dB)	Noise Figure	-	7	-	-	7.5	-

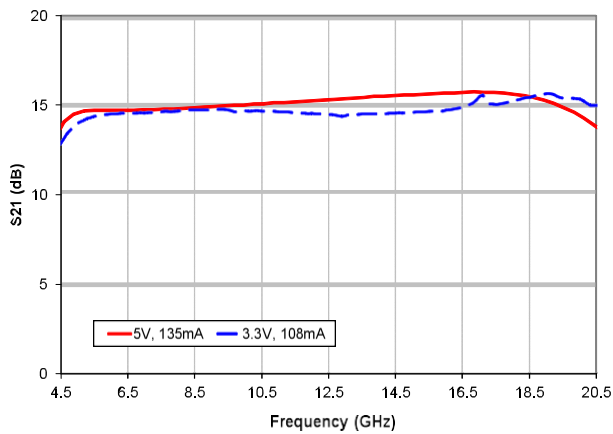
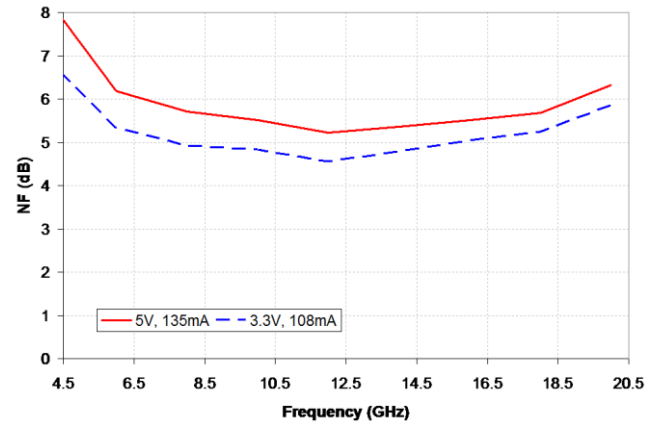
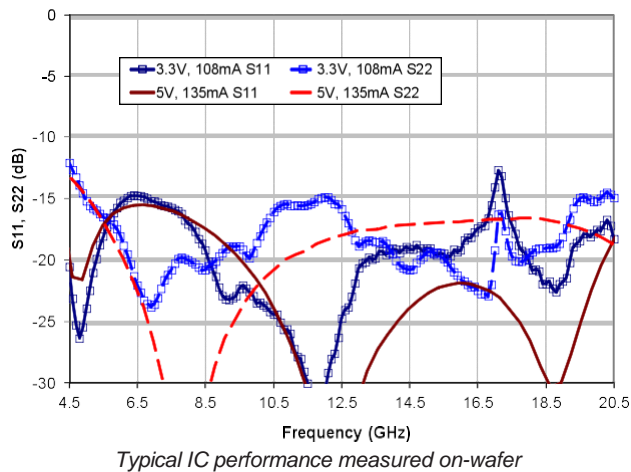
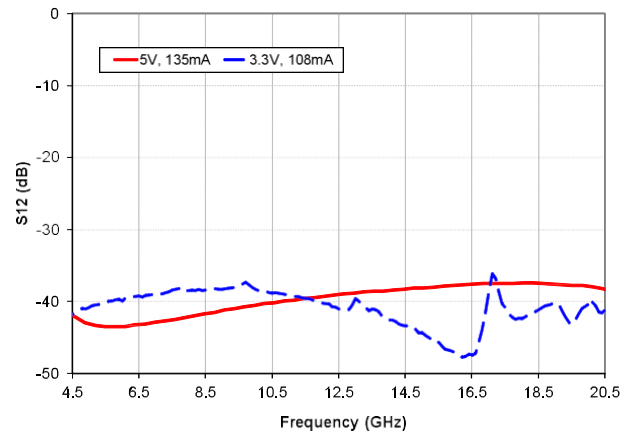
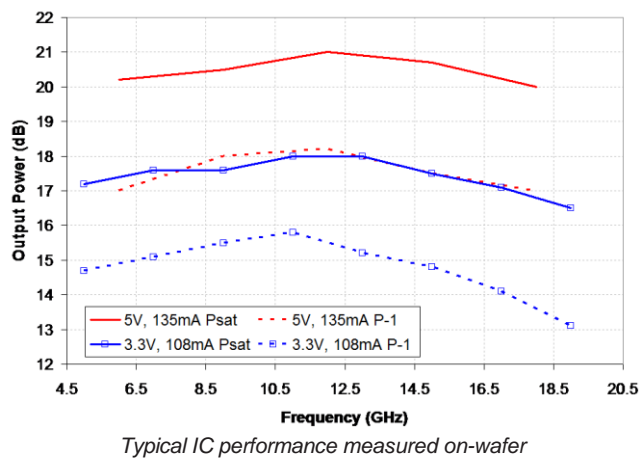
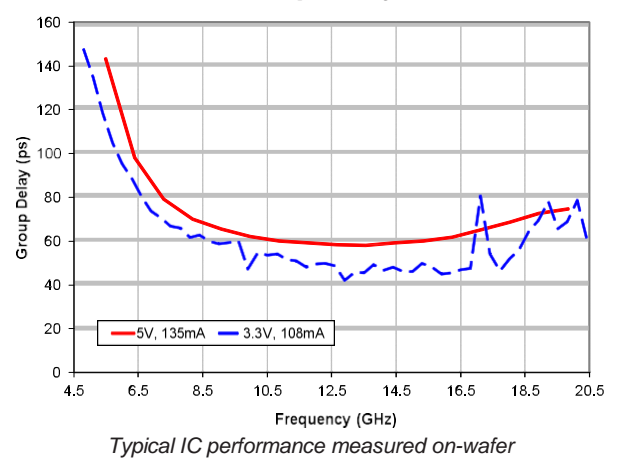
S21

Noise Figure

S11, S22

S12

Output Power

Group Delay


Table 1: Supplemental Specifications

Parameter	Description	Min	Typ	Max
Vdd1	Drain Bias Voltage FET1	3V	5V	6V
Idd1	Drain Bias Current FET1	-	65mA	90mA
Vdd2	Drain Bias Voltage FET2	3V	5V	6V
Idd2	Drain Bias Current FET2	-	90mA	110mA
Vgg1	Gate Bias Voltage FET1	-4V	N/C	+1V
Vgg2	Gate Bias Voltage FET2	-4V	N/C	+1V
P _{in}	Input Power (CW)	-	-	12dBm
P _{dc}	Power Dissipation	-	0.675W	-
T _{ch}	Channel Temperature	-	-	150°C
Θ _{ch}	Thermal Resistance (T _{case} =85°C)	-	60° C/W	-



Caution, ESD
Sensitive Device

DC Bias

The MMA021AA is typically biased by applying +5V to the two drain pads (Vdd1, Vdd2); the gates (Vgg1, Vgg2) will self-bias.

All four bias lines are available on-chip; both drains and both gates can be biased to different potentials. Grounded bond wires are not required, as the backside of the chip is both an RF and DC ground.

Negative potentials applied to the gates will reduce the drain current in that stage. This will increase the amplifier's efficiency by moving its operation closer to Class AB or B.

The MMA021AA can also be biased with +3.3V drain voltage. This yields good performance with the same supply used for mixed-signal circuitry or microprocessors.

Gain Control

ome gain control is available when operating the amplifier in the linear gain region. Negative voltage applied to Vgg1 and Vgg2 will reduce the amplifier gain. Additionally, Vdd1 and Vdd2 can also be used for linear low-frequency amplitude modulation.

Matching

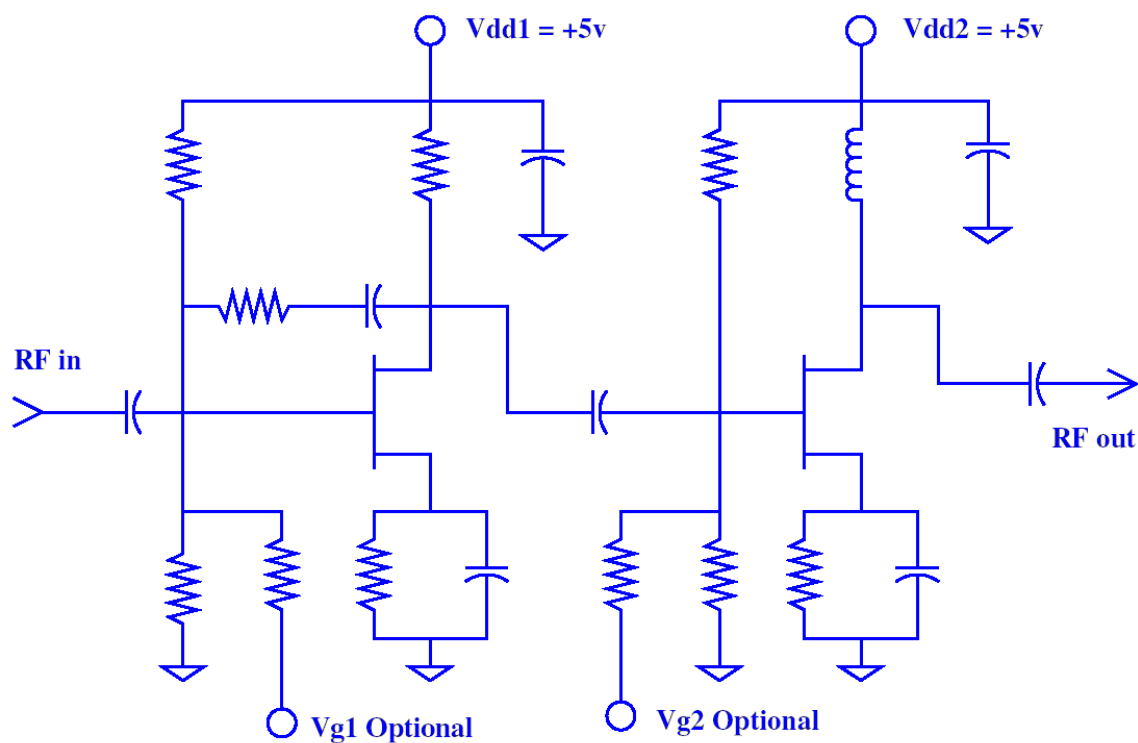
The MMA021AA has been designed with input and output impedances that best match a 50ohm system, and require no external matching networks.

Best performance will be obtained by using multiple short bondwires, or by using ribbon or mesh bondwires.

DC Blocks

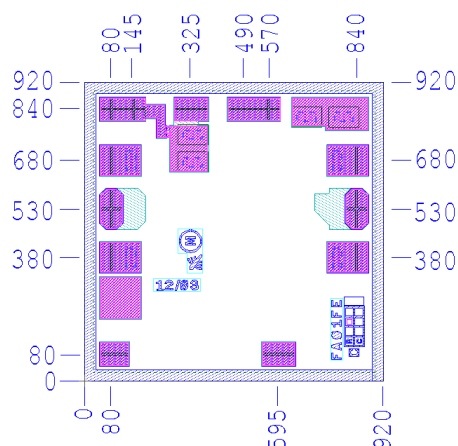
The amplifier is internally AC coupled to the RF input and output pads. DC blocking capacitors are not required for isolating bias voltages from external circuitry.

Low Frequency Schematic

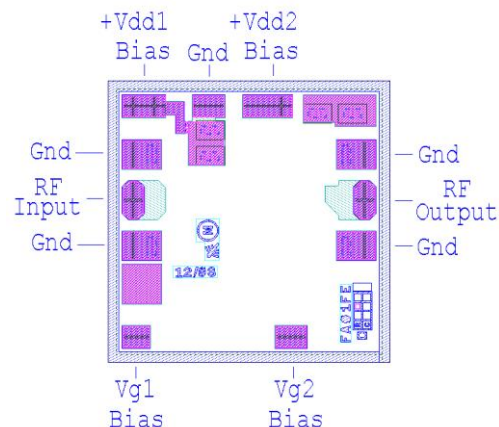


Chip layout showing pad locations.

All dimensions are in microns. Die thickness is 100 microns. Backside metal is gold, bond pad metal is gold.
Refer to Die Handling Application Note MM-APP-0001 (visit www.microsemi.com/mmics).



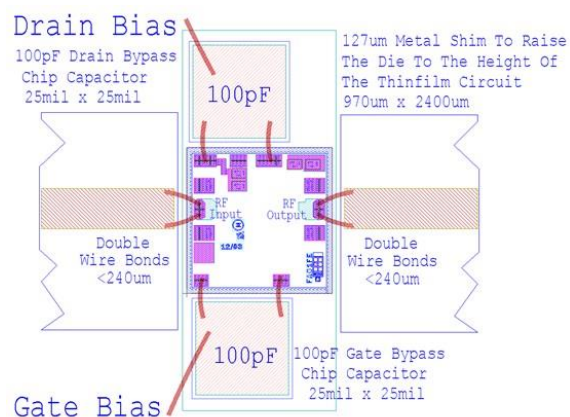
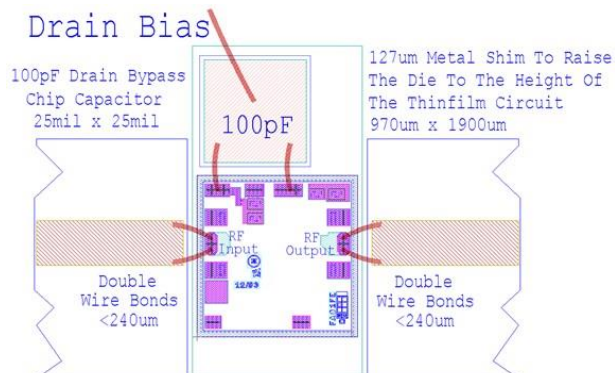
Chip size: 920x920um (36.2x36.2mil)
Chip size tolerance: $\pm 5\mu\text{m}$ (0.2mil)
Chip thickness: $100 \pm 10\mu\text{m}$ ($4 \pm 0.4\text{mil}$)
Pad dimensions: 80x80um (3.1x3.1mil)



All Dimensions Are in Microns

Single supply (self-biased) assembly diagram

Dual supply (externally-biased) assembly diagram



Pick-up and Chip Handling:

This MMIC has exposed air bridges on the top surface. **Do not pick up chip with vacuum on the die center;** handle from edges or with a custom collet.

Thermal Heat Sinking:

To avoid damage and for optimum performance, you must observe the maximum channel temperature and ensure adequate heat sinking.

ESD Handling and Bonding:

This MMIC is ESD sensitive; preventive measures should be taken during handling, die attach, and bonding.

Epoxy die attach is recommended. Please review our application note MM-APP-0001 handling and die attach recommendations, on our website for more handling, die attach and bonding information.

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