

FEATURES

R_{ON} : 300 Ω

Power Dissipation: 1.5mW

TTL/DTL/CMOS Direct Interface

Break-Before-Make Switching

Replaces DG506/DG507

CMOS 8 AND 16 CHANNEL ANALOG MULTIPLEXERS

AD7506, AD7507

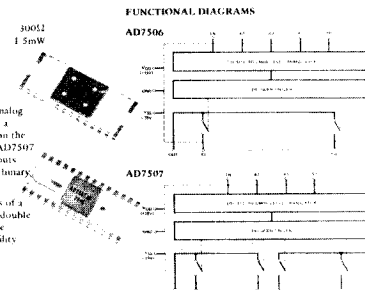
FEATURES

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GENERAL DESCRIPTION

The AD7506 is a monolithic CMOS 16-channel analog multiplexer packaged in a 28-pin DIP. It switches a common output to one of 16 inputs, depending on the state of four address lines and an "enable". The AD7507 is identical to the AD7506 except it has two outputs switched to two of 16 inputs depending on three binary address states and an "enable".

The AD7506 and AD7507 are excellent examples of a high-breakdown CMOS process combined with a double layer interconnect for high density. Both units are structurally passivated featuring increased stability and reliability.



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ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} - GND. +17V

V_{SS} - GND. -17V

V Between Any Switch Terminals. 25V

Digital Input Voltage Range. V_{DD} to GND

Switch Current (I_S , Continuous). 20mA

Switch Current (I_S , Surge)

1ms duration, 10% duty cycle. 35mA

Power Dissipation (Package)

28 pin Ceramic DIP

Up to +50°C. 1000mW

Derates above +50°C by. 10mW/°C

28 pin Plastic DIP

Up to +50°C. 1200mW

Derates above +50°C by. 12mW/°C

Operating Temperature

Plastic (J, K versions). 0 to +75°C

Ceramic (J, K versions). -25°C to +85°C

Ceramic (S, T versions). -55°C to +125°C

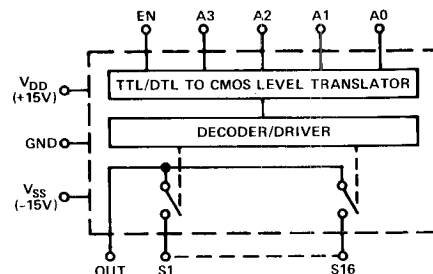
Storage Temperature. -65°C to +150°C

CAUTION:

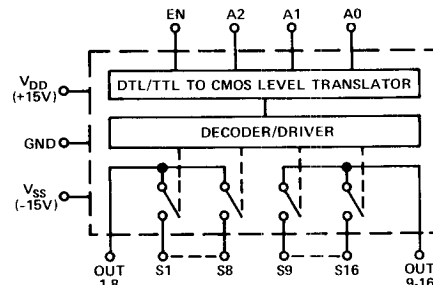
1. Do not apply voltages higher than V_{DD} and V_{SS} to any other terminal, especially when $V_{SS} = V_{DD} = 0V$ all other pins should be at 0V.
2. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

FUNCTIONAL DIAGRAMS

AD7506

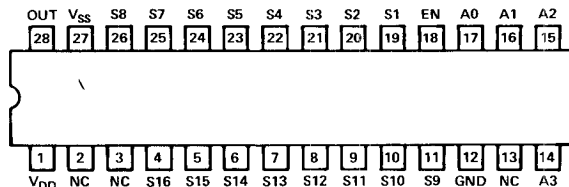


AD7507

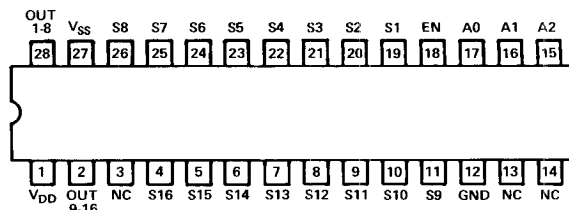


PIN CONFIGURATIONS (Top View)

AD7506



AD7507



SPECIFICATIONS

($V_{DD} = +15V$, $V_{SS} = -15V$ unless otherwise noted)

PARAMETER	VERSION ¹	SWITCH CONDITION	@ +25°C	OVER SPECIFIED TEMP. RANGE	TEST CONDITIONS
ANALOG SWITCH					
R_{ON}	J, K S, T	ON ON	300Ω typ, 450Ω max 400Ω max	550Ω max 500Ω max	$V_S = -10V$ to $+10V$, $I_S = 1mA$
R_{ON} vs. V_S	All	ON	15% typ		
R_{ON} vs. Temperature	All	ON	0.5%/°C typ		
ΔR_{ON} Between Switches	All	ON	4% typ		$V_S = 0V$, $I_S = 1mA$
R_{ON} vs. Temperature Between Switches	All	ON	0.05%/°C typ		
I_S	J, K S, T	OFF OFF	0.05nA typ, 5nA max 0.05nA typ, 1nA max	50nA max 50nA max	$V_S = -10V$, $V_{OUT} = +10V$
I_{OUT}	AD7506 S, T	J, K OFF	0.3nA typ, 20nA max 0.3nA typ, 10nA max	500nA max 500nA max	and $V_S = +10V$, $V_{OUT} = -10V$
	AD7507 S, T	J, K OFF	0.3nA typ, 10nA max 0.3nA typ, 5nA max	250nA max 250nA max	"Enable" Low
$I_{OUT} - I_S$	AD7506 S, T	J, K ON	0.3nA typ, 20nA max 0.3nA typ, 10nA max	500nA max 500nA max	$V_S = 0$
	AD7507 S, T	J, K ON	0.3nA typ, 10nA max 0.3nA typ, 5nA max	250nA max 250nA max	
DIGITAL CONTROL					
V_{INL}	J, S			0.8V max 3.0V min	Note 2
V_{INH}	K, T			2.4V min	
I_{INL} or I_{INH}	All		10μA max	30μA max	
C_{IN}	All		3pF typ		
DYNAMIC CHARACTERISTICS³					
$t_{TRANSITION}$	J, S K, T		700ns typ 700ns typ, 1000ns max		$V_{IN}: 0$ to $3.0V$
t_{OPEN}	All		100ns typ		
$t_{ON} (E_N)$	J, S K, T		0.8μs typ 1.5μs max		$V_{EN}: 0$ to $3.0V$
$t_{OFF} (E_N)$	J, S K, T		0.8μs typ 1μs max		
"OFF" Isolation	All		70dB typ		$V_{EN} = 0$, $R_L = 200Ω$, $C_L = 3.0pF$, $V_S = 3.0V$ rms, $f = 50kHz$
C_S	All	OFF	5pF typ		
C_{OUT}	AD7506 AD7507	All OFF	40pF typ 20pF typ		
C_{S-OUT}	All	OFF	0.5pF typ		
C_{SS} Between Any Two Switches	All	OFF	0.5pF typ		
POWER SUPPLY					
I_{DD}	J, K S, T	OFF OFF	0.05mA typ, 1mA max 0.05mA typ, 1mA max	2mA max	All Digital Inputs Low
I_{SS}	J, K S, T	OFF OFF	0.05mA typ, 1mA max 0.05mA typ, 1mA max	2mA max	
I_{DD}	J, K S, T	ON ON	0.3mA typ, 1mA max 0.3mA typ, 1mA max	2mA max	All Digital Inputs High
I_{SS}	J, K S, T	ON ON	0.05mA typ, 1mA max 0.05mA typ, 1mA max	2mA max	

NOTES:

¹ JN, KN versions specified for 0 to +75°C; JD, KD versions for -55°C to +85°C; and SD, TD versions for -55°C to +125°C.

² A pullup resistor, typically 1-2kΩ is required to make the J and S versions compatible with TTL/DTL. The maximum value is determined by the output leakage current of the driver gate when in the high state.

³ AC parameters are sample tested to ensure conformance to specifications.

Specifications subject to change without notice.

TRUTH TABLES

AD7506					
A ₃	A ₂	A ₁	A ₀	E _N	"ON"
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16
X	X	X	X	0	None

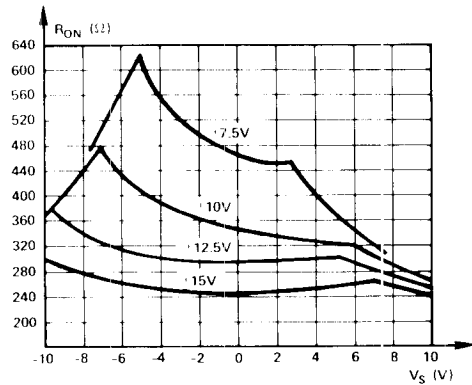
AD7507				
A ₂	A ₁	A ₀	E _N	"ON"
0	0	0	1	1 & 9
0	0	1	1	2 & 10
0	1	0	1	3 & 11
0	1	1	1	4 & 12
1	0	0	1	5 & 13
1	0	1	1	6 & 14
1	1	0	1	7 & 15
1	1	1	1	8 & 16
X	X	X	0	None

ORDERING INFORMATION

Plastic (Suffix N)	Ceramic (Suffix D)	Operating Temperature Range
AD7506JN AD7506KN AD7507JN AD7507KN		0 to +75°C
	AD7506JD AD7506KD AD7507JD AD7507KD	-25°C to +85°C
	AD7506SD AD7506TD AD7507SD AD7507TD	-55°C to +125°C

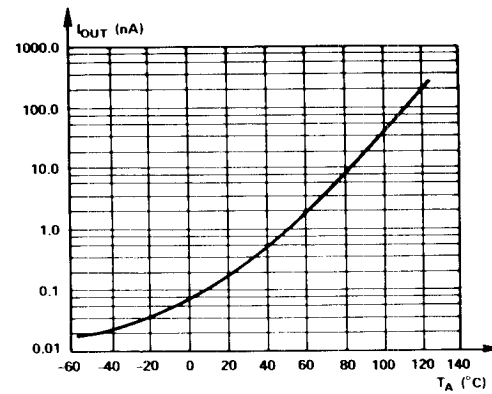
Typical Performance Characteristics

1. R_{ON} vs. V_S

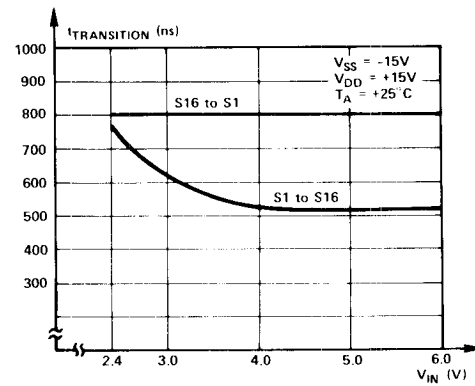


At Different Power Supplies

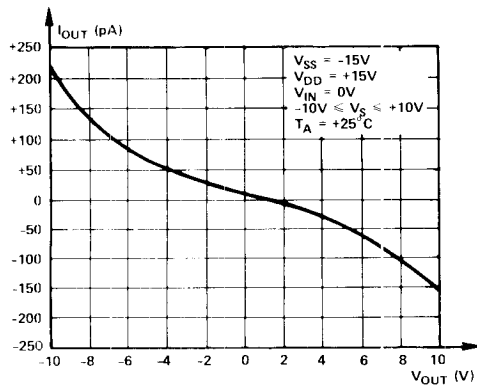
3. I_{OUT} vs. T_A



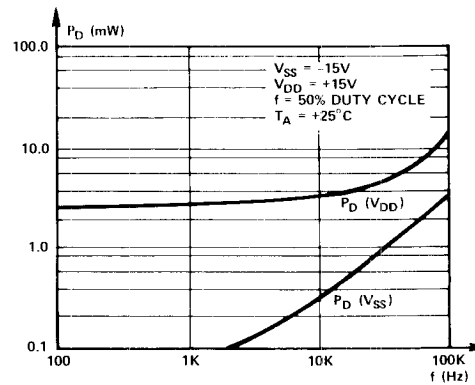
4. $t_{TRANSITION}$ vs. V_{IN}



2. I_{OUT} vs. V_{OUT}

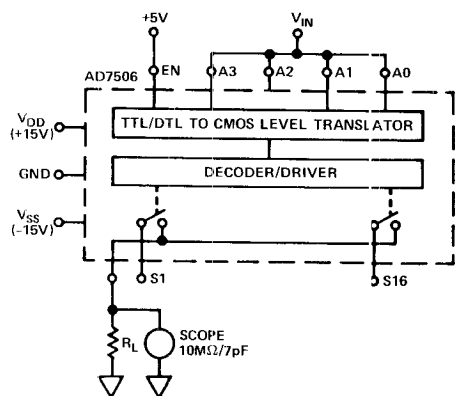


5. P_D vs. Logic Frequency

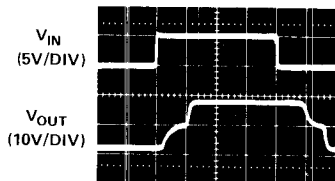


TYPICAL SWITCHING CHARACTERISTICS

TEST CIRCUIT 1

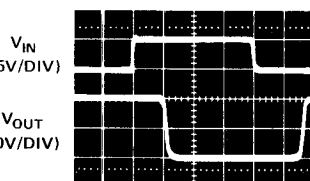


0.5μs/DIV



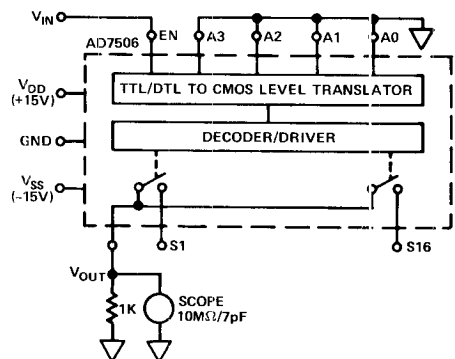
$S_1 = -10V, S_{16} = +10V,$
 $S_2 - S_{15} = 0V, R_L = 1K$

0.5μs/DIV

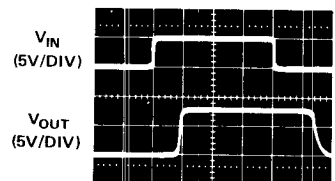


$S_1 = +10V, S_2 = -10V,$
 $S_2 - S_{15} = 0V, R_L = \infty$

TEST CIRCUIT 2

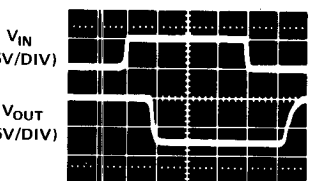


0.5μs/DIV



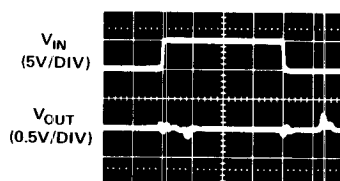
$S_1 \text{ through } S_{16} = +10V$

0.5μs/DIV



$S_1 \text{ through } S_{16} = -10V$

0.5μs/DIV

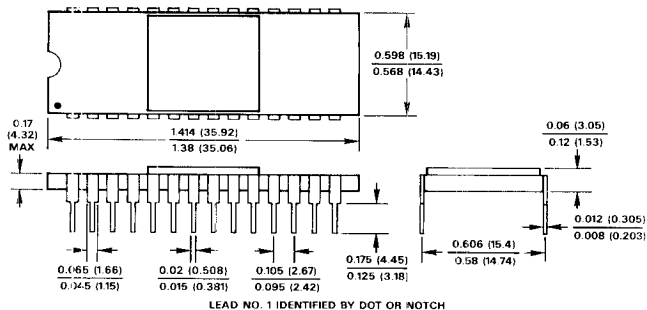


$S_1 \text{ through } S_{16} = 0V$

OUTLINE DIMENSIONS

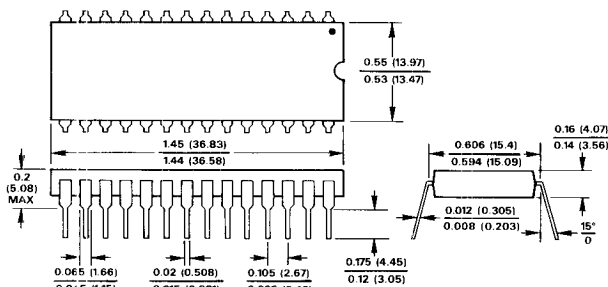
Dimensions shown in inches and (mm).

28-PIN CERAMIC DIP (SUFFIX D)



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH

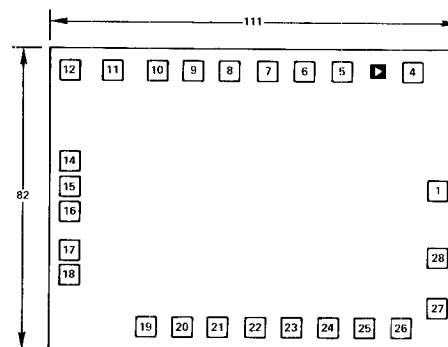
28-PIN PLASTIC DIP (SUFFIX N)



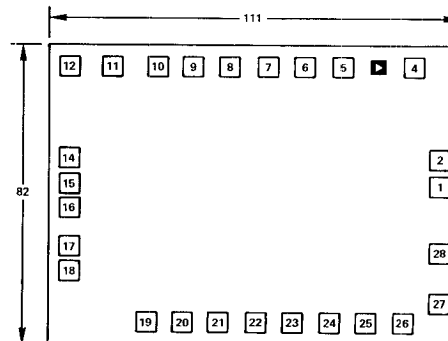
LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH

BONDING DIAGRAMS

AD7506



AD7507



All bonding pads are 4 x 4 MIL.
 All pad numbers correspond with DIP package pin configuration.