# MC74HC541A

# Octal 3-State Noninverting Buffer/Line Driver/Line Receiver

## High−Performance Silicon−Gate CMOS

The MC74HC541A is identical in pinout to the LS541. The device inputs are compatible with Standard CMOS outputs. External pull−up resistors make them compatible with LSTTL outputs.

The HC541A is an octal noninverting buffer/line driver/line receiver designed to be used with 3−state memory address drivers, clock drivers, and other bus−oriented systems. This device features inputs and outputs on opposite sides of the package and two ANDed active−low output enables.

The HC541A is similar in function to the HC540A, which has inverting outputs.

### Features

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1 µA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7 A Requirements
- Chip Complexity: 134 FETs or 33.5 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
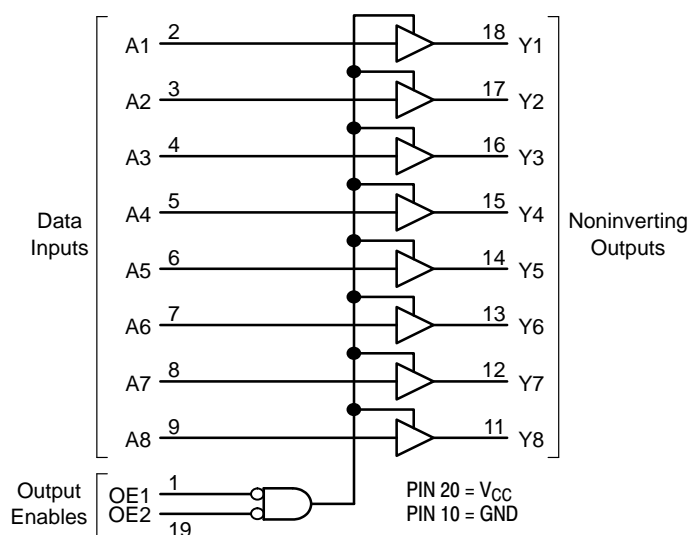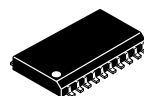- These Devices are Pb−Free and are RoHS Compliant
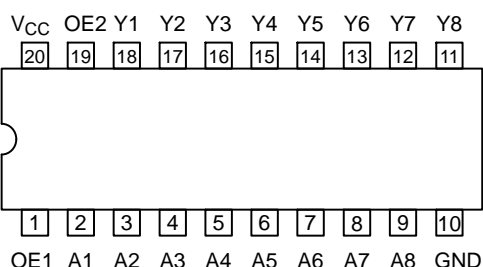


**Figure 1. Logic Diagram**

PIN 20 = V$_{CC}$
PIN 10 = GND

**SOIC−20**
**DW SUFFIX**
**CASE 751D**

**TSSOP−20**
**DT SUFFIX**
**CASE 948E**

### PIN ASSIGNMENT



| V$_{CC}$ | OE2 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 | Y8 |
| 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
| OE1 | A1 | A2 | A3 | A4 | A5 | A6 | A7 | A8 | GND |

### MARKING DIAGRAMS



HC541A
AWLYYWWG

HC
541A
ALYW▪
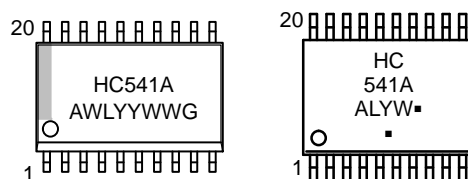
**SOIC−20**

**TSSOP−20**

| A | = Assembly Location |
| WL, L | = Wafer Lot |
| YY, Y | = Year |
| WW, W | = Work Week |
| G or ▪ | = Pb−Free Package |

(Note: Microdot may be in either location)

### FUNCTION TABLE

| Inputs | | | Output Y |
|---|---|---|---|
| OE1 | OE2 | A | |
| L | L | L | L |
| L | L | H | H |
| H | X | X | Z |
| X | H | X | Z |

X = Don't Care
Z = High Impedance

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# MC74HC541A

**MAXIMUM RATINGS**

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | | −0.5 to +7.0 | V |
| $V_I$ | DC Input Voltage | | $−0.5 \leq V_I \leq V_{CC} + 0.5$ | V |
| $V_O$ | DC Output Voltage (Note 1) | | $−0.5 \leq V_O \leq V_{CC} + 0.5$ | V |
| $I_{IK}$ | DC Input Diode Current | | ±20 | mA |
| $I_{OK}$ | DC Output Diode Current | | ±35 | mA |
| $I_O$ | DC Output Sink Current | | ±35 | mA |
| $I_{CC}$ | DC Supply Current per Supply Pin | | ±75 | mA |
| $I_{GND}$ | DC Ground Current per Ground Pin | | ±75 | mA |
| $T_{STG}$ | Storage Temperature Range | | −65 to +150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds | | 260 | °C |
| $T_J$ | Junction Temperature under Bias | | +150 | °C |
| $\theta_{JA}$ | Thermal Resistance | SOIC<br>TSSOP | 96<br>128 | °C/W |
| $P_D$ | Power Dissipation in Still Air at 85°C | SOIC<br>TSSOP | 500<br>450 | mW |
| MSL | Moisture Sensitivity | | Level 1 | |
| $F_R$ | Flammability Rating | Oxygen Index: 30% − 35% | UL 94 V−0 @ 0.125 in | |
| $V_{ESD}$ | ESD Withstand Voltage | Human Body Model (Note 2)<br>Machine Model (Note 3)<br>Charged Device Model (Note 4) | > 4000<br>> 300<br>> 1000 | V |
| $I_{Latchup}$ | Latchup Performance | Above $V_{CC}$ and Below GND at 85°C (Note 5) | ±300 | mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. $I_O$ absolute maximum rating must be observed.
2. Tested to EIA/JESD22−A114−A.
3. Tested to EIA/JESD22−A115−A.
4. Tested to JESD22−C101−A.
5. Tested to EIA/JESD78.

**RECOMMENDED OPERATING CONDITIONS**

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | (Referenced to GND) | 2.0 | 6.0 | V |
| $V_{IN}$, $V_{OUT}$ | DC Input Voltage, Output Voltage | (Referenced to GND) | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature Range, All Package Types | | −55 | +125 | °C |
| $t_r$, $t_f$ | Input Rise/Fall Time<br>(Figure 2) | $V_{CC}$ = 2.0 V<br>$V_{CC}$ = 4.5 V<br>$V_{CC}$ = 6.0 V | 0<br>0<br>0 | 1000<br>500<br>400 | ns |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
6. Unused inputs may not be left open. All inputs must be tied to a high−logic voltage level or a low−logic input voltage level.

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## DC CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Condition | V_CC V | Guaranteed Limit −55 to 25°C | ≤85°C | ≤125°C | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Minimum High–Level Input Voltage | $V_{OUT} = 0.1$ V $\lvert I_{OUT}\rvert \leq 20$ μA | 2.0 3.0 4.5 6.0 | 1.50 2.10 3.15 4.20 | 1.50 2.10 3.15 4.20 | 1.50 2.10 3.15 4.20 | V |
| $V_{IL}$ | Maximum Low–Level Input Voltage | $V_{OUT} = V_{CC} - 0.1$ V $\lvert I_{OUT}\rvert \leq 20$ μA | 2.0 3.0 4.5 6.0 | 0.50 0.90 1.35 1.80 | 0.50 0.90 1.35 1.80 | 0.50 0.90 1.35 1.80 | V |
| $V_{OH}$ | Minimum High–Level Output Voltage | $V_{IN} = V_{IL}$ $\lvert I_{OUT}\rvert \leq 20$ μA | 2.0 4.5 6.0 | 1.9 4.4 5.9 | 1.9 4.4 5.9 | 1.9 4.4 5.9 | V |
| | | $V_{IN} = V_{IL}$ $\lvert I_{OUT}\rvert \leq 3.6$ mA $\lvert I_{OUT}\rvert \leq 6.0$ mA $\lvert I_{OUT}\rvert \leq 7.8$ mA | 3.0 4.5 6.0 | 2.48 3.98 5.48 | 2.34 3.84 5.34 | 2.20 3.70 5.20 | |
| $V_{OL}$ | Maximum Low–Level Output Voltage | $V_{IN} = V_{IH}$ $\lvert I_{OUT}\rvert \leq 20$ μA | 2.0 4.5 6.0 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | V |
| | | $V_{IN} = V_{IH}$ $\lvert I_{OUT}\rvert \leq 3.6$ mA $\lvert I_{OUT}\rvert \leq 6.0$ mA $\lvert I_{OUT}\rvert \leq 7.8$ mA | 3.0 4.5 6.0 | 0.26 0.26 0.26 | 0.33 0.33 0.33 | 0.40 0.40 0.40 | |
| $I_{IN}$ | Maximum Input Leakage Current | $V_{IN} = V_{CC}$ or GND | 6.0 | ±0.1 | ±1.0 | ±1.0 | μA |
| $I_{OZ}$ | Maximum 3–State Leakage Current | Output in High Impedance State $V_{IN} = V_{IL}$ or $V_{IH}$ $V_{OUT} = V_{CC}$ or GND | 6.0 | ±0.5 | ±5.0 | ±10.0 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | $V_{IN} = V_{CC}$ or GND $I_{OUT} = 0$ μA | 6.0 | 4 | 40 | 160 | μA |

## AC CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

| Symbol | Parameter | V_CC V | Guaranteed Limit −55 to 25°C | ≤85°C | ≤125°C | Unit |
|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, Input A to Output Y (Figures 2 and 4) | 2.0 3.0 4.5 6.0 | 80 30 18 15 | 100 40 23 20 | 120 55 28 25 | ns |
| $t_{PLZ}$, $t_{PHZ}$ | Maximum Propagation Delay, Output Enable to Output Y (Figures 3 and 5) | 2.0 3.0 4.5 6.0 | 110 45 25 21 | 140 60 31 26 | 165 75 38 31 | ns |
| $t_{PZL}$, $t_{PZH}$ | Maximum Propagation Delay, Output Enable to Output Y (Figures 3 and 5) | 2.0 3.0 4.5 6.0 | 110 45 25 21 | 140 60 31 26 | 165 75 38 31 | ns |
| $t_{TLH}$, $t_{THL}$ | Maximum Output Transition Time, Any Output (Figures 2 and 4) | 2.0 3.0 4.5 6.0 | 60 22 12 10 | 75 28 15 13 | 90 34 18 15 | ns |
| $C_{IN}$ | Maximum Input Capacitance | | 10 | 10 | 10 | pF |
| $C_{OUT}$ | Maximum 3–State Output Capacitance (High Impedance State Output) | | 15 | 15 | 15 | pF |

| | | Typical @ 25°C, $V_{CC} = 5.0$ V, $V_{EE} = 0$ V | |
|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance (Per Buffer) (Note 7) | 35 | pF |

7. Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

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$t_r$     $t_f$

V_CC

90%

INPUT A   50%

10%

GND

$t_{PLH}$      $t_{PHL}$

90%

OUTPUT Y   50%

10%

$t_{TLH}$      $t_{THL}$
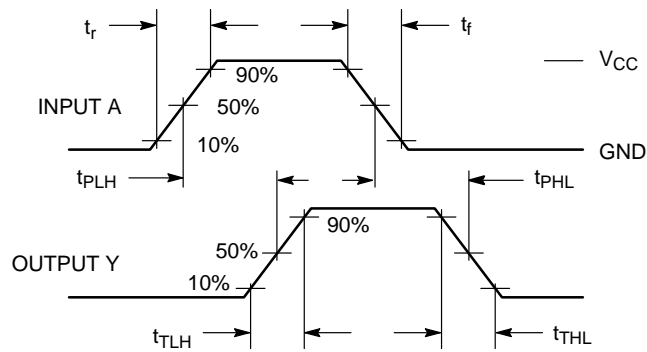
**Figure 2. Switching Waveform**

$V_{CC}$

OE1 or OE2   50%     50%

GND

$t_{PZL}$     $t_{PLZ}$

HIGH
IMPEDANCE

OUTPUT Y   50%

10%   $V_{OL}$

$t_{PZH}$     $t_{PHZ}$

90%   $V_{OH}$

OUTPUT Y   50%

HIGH
IMPEDANCE
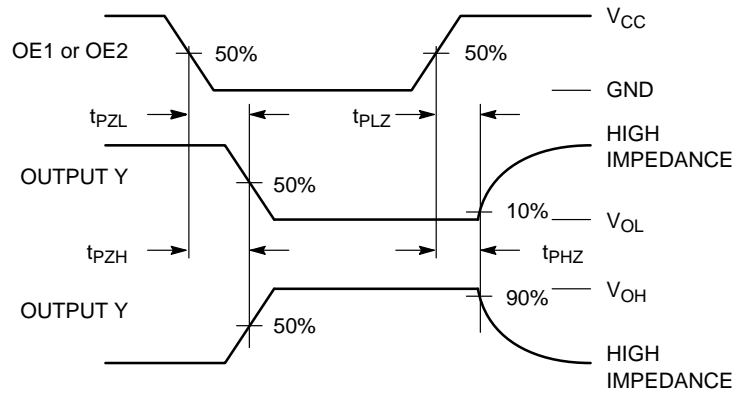
**Figure 3. Switching Waveform**

TEST
POINT

DEVICE
UNDER
TEST

OUTPUT

$C_L$*
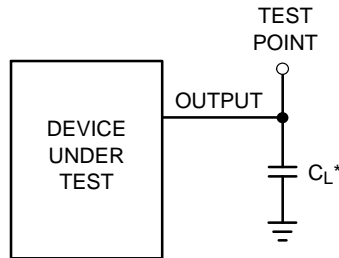
*Includes all probe and jig capacitance

**Figure 4. Test Circuit**

TEST
POINT

DEVICE
UNDER
TEST

OUTPUT   1 kΩ

CONNECT TO $V_{CC}$ WHEN
TESTING $t_{PLZ}$ AND $t_{PZL}$.
CONNECT TO GND WHEN
TESTING $t_{PHZ}$ and $t_{PZH}$.

$C_L$*
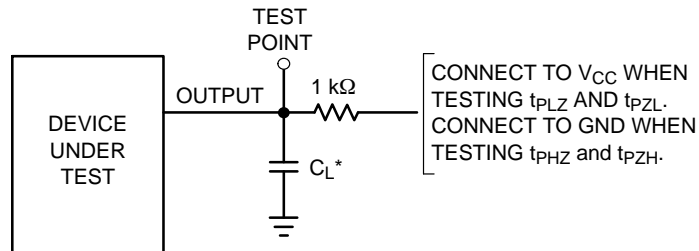
*Includes all probe and jig capacitance

**Figure 5. Test Circuit**

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## PIN DESCRIPTIONS

### INPUTS

**A1, A2, A3, A4, A5, A6, A7, A8 (PINS 2, 3, 4, 5, 6, 7, 8, 9)**

Data input pins. Data on these pins appear in non−inverted form on the corresponding Y outputs, when the outputs are enabled.

### CONTROLS

**OE1, OE2 (PINS 1, 19)**

Output enables (active−low). When a low voltage is applied to both of these pins, the outputs are enabled and the device functions as an non−inverting buffer. When a high voltage is applied to either input, the outputs assume the high impedance state.

### OUTPUTS

**Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8 (PINS 18, 17, 16, 15, 14, 13, 12, 11)**

Device outputs. Depending upon the state of the output enable pins, these outputs are either non−inverting outputs or high−impedance outputs.
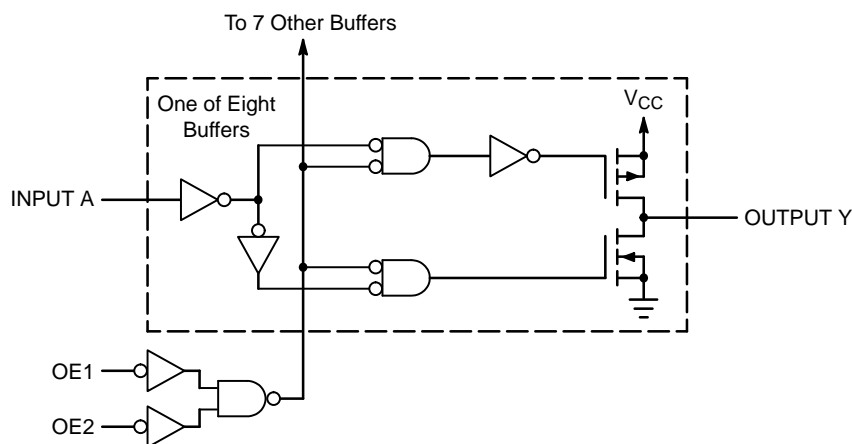


**Figure 6. Logic Detail**

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MC74HC541ADWG | SOIC−20 WIDE (Pb−Free) | 38 Units / Rail |
| MC74HC541ADWR2G | SOIC−20 WIDE (Pb−Free) | 1000 Tape & Reel |
| NLV74HC541ADWR2G* | SOIC−20 WIDE (Pb−Free) | 1000 Tape & Reel |
| MC74HC541ADTG | TSSOP−20 (Pb−Free) | 75 Units / Rail |
| MC74HC541ADTR2G | TSSOP−20 (Pb−Free) | 2500 Tape & Reel |
| NLV74HC541ADTR2G* | TSSOP−20 (Pb−Free) | 2500 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

## PACKAGE DIMENSIONS

**TSSOP−20**
**DT SUFFIX**
CASE 948E−02
ISSUE C



**SECTION N−N**

**DETAIL E**

**SEATING PLANE**
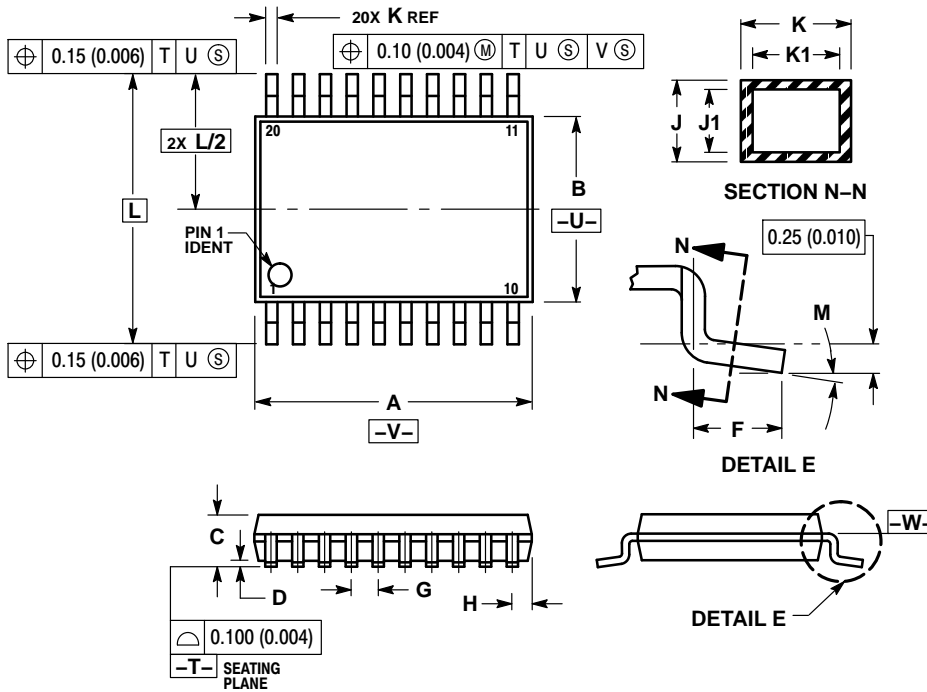
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| DIM | MILLIMETERS | | INCHES | |
| --- | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

**SOLDERING FOOTPRINT\***

7.06

0.65 PITCH

16X 0.36

16X 1.26

DIMENSIONS: MILLIMETERS
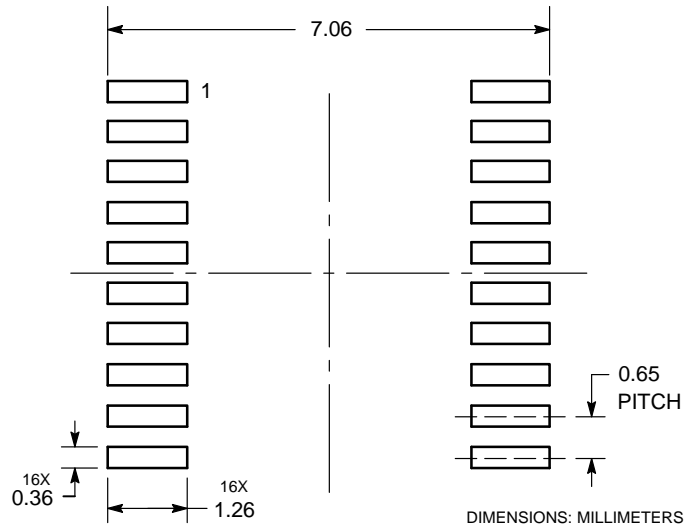
\*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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## PACKAGE DIMENSIONS

**SOIC−20**
**DW SUFFIX**
CASE 751D−05
ISSUE G
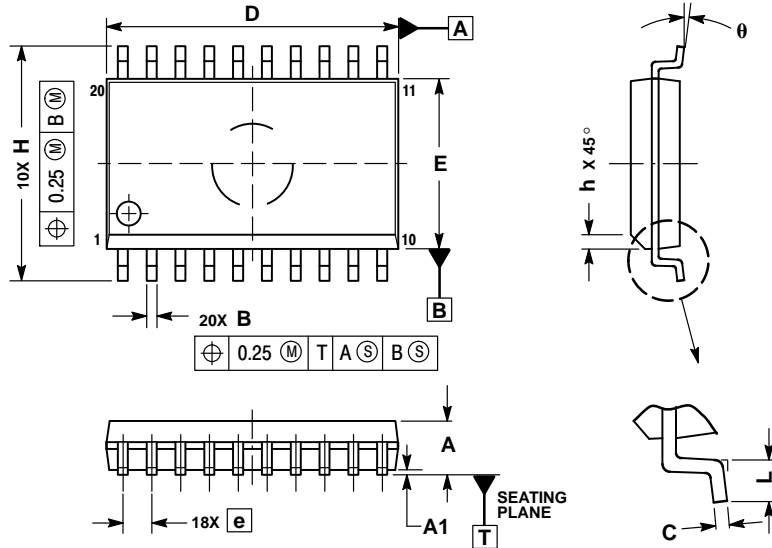
NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | |
| --- | --- | --- |
| | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0 ° | 7 ° |

**MC74HC541A/D**