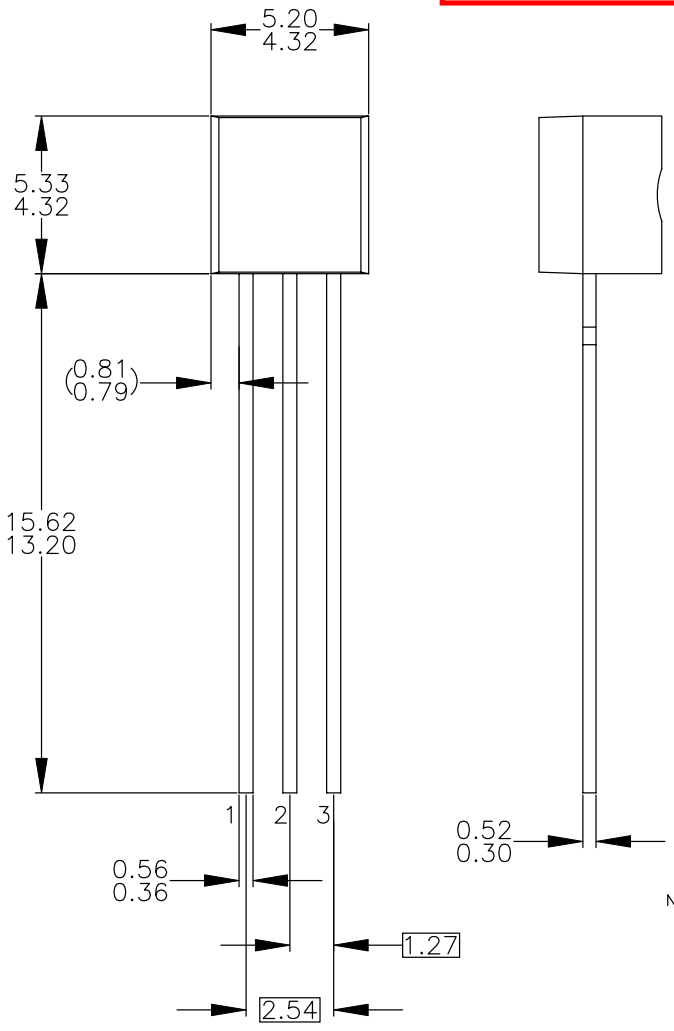
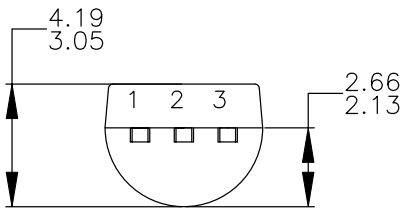
REVISIONS

| NO. | DESCRIPTION | DATE | NAME/SITE |
|---|---|---|---|
| A | RELEASE TO DOCUMENT CONTROL | MAR.4'96 | RP |
| B | RDRW AS PER STD DWG TEMPLATE. CHG DIM REF FR DUAL DIM INCH[MM] TO SINGLE DIM MM. CHG LD PITCH DIM FR 1.14–1.40 TO 1.27 BSC. ADD DIM 2.54 BSC. CHG PKG WIDTH DIM FR 4.32– 4.70 TO 4.32–4.83; CHG PKG HEIGHT DIM FR 4.32–4.70 TO 4.32–4.78; CHG LD THICK DIM FR 0.30– 0.48 TO 0.30–0.52; DAMBAR–PKG DIM FR 1.27–1.65 TO 0.90–1.65; LD LGH DIM FR 14.47–15.64 TO 14.47–15.62; PKG DIM: 1.02–1.52 TO 0.92–1.52, 3.81–4.45 TO 3.40–4.80; NOTE 2: ADD DMOS "M" OPT'N AND LEGEND; NOTE B PKG 94 JFET OPT'N: CHG D TO S, CHG S TO D. ADD NOTE C; MOVE NOTE B INFO FR PKG 97&98 TO NEW NOTE D. | 40CT1999 | RCM/MRG |
| 3 | CHG LD LEN FR $^{15.61}_{14.07}$ TO $^{15.62}_{13.20}$; CHG MOLD BODY HT FR $^{4.78}_{4.32}$ TO $^{5.33}_{4.32}$; CHG PKG EDGE TO LD EDGE DIST FR (0.81) TO $^{(0.81)}_{(0.79)}$; CHG MOLD BODY WIDTH FR $^{4.83}_{4.32}$ TO $^{5.20}_{4.32}$; ADD PKG THICKNESS DIM 'E'; CHG 's' DIM FR $^{2.41}_{2.15}$ TO $^{2.66}_{2.13}$; REMOVE DAMBAR & EJECTOR PIN LOCATOR FEATURES & DIMENSIONS; REMOVE MOLDED SURFACE & DRAFT ANGLE DIMS; ADD NOTE ON JEDEC REFERENCE; ADD NOTE ON ASME Y14.5M–1994; REMOVE NOTE ON L34Z OPTION; ADD NOTE ON DWG FILENAME. | 12FEB08 | BMR/FSCP |

**APPROVED**
July-14-2008




NOTES: UNLESS OTHERWISE SPECIFIED

A) DRAWING WITH REFERENCE TO JEDEC TO–92 RECOMMENDATIONS.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DRAWING CONFORMS TO ASME Y14.5M–1994.
D) TO–92 (92,94,96,97,98) PIN CONFIGURATION:

| PIN | 92 | | | 94 | | | 96 | | | 97 | | | 98 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | P | F | M | P | F | M | B | F | M | P | F | M | P | F | M |
| 1 | E | S | S | E | S | S | B | D | G | C | G | D | C | G | D |
| 2 | B | D | G | C | G | D | E | S | S | B | D | G | E | S | S |
| 3 | C | G | D | B | D | G | C | G | D | E | S | S | B | D | G |

LEGEND:
P – BIPOLAR
F – JFET
M – DMOS
E – EMITTER
B – BASE
C – COLLECTOR
D – DRAIN
S – SOURCE
G – GATE

E) FOR PACKAGE 92, 94, 96, 97 AND 98: PIN CONFIGURATION DRAIN "D" AND SOURCE "S" ARE INTERCHANGEAGLE AT JFET "F" OPTION.
F) DRAWING FILENAME: MKT–ZA03DREV3.

| APPROVALS | DATE |
|---|---|
| DRAWN: J.U. COMPARATIVO JR. | 03APR2008 |
| CHECKED: L. GALERA | |
| APPROVED: M.R. GESTOLE | |
| G.S. BAJE | |

PROJECTION INCH [MM]

FAIRCHILD SEMICONDUCTOR™

3LD,TO–92,MOLDED
STD STRAIGHT LD
(NO EOL CODE)

| SCALE | SIZE | DRAWING NUMBER | REV |
|---|---|---|---|
| 1:1 | N/A | MKT–ZA03D | 3 |

FORMERLY: N/A
SHEET : 1 OF 1

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Fairchild Semiconductor:

PN4416 BC327A_D26Z