LMS1485 5V Low Power RS-485 Differential Bus Transceiver

Check for Samples: LMS1485

FEATURES

- **Meet ANSI Standard RS-485-A and RS-422-B**
- **Data Rate 30Mbps**
- **Single Supply Voltage Operation, 5V**
- **Wide Input and Output Voltage Range**
- **Thermal Shutdown Protection**
- **Short Circuit Protection**
- **Driver Propagation Delay 10ns**
- **Receiver Propagation Delay 25ns**
- **High Impedance Outputs With Power Off**
- **Open Circuit Fail-Safe for Receiver**
- **Extended Operating Temperature Range −40°C to 85°C**
- **ESD Rating 8kV HBM**
- **Drop-In Replacement to ADM1485 and LT1485**
- **Available in 8-pin SOIC**
- **Low Supply Current, I_{CC} = 1mA**

APPLICATIONS

- **Low Power RS-485 Systems**
- **Network Hubs, Bridges, and Routers**
- **Point of Sales Equipment (ATM, Barcode Scanners,…)**
- **Local Area Networks (LAN)**
- **Integrated Service Digital Network (ISDN)**
- **Industrial Programmable Logic Controllers**
- **High Speed Parallel and Serial Applications**
- **Multipoint Applications with Noisy Environment**

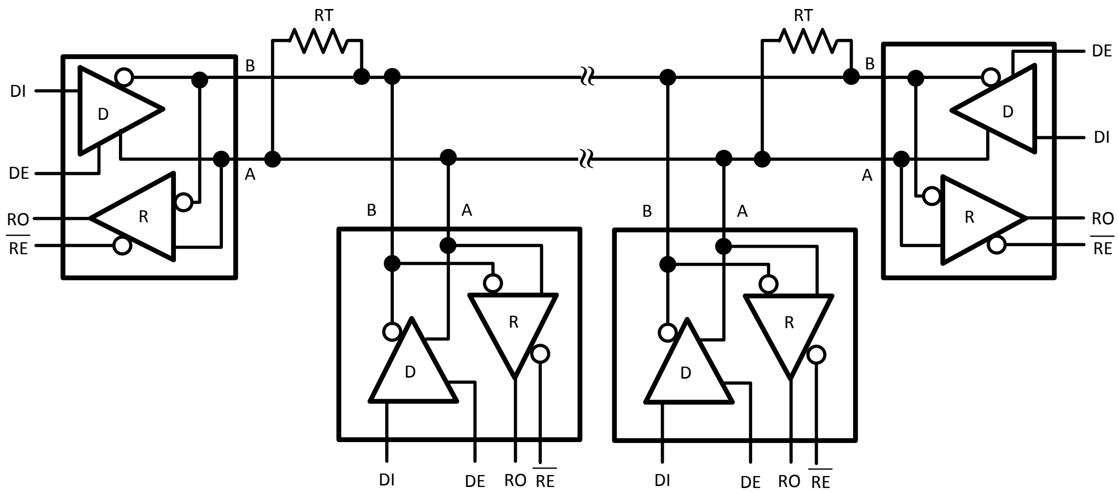
DESCRIPTION

The LMS1485 is a low power differential bus/line transceiver designed for high speed bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines. It meets ANSI Standards TIA/EIA RS422-B, TIA/EIA RS485-A and ITU recommendation and V.11 and X.27.

The LMS1485 combines a Tri-State differential line driver and differential input receiver, both of which operate from a single 5.0V power supply. The driver and receiver have an active high and active low, respectively, that can be externally connected to function as a direction control. The driver and receiver differential inputs are internally connected to form differential input/output (I/O) bus ports that are designed to offer minimum loading to bus whenever the driver is disabled or when V_{CC} = 0V. These ports feature wide positive and negative common mode voltage ranges, making the device suitable for multipoint applications in noisy environments.

The LMS1485 is build with Texas Instruments' advanced BiCMOS process and is available in a 8-Pin SOIC package. It is a drop-in socket replacement to ADI's ADM1485 and LTC's LT1485.

Typical Application



A typical multipoint application is shown in the above figure. Terminating resistors, RT, are typically required but only located at the two ends of the cable. Pull up and pull down resistors maybe required at the end of the bus to provide failsafe biasing. The biasing resistors provide a bias to the cable when all drivers are in Tri-State, See Texas Instruments Application Note, AN-847 (SNLA031) for further information.

Connection Diagram

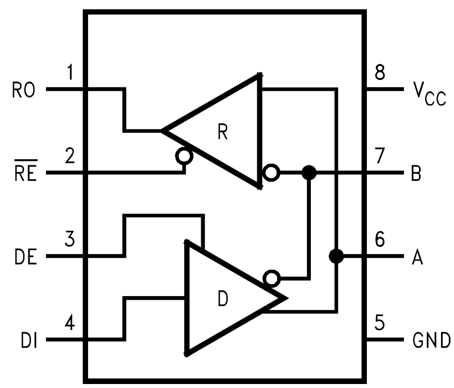


Figure 1. 8-Pin SOIC (Top View)

PIN DESCRIPTIONS

Pin #	I/O	Name	Function
1	O	RO	Receiver Output: If A > B by 200 mV, RO will be high; If A < B by 200mV, RO will be low. RO will be high also if the inputs (A and B) are open (non-terminated)
2	I	$\overline{RE}$	Receiver Output Enable: RO is enabled when $\overline{RE}$ is low; RO is in TRI-STATE when $\overline{RE}$ is high
3	I	DE	Driver Output Enable: The driver outputs (A and B) are enabled when DE is high; they are in Tri-State when DE is low. Pins A and B also function as the receiver input pins (see below)
4	I	DI	Driver Input: A low on DI forces A low and B high while a high on DI forces A high and B low when the driver is enabled
5	N/A	GND	Ground
6	I/O	A	Non-inverting Driver Output and Receiver Input pin. Driver Output levels conform to RS-485 signaling levels
7	I/O	B	Inverting Driver Output and Receiver Input pin. Driver Output levels conform to RS-485 signaling levels
8	N/A	V_{CC}	Power Supply: 4.75V ≤ V_{CC} ≤ 5.25V

TRUTH TABLE (1)

DRIVER SECTION				
$\overline{RE}$	**DE**	**DI**	**A**	**B**
X	H	H	H	L
X	H	L	L	H
X	L	X	Z	Z
RECEIVER SECTION				
$\overline{RE}$	**DE**	**A-B**		**RO**
L	L	≥ +0.2V		H
L	L	≤ −0.2V		L
H	X	X		Z
L	L	OPEN *		H

(1) * = Non Terminated, Open Input only
X = Irrelevant
Z = Tri-State
H = High level
L = Low level

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS [1][2]

Supply Voltage, V_{CC} [3]		7V
Input Voltage, V_{IN} (DI, DE, or $\overline{RE}$)		−0.3V to V_{CC}+ 0.3V
Voltage Range at Any Bus Terminal (AB)		−7V to 12V
Receiver Outputs		−0.3V to V_{CC} + 0.3V
Package Thermal Impedance, θ_{JA}	SOIC [4]	125°C/W
Junction Temperature [4]		150°C
Operating Free-Air Temperature Range, T_A	Commercial	0°C to 70°C
	Industrial	−40°C to 85°C
Storage Temperature Range		−65°C to 150°C
ESD Rating [5] [6]		8kV
ESD Rating [5] [7]		2kV
Soldering Information	Infrared or Convection (20 sec.)	235°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the ELECTRICAL CHARACTERISTICS section.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.
(5) ESD rating based upon human body model, 100pF discharged through 1.5kΩ.
(6) ESD rating applies to pins 6 and 7
(7) ESD rating applies to pins 1, 2, 3, 4, 5 and 8

OPERATING RATINGS

	Min	Nom	Max	
Supply Voltage, V_{CC}	4.75	5.0	5.25	V
Voltage at any Bus Terminal (Separately or Common Mode), V_{IN} or V_{IC}	−7		12	V
High-Level Input Voltage, V_{IH} [1]	2			V
Low-Level Input Voltage, V_{IL} [1]			0.8	V
Differential Input Voltage, V_{ID} [2]			±12	V

(1) Voltage limits apply to DI, DE, $\overline{RE}$ pins.
(2) Differential input/output bus voltage is measured at the non-inverting terminal A with respect to the inverting terminal B.

ELECTRICAL CHARACTERISTICS

Over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Driver Section						
V_{OD}	Differential Output Voltage	R = ∞ (Figure 13)			5	V
V_{OD1}	Differential Output Voltage	R = 50Ω (Figure 13), RS-422	2		5	V
V_{OD2}	Differential Output Voltage	R = 27Ω (Figure 13), RS-485	1.5		5	V
V_{OD3}	Differential Output Voltage	V_{TEST} = −7V to + 12V (Figure 14)	1.5		5	V
ΔV_{OD}	Change in Magnitude of Differential Output Voltage	R = 27Ω or 50Ω (Figure 13), See [1]	−0.2		0.2	V
V_{OC}	Common-Mode Output Voltage	R = 27Ω or 50Ω (Figure 13), See [1]			3	V
ΔV_{OC}	Change in Magnitude of Common-Mode Output Voltage	R = 27Ω or 50Ω (Figure 13), See [1]	−0.2		0.2	V
I_{OSD}	Short-Circuit Output Current	V_O = High, −7V≤V_{CM} ≤+12V	−250		250	mA
		V_O = Low, −7V ≤V_{CM} ≤+12V	−250		250	
V_{INL}	CMOS Input Logic Threshold Low	DE, DI, $\overline{RE}$			0.8	V

(1) $|\Delta V_{OD}|$ and $|\Delta V_{OC}|$ are changes in magnitude of V_{OD} and V_{OC}, respectively when the input changes from high to low levels.

ELECTRICAL CHARACTERISTICS (continued)

Over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{INH}	CMOS Input Logic Threshold High	DE, DI, $\overline{RE}$	2			V
I_{IN}	Logic Input Current	DE, DI	−1		1	μA
Receiver Section						
V_{TH}	Differential Input Threshold Voltage	$-7V \le V_{CM} \le +12V$	−0.2		+0.2	V
ΔV_{TH}	Input Hysteresis Voltage ($V_{TH+} - V_{TH-}$)	$V_{CM} = 0$		70		mV
R_{IN}	Input Resistance	$-7V \le V_{CM} \le +12V$	12			kΩ
I_{IN}	Input Current (A, B)	$V_{IN} = 12V$			1	mA
		$V_{IN} = -7V$	−0.8			
I_{RE}	Logic Enable Input Current	$\overline{RE}$	−1		1	μA
V_{OL}	CMOS Low-Level Output Voltage	$I_{OL} = 4mA$			0.4	V
V_{OH}	CMOS High-Level Output Voltage	$I_{OH} = -4mA$	4			V
I_{OSR}	Short-Circuit Output Current	V_O = GND or V_{CC}	7		85	mA
I_{OZ}	Tristate Output Leakage Current	$0.4V \le V_O \le +2.4V$	−1		1	μA
Power Supply Current						
I_{CC}	Supply Current	Driver Enabled, Output = No Load, Digital Inputs = GND or V_{CC}		1.1	2.2	mA
		Driver Disabled, Output = No Load, Digital Inputs = GND or V_{CC}		1	2.2	mA
Switching Characteristics						
Driver						
T_{PLH}, T_{PHL}	Propagation Delay Input to Output	$R_L = 54\Omega$, $C_L = 100pF$ (Figure 15, Figure 19)		11	20	ns
T_{SKEW}	Driver Output Skew	$R_L = 54\Omega$, $C_L = 100pF$ (Figure 15, Figure 19)		1		ns
T_R, T_F	Driver Rise and Fall Time	$R_L = 100\Omega$, $C_L = 100pF$ (Figure 15, Figure 19)		5	10	ns
T_{ENABLE}	Driver Enable to Ouput Valid Time	(Figure 16, Figure 20)		18	32	ns
$T_{DISABLE}$	Output Disable Time	(Figure 16, Figure 20)		20	40	ns
Receiver						
T_{PLH}, T_{PHL}	Propagation Delay Input to Output	$C_L = 15pF$ (Figure 17, Figure 19)	18	33	55	ns
T_{SKEW}	Receiver Output Skew	(Figure 17, Figure 19)		2		ns
T_{ENABLE}	Receiver Enable Time	(Figure 18, Figure 22)		6	25	ns
$T_{DISABLE}$	Receiver Disable Time	(Figure 18, Figure 22)		15	25	ns

TYPICAL PERFORMANCE CHARACTERISTICS

Receiver Output Low Voltage vs. Output Current

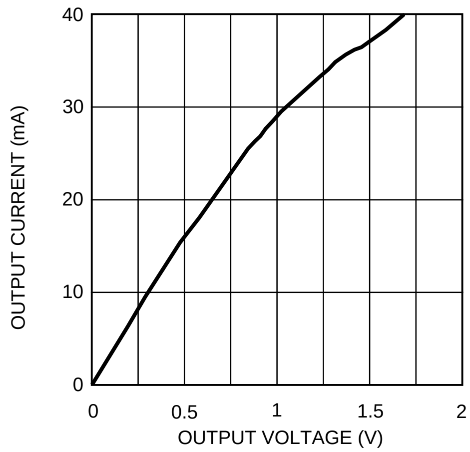


Figure 2.

Receiver Output High Voltage vs. Output Current

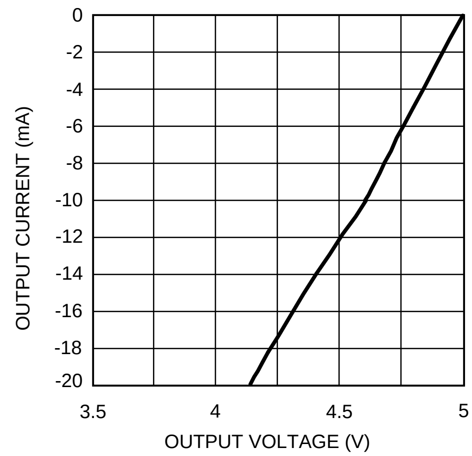


Figure 3.

Receiver Output High Voltage vs. Temperature

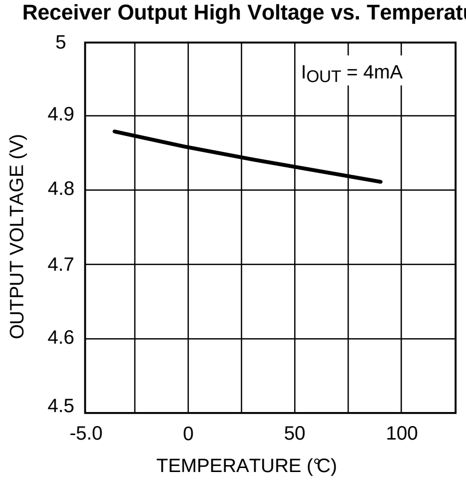


Figure 4.

Receiver Output Low Voltage vs. Temperature

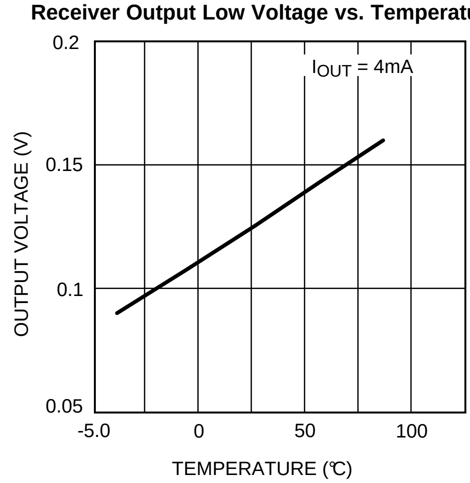


Figure 5.

Driver Differential Output Voltage vs. Output Current

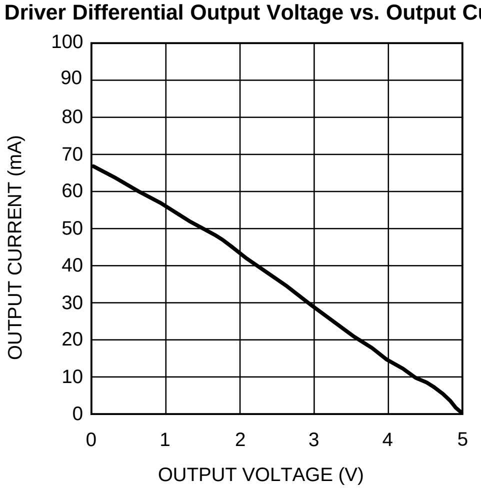


Figure 6.

Driver Differential Output Voltage vs. Temperature R_L = 54Ω

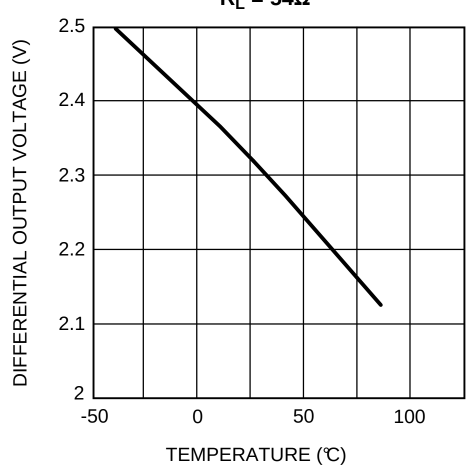


Figure 7.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Driver Output Low Voltage vs. Output Current

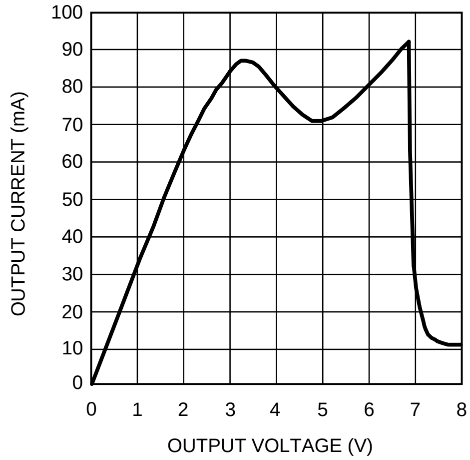


Figure 8.

Driver Output High Voltage vs. Output Current

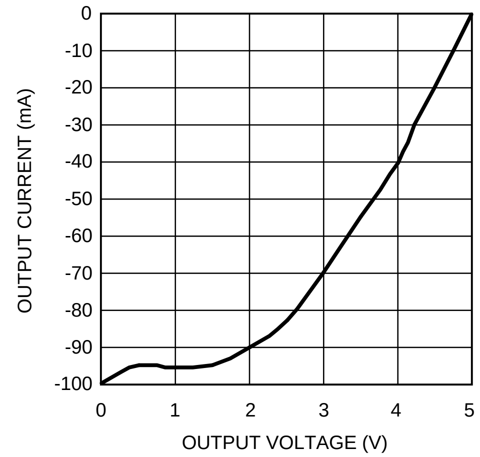


Figure 9.

Supply Current vs. Temperature

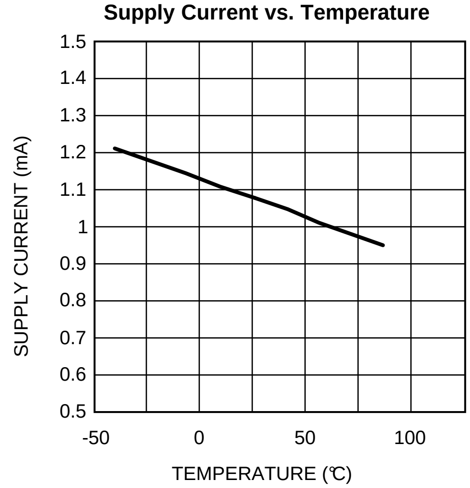


Figure 10.

Receiver Skew vs. Temperature

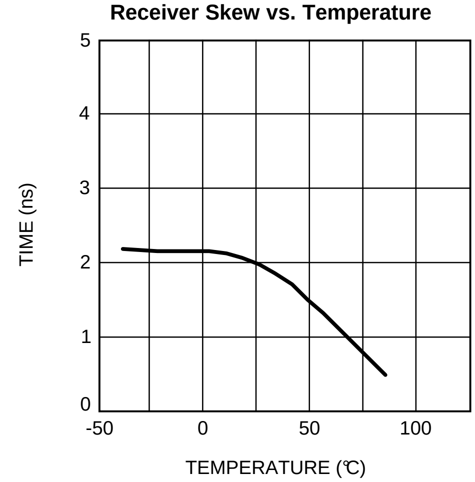


Figure 11.

Driver Skew vs. Temperature

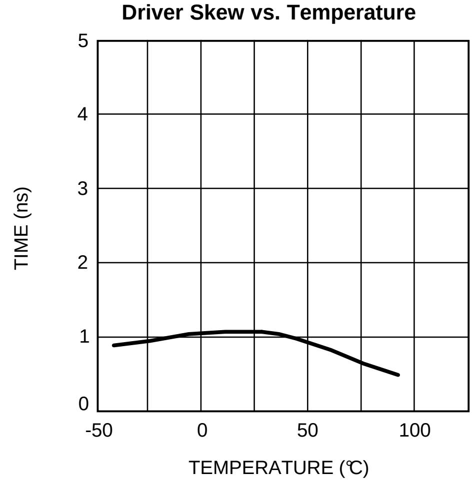


Figure 12.

PARAMETER MEASURING INFORMATION

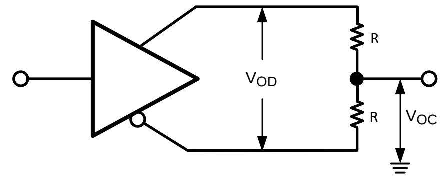


Figure 13. Test Circuit for V_{OD} and V_{OC}

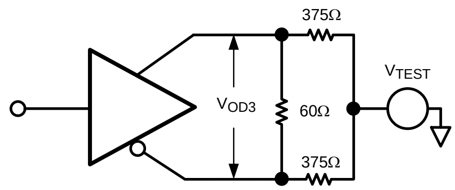


Figure 14. Test Circuit for V_{OD3}

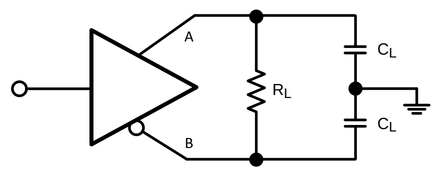


Figure 15. Test Circuit for Driver Propagation Delay

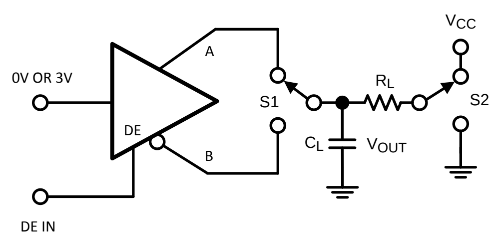


Figure 16. Test Circuit for Driver Enable / Disable

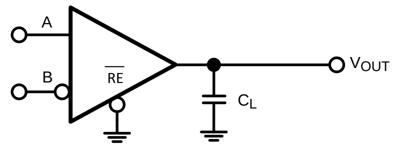


Figure 17. Test Circuit for Receiver Propagation Delay

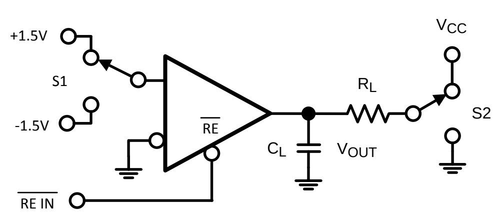


Figure 18. Test Circuit for Receiver Enable / Disable

SWITCHING CHARACTERISTICS

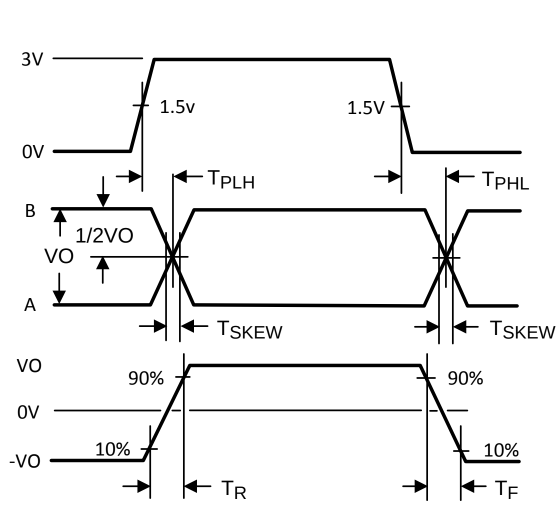


Figure 19. Driver Propagation Delay, Rise / Fall Time

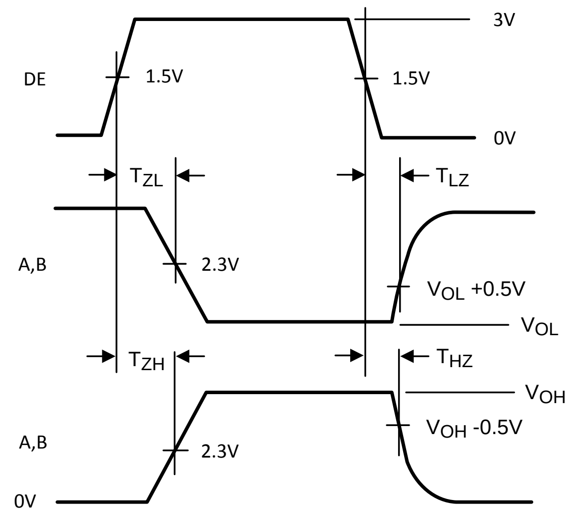


Figure 20. Driver Enable / Disable Time

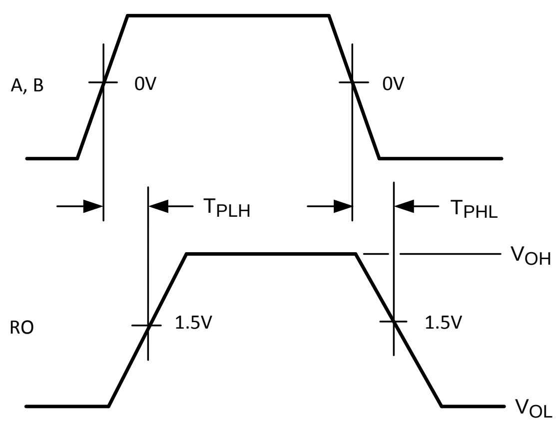


Figure 21. Receiver Propagation Delay

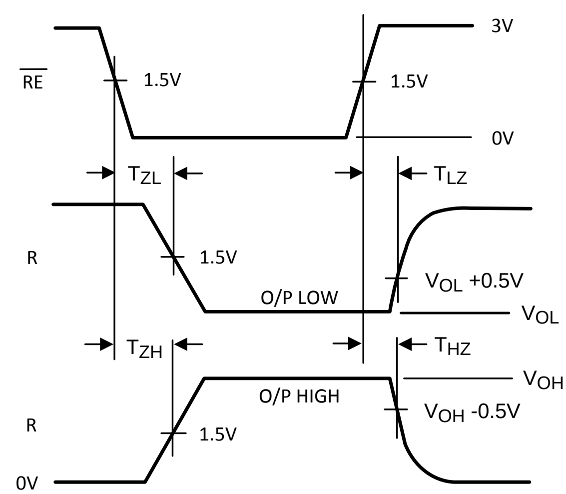


Figure 22. Receiver Enable / Disable Time

APPLICATION INFORMATION

Power Line Noise Filtering

A factor to consider in designing power and ground is noise filtering. A noise filtering circuit is designed to prevent noise generated by the integrated circuit (IC) as well as noise entering the IC from other devices. A common filtering method is to place by-pass capacitors (C_{bp}) between the power and ground lines.

Placing a by-pass capacitor (C_{bp}) with the correct value at the proper location solves many power supply noise problems. Choosing the correct capacitor value is based upon the desired noise filtering range. Since capacitors are not ideal, they may act more like inductors or resistors over a specific frequency range. Thus, many times two by-pass capacitors may be used to filter a wider bandwidth of noise. It is highly recommended to place a larger capacitor, such as 10µF, between the power supply pin and ground to filter out low frequencies and a 0.1µF to filter out high frequencies.

By pass-capacitors must be mounted as close as possible to the IC to be effective. Long leads produce higher impedance at higher frequencies due to stray inductance. Thus, this will reduce the by-pass capacitor's effectiveness. Surface mounted chip capacitors are the best solution because they have lower inductance.

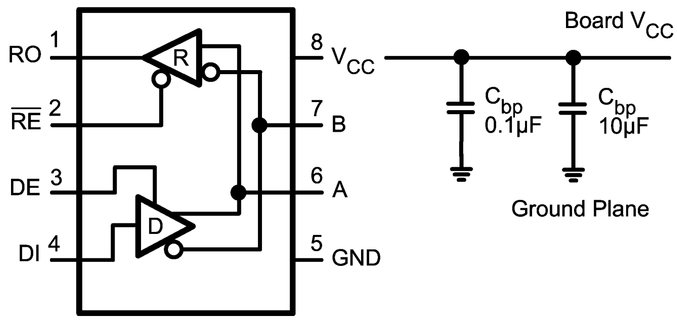


Figure 23. Placement of by-pass Capacitors, C_{bp}

REVISION HISTORY

Changes from Revision E (April 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	10