19-4759; Rev 1; 1/99

EVALUATION KIT MANUAL FOLLOWS DATA SHEET

MAXIM

1-Cell to 3-Cell, High-Power (1A), Low-Noise, Step-Up DC-DC Converters

General Description

The MAX1700/MAX1701 are high-efficiency, low-noise, step-up DC-DC converters intended for use in battery-powered wireless applications. They use a synchronous-rectified pulse-width-modulation (PWM) boost topology to generate 2.5V to 5.5V outputs from battery inputs such as one to three NiCd/NiMH cells or one Li-Ion cell. Both devices have an internal 1A, 130mΩ N-channel MOSFET switch and a 250mΩ P-channel synchronous rectifier.

With their internal synchronous rectifier, the MAX1700/MAX1701 deliver 5% better efficiency than similar non-synchronous converters. They also feature a pulse-frequency-modulation (PFM) standby mode to improve efficiency at light loads, and a 3µA shutdown mode.

The MAX1700/MAX1701 come in 16-pin QSOP packages (which occupy the same space as an 8-pin SO). The MAX1701 includes two comparators to generate power-good and low-battery warning outputs. It also contains a gain block that can be used to build a linear regulator using an external P-channel pass device.

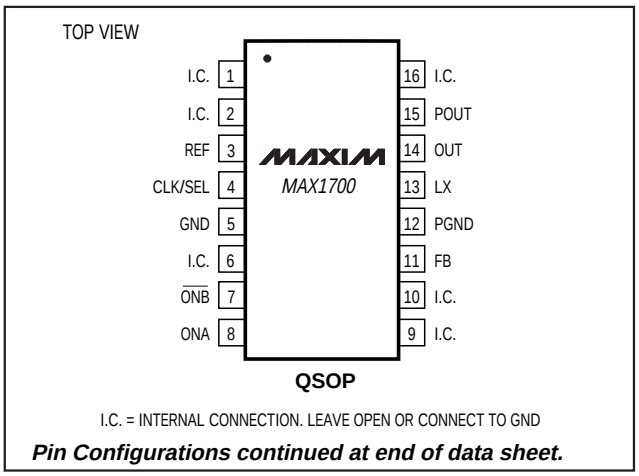
For higher-power outputs, refer to the MAX1703. For dual outputs (step-up and linear regulator), refer to the MAX1705/MAX1706. For an on-board analog-to-digital converter, refer to the MAX848/MAX849.

The MAX1701 evaluation kit is available to speed design time.

Applications

Digital Cordless Phones
PCS Phones
Wireless Handsets
Two-Way Pagers
Personal Communicators
Palmtop Computers
Hand-Held Instruments

Pin Configurations



QSOP

I.C. = INTERNAL CONNECTION. LEAVE OPEN OR CONNECT TO GND

Pin Configurations continued at end of data sheet.

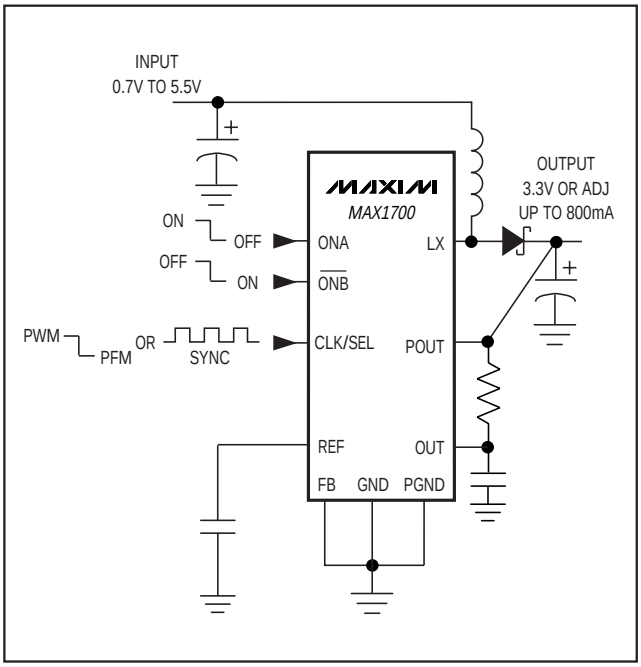
Features

- **Up to 96% Efficiency**
- **1.1 V_{IN} Guaranteed Start-Up**
- **0.7V to 5.5V Input Range**
- **Up to 800mA Output**
- **Step-Up Output (adjustable from 2.5V to 5.5V)**
- **PWM/PFM Synchronous-Rectified Topology**
- **External Clock or Internal 300kHz Oscillator**
- **3µA Logic-Controlled Shutdown**
- **Power-Good Output (MAX1701)**
- **Low-Battery Comparator (MAX1701)**
- **Uncommitted Gain Block (MAX1701)**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1700EEE	-40°C to +85°C	16 QSOP
MAX1701EEE	-40°C to +85°C	16 QSOP

Typical Operating Circuit



1-Cell to 3-Cell, High-Power (1A), Low-Noise, Step-Up DC-DC Converters

ABSOLUTE MAXIMUM RATINGS

ONA, $\overline{ONB}$, OUT, AO, POK, LBO to GND .....-0.3V, +6V
PGND to GND .....±0.3V
LX to PGND .....-0.3V,V_{POUT}+0.3V
CLK/SEL, AIN, REF, FB, LBP, LBN, POUT to GND .....-0.3V, V_{OUT}+0.3V .....
Continuous Power Dissipation (T_A=+70°C)
16-QSOP (Derate 8.30mW/°C above +70°C) 667mW

Operating Temperature Ranges
MAX1700EEE, MAX1701EEE .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(CLK/SEL = ONA = $\overline{ONB}$ = FB = PGND = GND, OUT = POUT, V_{OUT} = 3.6V (Note 6); MAX1701: AIN = LBN = GND, LBP = REF, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC-DC CONVERTER						
Input Voltage Range (Note 1)				0.7	5.5	V
Minimum Start-Up Voltage (Note 2)	I_{LOAD} < 1mA, T_A = +25°C			0.9	1.1	V
Frequency in Start-Up Mode	V_{OUT} = 1.5V		40	150	300	kHz
Output Voltage (Note 3)	V_{FB} < 0.1V, CLK/SEL = OUT, V_{BATT} = 2.4V, includes load regulation error for 0A ≤ I_{LX} ≤ 0.55A		3.17	3.30	3.38	V
FB Regulation Voltage	Adjustable output, CLK/SEL = OUT, V_{BATT} = 2.4V, includes load regulation error for 0A ≤ I_{LX} ≤ 0.55A		1.210	1.24	1.255	V
FB Input Current	V_{FB} = 1.25V			0.01	20	nA
Output Voltage Adjust Range			2.5		5.5	V
Output Voltage Lockout Threshold	(Note 4)		2.0	2.15	2.3	V
Load Regulation (Note 5)	CLK/SEL = OUT, No load to full load			-1.6		%
Supply Current in Shutdown	$V_{\overline{ONB}}$ = 3.6V	MAX1700		0.1	20	µA
		MAX1701		3	20	
Supply Current in Low-Power Mode (Note 6)	CLK/SEL = GND (MAX1700)			35	70	µA
	CLK/SEL = GND (MAX1701)			55	110	
Supply Current in Low-Noise Mode (Note 6)	CLK/SEL = OUT (MAX1700)			125	250	µA
	CLK/SEL = OUT (MAX1701)			140	300	
DC-DC SWITCHES						
POUT Leakage Current	V_{LX} = 0V, V_{OUT} = 5.5V			0.1	20	µA
LX Leakage Current	V_{LX} = $V_{\overline{ONB}}$ = V_{OUT} = 5.5V			0.1	20	µA
Switch On-Resistance	N-channel	CLK/SEL = GND		0.2	0.45	Ω
		CLK/SEL = OUT		0.13	0.28	
	P-channel			0.25	0.5	
N-Channel Current Limit	CLK/SEL = OUT		1100	1300	1600	mA
	CLK/SEL = GND		250	400	550	
P-Channel Turn-Off Current	CLK/SEL = GND		20		120	mA

ELECTRICAL CHARACTERISTICS (continued)

(CLK/SEL = ONA = $\overline{ONB}$ = FB = PGND = GND, OUT = POUT, V_{OUT} = 3.6V (Note 6); MAX1701: AIN = LBN = GND, LBP = REF, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GAIN BLOCK (MAX1701)					
AIN Reference Voltage	I_{AO} = 20µA	1.237	1.25	1.263	V
AIN Input Current	V_{AIN} = 1.5V	-30		30	nA
Transconductance	10µA < I_{AO} = 100µA	5	9	16	mmho
AO Output Low Voltage	V_{AIN} = 0.7V, I_{AO} = 100µA		0.1	0.4	V
AO Output High Leakage	V_{AIN} = 1.5V, V_{AO} = 5.5V		0.01	1	µA
POWER GOOD (MAX1701)					
Internal Trip Level	Rising V_{OUT}, V_{FB} < 0.1V	2.93	2.97	3.02	V
External Trip Level	Rising V_{FB}	1.1	1.12	1.14	V
POK Low Voltage	I_{SINK} = 1mA, V_{OUT} = 3.6V or I_{SINK} = 20µA, V_{OUT} = 1V		0.03	0.4	V
POK High Leakage Current	V_{OUT} = V_{POK} = 5.5V		0.01	1	µA
LOW-BATTERY COMPARATOR					
LBN, LBP Input Offset	LBP falling, 15mV hysteresis	-5	±0.5	5	mV
LBN, LBP Common Mode Range	To maintain input offset < ±5mV (at least one input must be within this range)	0.5		1.5	V
LBO Output Low Voltage	I_{SINK} = 1mA, V_{OUT} = 3.6V or I_{SINK} = 20µA, V_{OUT} = 1V		0.03	0.4	V
LBO High Leakage	V_{OUT} = V_{LBO} = 5V		0.01	1	µA
LBN, LBP Input Current	V_{LBP} = V_{LBN} = 1.5V			20	nA
REFERENCE					
Reference Output Voltage	I_{REF} = 0	1.237	1.250	1.263	V
REF Load Regulation	-1µA < I_{REF} < 50µA		5	15	mV
REF Supply Rejection	2.5V < V_{OUT} < 5V		0.2	5	mV
LOGIC AND CONTROL INPUTS					
Input Low Voltage (Note 7)	1.2V < V_{OUT} < 5.5V, ONA and $\overline{ONB}$			0.2V_{OUT}	V
	2.5V < V_{OUT} < 5.5V, CLK/SEL			0.2V_{OUT}	
Input High Voltage (Note 7)	1.2V < V_{OUT} < 5.5V, ONA and $\overline{ONB}$	0.8V_{OUT}			V
	2.5V < V_{OUT} < 5.5V, CLK/SEL	0.8V_{OUT}			
Logic Input Current	ONA, $\overline{ONB}$, and CLK/SEL	-1		1	µA
Internal Oscillator Frequency	CLK/SEL = OUT	260	300	340	kHz
Oscillator Maximum Duty Cycle		80	86	90	%
External Clock Frequency Range		200		400	kHz
Minimum CLK/SEL Pulse Width			200		ns
Maximum CLK/SEL Rise/Fall Time			100		ns

ELECTRICAL CHARACTERISTICS (continued)

(CLK/SEL = ONA = $\overline{ONB}$ = FB = PGND = GND, OUT = POUT, V_{OUT} = 3.6V (Note 6); MAX1701: AIN = LBN = GND, LBP = REF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 8)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC-DC CONVERTER						
Output Voltage (Note 3)	V_{FB} < 0.1V, CLK/SEL = OUT, V_{BATT} = 2.4V, includes load regulation error for 0A ≤ I_{LX} ≤ 0.55A		3.17		3.38	V
FB Regulation Voltage	Adjustable output, CLK/SEL = OUT, V_{BATT} = 2.4V, includes load regulation error for 0A ≤ I_{LX} ≤ 0.55A		1.20		1.27	V
Output Voltage Lockout Threshold	(Note 4)		2.0		2.3	V
Supply Current in Shutdown	$V_{\overline{ONB}}$ = 3.6V				20	µA
Supply Current in Low-Power Mode (Note 6)	CLK/SEL = GND (MAX1700)				70	µA
	CLK/SEL = GND (MAX1701)				110	
Supply Current in Low-Noise Mode (Note 6)	CLK/SEL = OUT (MAX1700)				250	µA
	CLK/SEL = OUT (MAX1701)				300	
DC-DC SWITCHES						
Switch On-Resistance	N-channel	CLK/SEL = GND			0.45	Ω
		CLK/SEL = OUT			0.28	
	P-channel				0.5	
N-Channel Current Limit	CLK/SEL = OUT		1100		1800	mA
	CLK/SEL = GND		250		600	
GAIN BLOCK (MAX1701)						
AIN Reference Voltage	I_{AO} = 20µA		1.23		1.27	V
Transconductance	10µA < I_{AO} < 100µA		5		16	mmho
POWER-GOOD (MAX1701)						
Internal Trip Level	Rising V_{OUT}, V_{FB} < 0.1V		2.92		3.03	V
External Trip Level	Rising V_{FB}		1.1		1.14	V
LOW-BATTERY COMPARATOR (MAX1701)						
LBN, LBP Input Offset	LBP falling, 15mV hysteresis		-5		5	mV
LBN, LBP Common Mode Range	To maintain input offset < ±5mV (at least one input must be within this range)		0.5		1.5	V
REFERENCE						
Reference Output Voltage	I_{REF} = 0		1.23		1.27	V

ELECTRICAL CHARACTERISTICS (continued)

(CLK/SEL = ONA = $\overline{ONB}$ = FB = PGND = GND, OUT = POUT, V_{OUT} = 3.6V, MAX1701: AIN = LBN = GND, LBP = REF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 8)

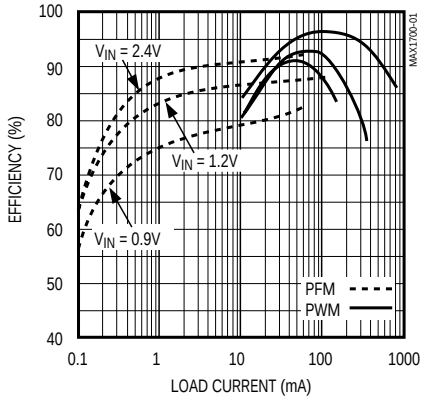
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC AND CONTROL INPUTS					
Input Low Voltage (Note 7)	1.2V < V_{OUT} < 5.5V, ONA and $\overline{ONB}$			0.2V_{OUT}	V
	2.5V < V_{OUT} < 5.5V, CLK/SEL			0.2V_{OUT}	
Input High Voltage (Note 7)	1.2V < V_{OUT} < 5.5V, ONA and $\overline{ONB}$	0.8V_{OUT}			V
	2.5V < V_{OUT} < 5.5V, CLK/SEL	0.8V_{OUT}			
Logic Input Current	ONA, $\overline{ONB}$, and CLK/SEL	-1		1	µA
Internal Oscillator Frequency	CLK/SEL = OUT	260		340	kHz
Oscillator Maximum Duty Cycle		80		92	%
External Clock Frequency Range		200		400	kHz

Note 1: Operating voltage. Since the regulator is bootstrapped to the output, once started it will operate down to 0.7V input.
Note 2: Start-up is tested with the circuit of Figure 2.
Note 3: In low-power mode (CLK/SEL = GND), the output voltage regulates 1% higher than low-noise mode (CLK/SEL = OUT or synchronized).
Note 4: The regulator is in start-up mode until this voltage is reached. Do not apply full load current.
Note 5: Load regulation is measured from no-load to full load where full load is determined by the N-channel switch current limit.
Note 6: Supply current from the 3.30V output is measured between the 3.30V output and the OUT pin. This current correlates directly to the actual battery supply current, but is reduced in value according to the step-up ratio and efficiency. Set V_{OUT} = 3.6V to keep the internal switch open when measuring the current into the device.
Note 7: ONA and $\overline{ONB}$ have hysteresis of approximately 0.15xV_{OUT}.
Note 8: Specifications to -40°C are guaranteed by design and not production tested.

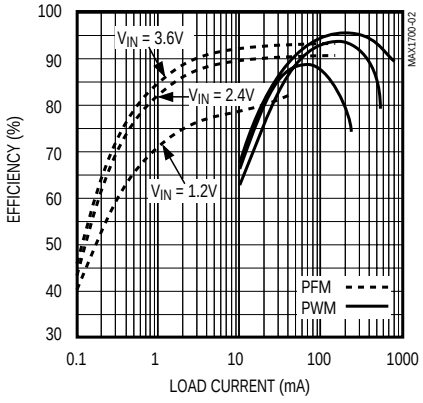
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

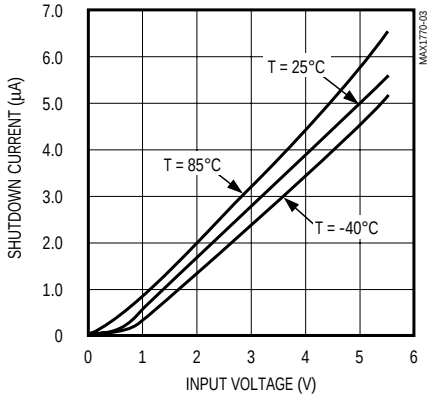
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 3.3V)



EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 5V)



MAX1701 SHUTDOWN CURRENT vs. INPUT VOLTAGE (V)

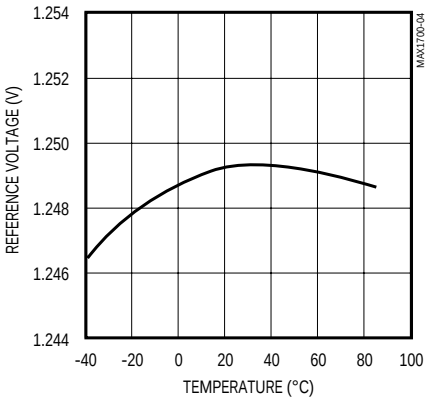


1-Cell to 3-Cell, High-Power (1A), Low-Noise, Step-Up DC-DC Converters

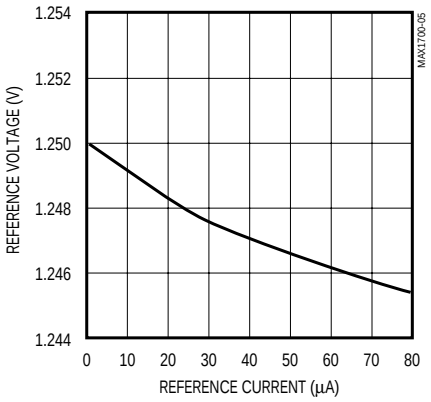
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

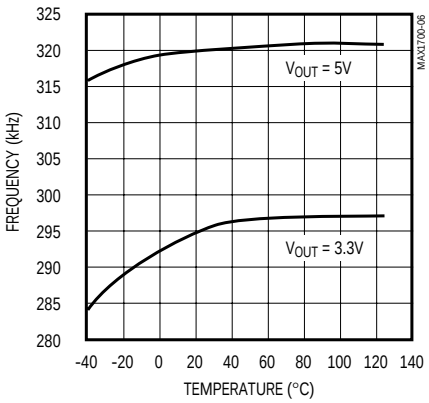
REFERENCE VOLTAGE vs. TEMPERATURE



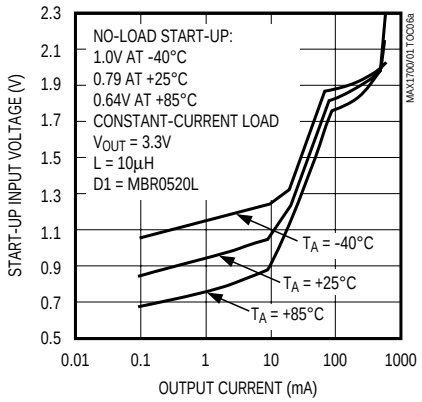
REFERENCE VOLTAGE vs. REFERENCE CURRENT



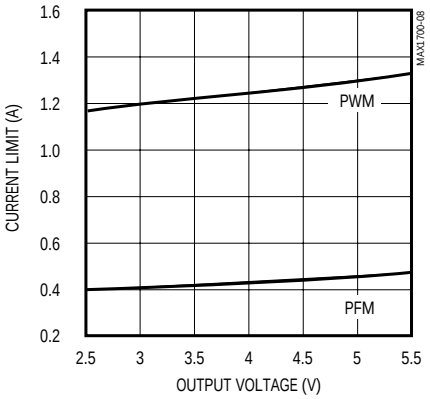
FREQUENCY vs. TEMPERATURE



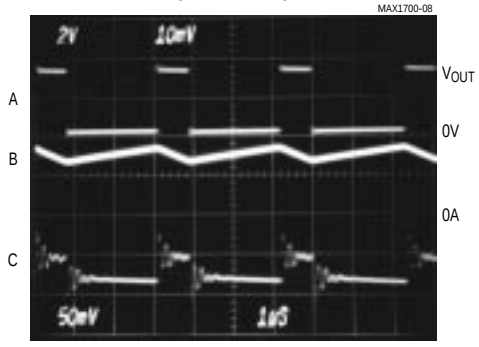
START-UP INPUT VOLTAGE vs. OUTPUT CURRENT



PEAK INDUCTOR CURRENT vs. OUTPUT VOLTAGE



HEAVY-LOAD SWITCHING WAVEFORMS (V_{OUT} = 3.3V)



1µs/div

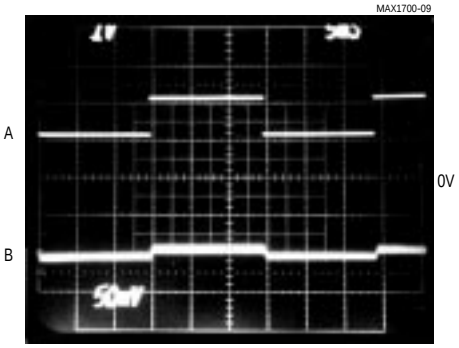
V_{IN} = 1.1V, I_{OUT} = 200mA, V_{OUT} = 3.3V

A = LX VOLTAGE, 2V/div

B = INDUCTOR CURRENT, 0.5A/div

C = V_{OUT} RIPPLE, 50mV/div, AC COUPLED

LINE-TRANSIENT RESPONSE



5ms/div

I_{OUT} = 0mA, V_{OUT} = 3.3V

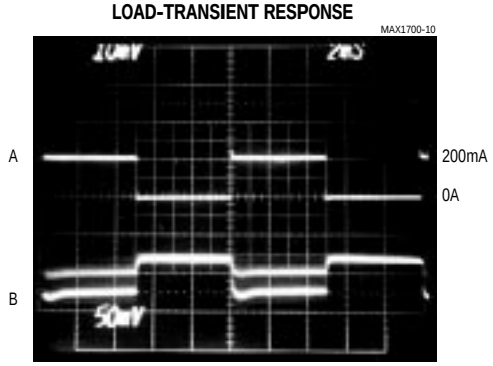
A = V_{IN}, 1.1V TO 2.1V, 1V/div

B = V_{OUT} RIPPLE, 50mV/div, AC COUPLED

Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

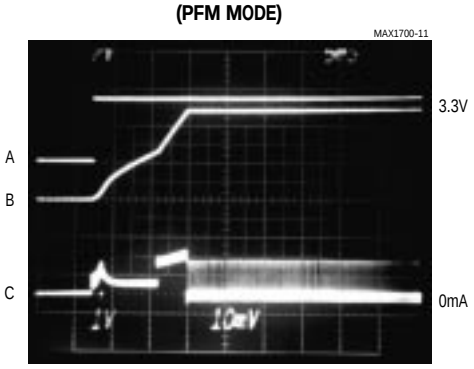
LOAD-TRANSIENT RESPONSE



2ms/div

V_{IN} = 1.1V, V_{OUT} = 3.3V
A = LOAD CURRENT, 0mA TO 200mA, 0.2A/div
B = V_{OUT} RIPPLE, 50mV/div, AC COUPLED

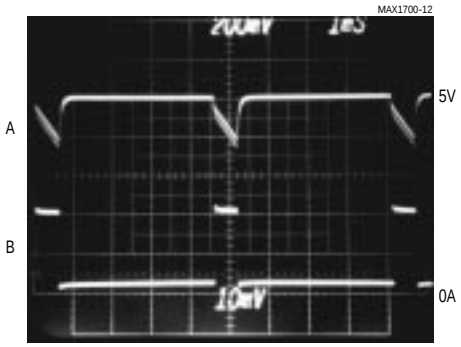
POWER-ON DELAY (PFM MODE)



5ms/div

A = V_{ON1}, 2V/div
B = V_{OUT}, 1V/div
C = INPUT CURRENT, 0.2A/div

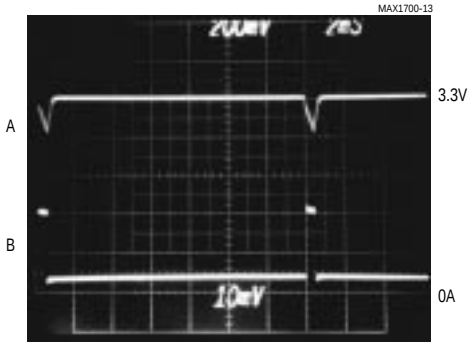
GSM LOAD-TRANSIENT RESPONSE



1ms/div

V_{IN} = 3.6V, V_{OUT} = 5V, C_{OUT} = 440µF
A = V_{OUT} RIPPLE, 200mV/div, AC COUPLED
B = LOAD CURRENT, 100mA TO 1A, 0.5A/div,
PULSE WIDTH = 577µs

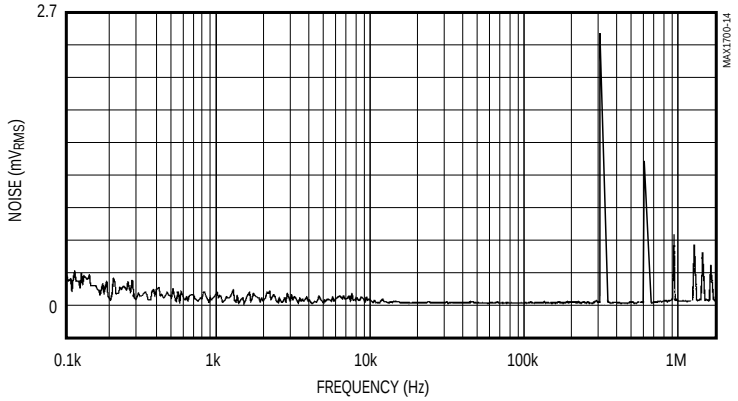
DECT LOAD-TRANSIENT RESPONSE



2ms/div

V_{IN} = 1.2V, V_{OUT} = 3.3V, C_{OUT} = 440µF
A = V_{OUT} RIPPLE, 200mV/div, AC COUPLED
B = LOAD CURRENT, 50mA TO 400mA, 0.2A/div,
PULSE WIDTH = 416µs

NOISE SPECTRUM
(V_{OUT} = 3.3V, V_{IN} = 1.2V, R_{LOAD} = 50Ω)



Pin Description

PIN		NAME	FUNCTION
MAX1700	MAX1701		
—	1	LBP	Low-Battery Comparator Non-Inverting Input
—	2	LBN	Low-Battery Comparator Inverting Input
3	3	REF	Reference Output. Bypass with a 0.22µF capacitor to GND. REF can source up to 50µA.
4	4	CLK/SEL	Switching-Mode Selection and External-Clock Synchronization Inputs. • CLK/SEL=Low: Low-power, delivers up to 10% of full load current. • CLK/SEL=High: High-power PWM mode. Full output power available. Operates in low-noise, constant-frequency mode. • CLK/SEL=External Clock: High-power PWM mode with the internal oscillator synchronized to the external clock. Turning on with CLK/SEL=0V also serves as a soft-start function since peak inductor current is limited to 25% of that allowed in PWM mode.
5	5	GND	Ground
—	6	POK	Power-Okay Comparator Output. Open drain N-channel output is low when V_{OUT} is 10% below regulation point. No internal delay is provided.
7	7	$\overline{ONB}$	Shutdown Input. When $\overline{ONB}$ =high and ONA=low, the IC is off and the load is connected to the battery through the Schottky diode.
8	8	ONA	Turn ON Input. When ONA=high or $\overline{ONB}$ =low, the IC turns on.
—	9	AO	Gain Block Output. This open-drain output sinks when $V_{AIN} < V_{REF}$.
—	10	AIN	Gain Block AIN input. When AIN is low, AO sinks current. The transconductance from AIN to AO is 9mmhos.
11	11	FB	DC-DC Converter Dual-Mode Feedback Input. For a fixed output voltage of +3.3V, connect FB to GND. For adjustable output, connect a divider between POUT and GND to set the output voltage in the range of 2.5V to 5V.
12	12	PGND	Source of N-Channel Power MOSFET Switch. Connect to high-current ground path.
13	13	LX	Drain of P-Channel Synchronous Rectifier and N-Channel Switch
14	14	OUT	Output Sense Input. Power source for the IC.
15	15	POUT	Source of P-Channel Synchronous Rectifier MOSFET Switch. Connect an external Schottky diode from LX to POUT.
—	16	LBO	Low-Battery Comparator Output. Open-drain N-channel output is low when LBN > LBP Input hysteresis is 15mV.
1, 2, 6, 9, 10, 16	—	I.C.	Internal Connection. Leave open or connect to GND.

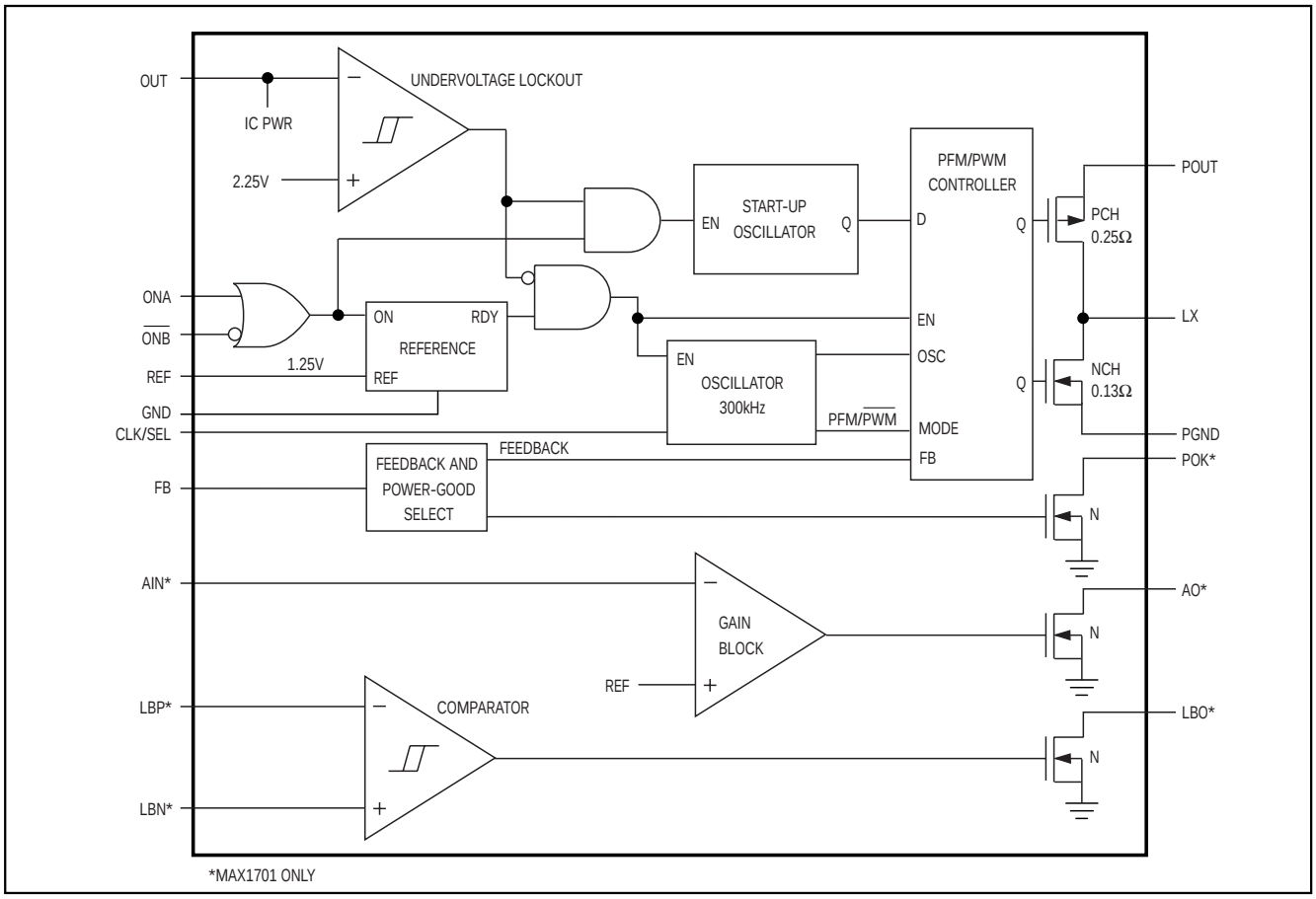


Figure 1. Functional Diagram

Detailed Description

The MAX1700/MAX1701 are highly efficient, low-noise power supplies for portable RF and data acquisition instruments. The MAX1700 combines a boost switching regulator, N-channel power MOSFET, P-channel synchronous rectifier, precision reference, and shutdown control. The MAX1701 contains all of the MAX1700 features plus a versatile gain amplifier, POK output, and a low-battery comparator (Figure 1). The MAX1700/MAX1701 come in a 16-pin QSOP package, which occupies no more space than an 8-pin SO.

The switching DC-DC converter boosts a 1- to 3-cell input to an adjustable output between 2.5V and 5.5V. The MAX1700/MAX1701 start from a low 1.1V input and remain operational down to 0.7V.

These devices are optimized for use in cellular phones and other applications requiring low noise during full-power operation, as well as low-quiescent current for maximum battery life during standby and shutdown modes. They feature constant-frequency (300kHz), low-noise PWM operation with up to 800mA output capability. See Table 1 for typical available output current. A low-quiescent-current, low-power mode offers an output up to 100mA and reduces quiescent power consumption to 200µW. In shutdown mode, the quiescent current is further reduced to just 3µA. Figure 2 shows the standard application circuit for the MAX1700/MAX1701.

Additional features include synchronous rectification for high efficiency and improved battery life, a POK output, and an uncommitted comparator for low-battery detection (MAX1701). A CLK input allows frequency synchronization to reduce interference. Dual shutdown controls allow shutdown using a momentary pushbutton switch and microprocessor control (MAX1701).

1-Cell to 3-Cell, High-Power (1A), Low-Noise, Step-Up DC-DC Converters

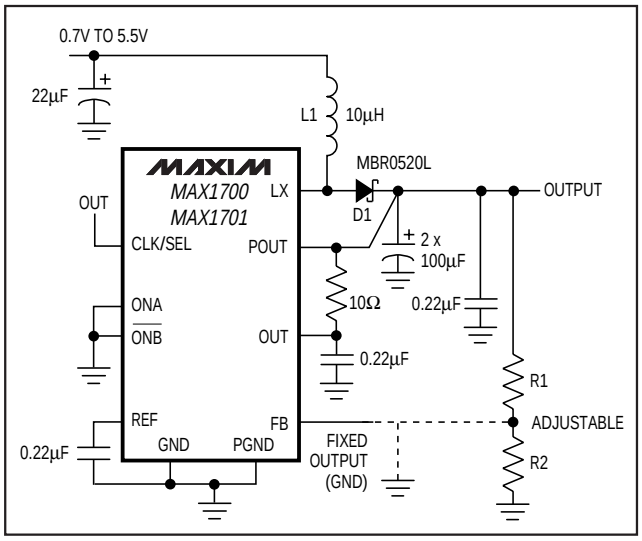


Figure 2. Fixed or Adjustable Output (PWM mode).

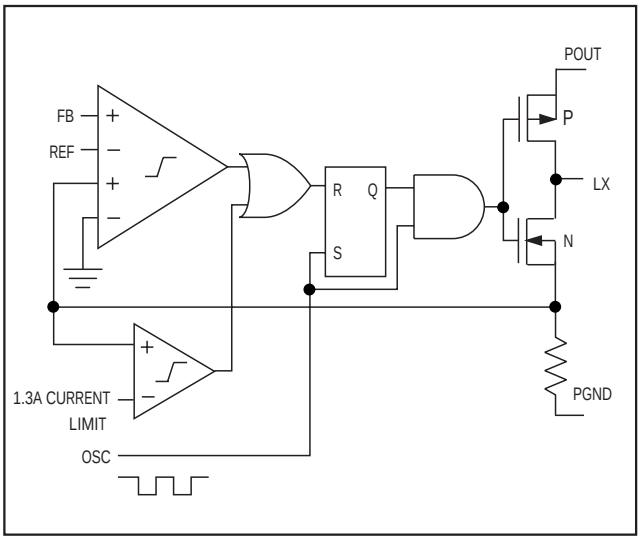


Figure 3. Simplified PWM Controller Block Diagram

Table 1. Typical Available Output Current

NUMBER OF CELLS	INPUT VOLTAGE (V)	OUTPUT VOLTAGE (V)	OUTPUT CURRENT (mA)
1 NiCd/NiMH	1.2	3.3	300
2 NiCd/NiMH	2.4	3.3	750
2 NiCd/NiMH	2.4	5.0	525
3 NiCd/NiMH or 1 Li-Ion	3.6	5.0	850

Table 2. Selecting the Operating Mode

CLK/SEL	MODE	FEATURES
0	Low Power	Low supply current
1	PWM	Low noise, high output current
External Clock (200kHz to 400kHz)	Synchronized PWM	Low noise, high output current

Step-Up Converter

The step-up switching DC-DC converter generates an adjustable output from 2.5V to 5.5V. During the first part of each cycle, the internal N-channel MOSFET switch is turned on. This allows current to ramp up in the inductor and store energy in a magnetic field. During the second part of each cycle, when the MOSFET is turned off, the voltage across the inductor reverses and forces current through the diode and synchronous rectifier to the output filter capacitor and load. As the energy stored in the inductor is depleted, the current ramps down and the output diode and synchronous rectifier turn off. Voltage across the load is regulated using either low-noise PWM or low-power operation, depending on the CLK/SEL pin setting (Table 2).

Low-Noise PWM Operation

When CLK/SEL is pulled high, the MAX1700/MAX1701 operate in a higher power, low-noise pulse-width-modulation (PWM) mode. During PWM operation, they switch at a constant frequency (300kHz) and then modulate the MOSFET switch pulse width to control the power transferred per cycle and regulate the voltage across the load. In PWM mode the devices can output up to 800mA. Switching harmonics generated by fixed-frequency operation are consistent and easily filtered. See the Noise Spectrum Plot in the *Typical Operating Characteristics.*

During PWM operation, each rising edge of the internal clock sets a flip-flop, which turns on the N-channel MOSFET switch (Figure 3). The switch is turned off when the sum of the voltage-error, slope compensation, and current-feedback signals trips a multi-input comparator and resets the flip-flop; the switch remains off for the rest of the cycle. When a change occurs in the output-voltage error signal into the comparator, it shifts the level to which the inductor current is allowed to ramp during each cycle and modulates the MOSFET switch pulse width. A second comparator enforces an inductor current limit of 1.6A max.

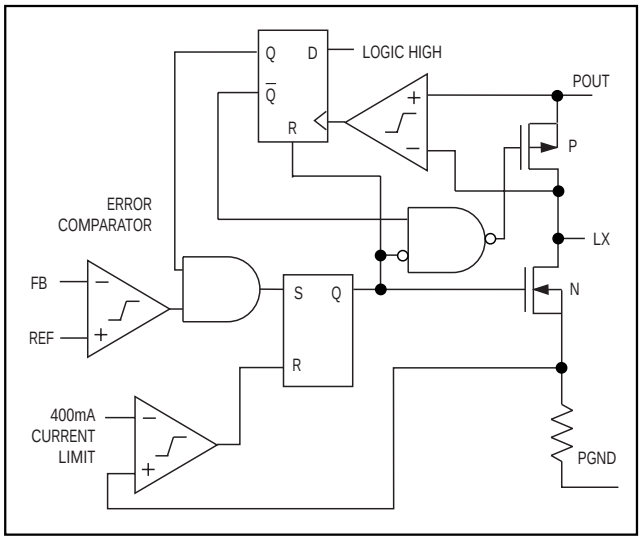


Figure 4. Controller Block Diagram in Low-Power PFM Mode

Synchronized PWM Operation

By applying an external clock to CLK/SEL, the MAX1700/MAX1701 can also be synchronized in PWM mode to a frequency between 200kHz and 400kHz. This allows the user to set the harmonics to avoid IF bands in wireless applications. The synchronous rectifier is also active during synchronized PWM operation.

Low-Power PFM Operation

Pulling CLK/SEL low places the MAX1700/MAX1701 in a low-power mode. During low-power mode, PFM operation regulates the output voltage by transferring a fixed amount of energy during each cycle and then modulating the switching frequency to control the power delivered to the output. The devices switch only as needed to service the load, resulting in the highest possible efficiency at light loads. Output current capability in PFM mode is 100mA. The output voltage is typically 1% higher than the output voltage in PWM mode.

During PFM operation, the error comparator detects the output voltage falling out of regulation and sets a flip-flop, turning on the N-channel MOSFET switch (Figure 4). When the inductor current ramps to the PFM mode current limit (400mA typical) and stores a fixed amount of energy, the current-sense comparator resets a flip-flop. The flip-flop turns off the N-channel switch and turns on the P-channel synchronous rectifier. A second flip-flop, previously reset by the switch's "on" signal, inhibits the error comparator from initiating another cycle until the energy stored in the inductor is transferred to the output filter capacitor and the synchronous rectifier current has ramped down to 70mA. This forces operation with a discontinuous inductor current.

Synchronous Rectifier

The MAX1700/MAX1701 feature an internal 250mΩ, P-channel synchronous rectifier to enhance efficiency. Synchronous rectification provides a 5% efficiency improvement over similar nonsynchronous boost regulators. In PWM mode, the synchronous rectifier is turned on during the second half of each switching cycle. In low-power mode, an internal comparator turns on the synchronous rectifier when the voltage at LX exceeds the boost-regulator output and then turns it off when the inductor current drops below 70mA.

Low-Voltage Start-Up Oscillator

The MAX1700/MAX1701 use a CMOS, low-voltage start-up oscillator for a 1.1V guaranteed minimum start-up input voltage at +25°C. On start-up, the low-voltage oscillator switches the N-channel MOSFET until the output voltage reaches 2.15V. Above this level, the normal boost-converter feedback and control circuitry take over. Once the device is in regulation, it can operate down to a 0.7V input since internal power for the IC is bootstrapped from the output using the OUT pin. Do not apply full load until the output exceeds 2.4V.

Table 3. On/Off Logic Control

ONA	$\overline{ONB}$	Status
0	0	On
0	1	Off
1	0	On
1	1	On

Shutdown

The MAX1700/MAX1701 shut down to reduce quiescent current to typically 3µA. During shutdown, the reference, low-battery comparator, gain block, and all feedback and control circuitry are off. The boost converter's output drops to one Schottky diode drop below the input.

Table 3 shows the control logic with ONA and $\overline{ONB}$. Both inputs have trip points near $0.5V_{OUT}$ with $0.15V_{OUT}$ hysteresis.

Low-Battery Comparator (MAX1701)

The internal low-battery comparator has uncommitted inputs and an open-drain output (LBO) capable of sinking 1mA. To use it as a low-battery-detection comparator, connect the LBN input to the reference, and connect the LBP input to an external resistor divider

1-Cell to 3-Cell, High-Power (1A), Low-Noise, Step-Up DC-DC Converters

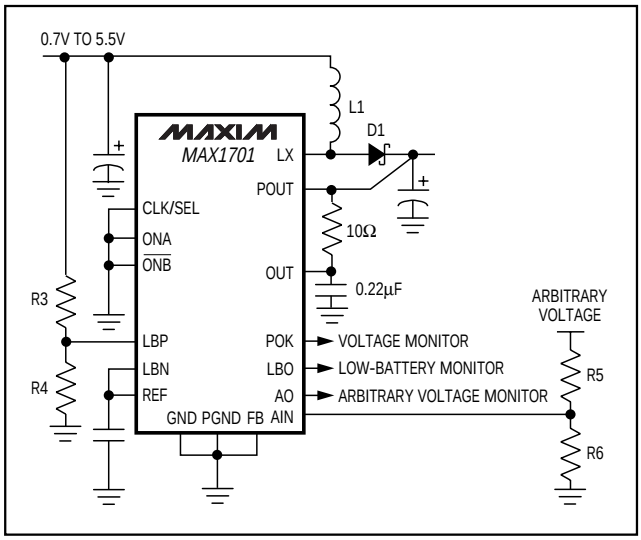


Figure 5. Detecting Battery Voltage Above 1.25V

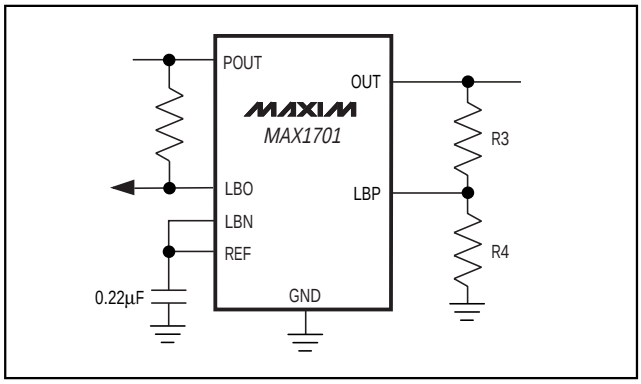


Figure 6. Using the Low-Battery Comparator to Sense the Output Voltage (MAX1701)

between the positive battery terminal and GND (Figure 5). The resistor values are then calculated as follows:

$$R3 = R4(V_{TH}/V_{LBN} - 1)$$

where V_{TH} is the desired input voltage trip threshold and $V_{LBN} = V_{REF} = 1.25V$. Since the input bias current into LBP is less than 20nA, R4 can be a large value (such as 270kΩ or less) without sacrificing accuracy. The inputs have a common-mode input range from 0.5V to 1.5V and an input-referred hysteresis of 15mV.

The low-battery comparator can also be used to monitor the output voltage, as shown in Figure 6.

To set the low-battery threshold to a voltage below the 1.25V reference, insert a resistor divider between REF and LBN and connect the battery to the LBP input through a 10kΩ current-limiting resistor (Figure 7). The equation for setting the resistors for the low-battery threshold is then as follows:

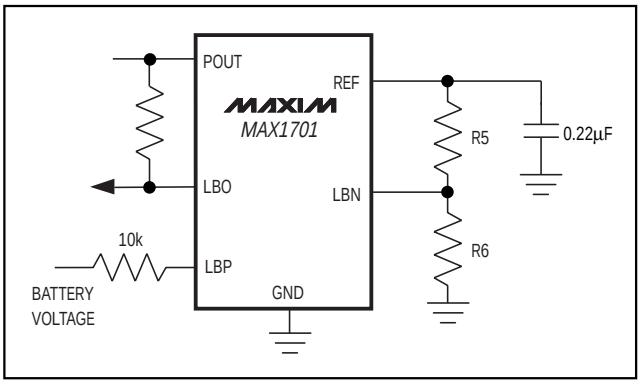


Figure 7. Detecting Battery Voltages Below 1.25V (MAX1701)

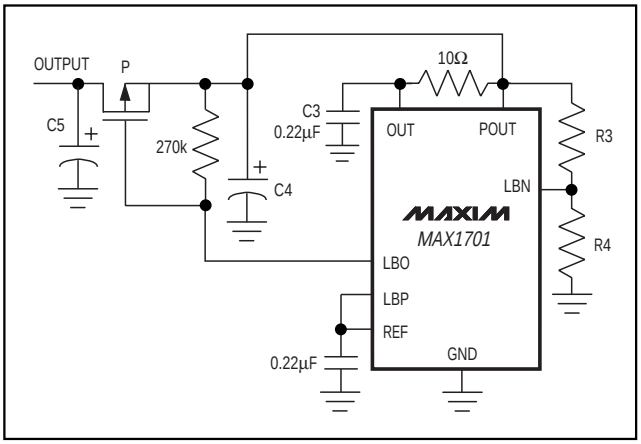


Figure 8. Using the Low-Battery Comparator for Load Control During Start-Up

$$R5 = R6(V_{REF}/V_{LBP} - 1)$$

where V_{LBP} is the desired voltage threshold. In Figures 5, 6, and 7, LBO goes low for a low-voltage input. The low-battery comparator can be used to check the output voltage or to control the load directly on P_{OUT} during start-up (Figure 8). Use the following equation to set the resistor values:

$$R3 = R4(V_{OUTTH}/V_{LBP} - 1)$$

where V_{OUTTH} is the desired output-voltage trip point and V_{LBP} is connected to the reference or 1.25V.

Reference

The MAX1700/MAX1701 have an internal 1.250V, 1% bandgap reference. Connect a 0.22µF bypass capacitor to GND within 0.2in. (5mm) of the REF pin. REF can source up to 50µA of external load current.

Power-OK (MAX1701)

The MAX1701 features a power-good comparator. This comparator's open-drain output (POK) is pulled low when the output voltage falls to 10% below the regulation point.

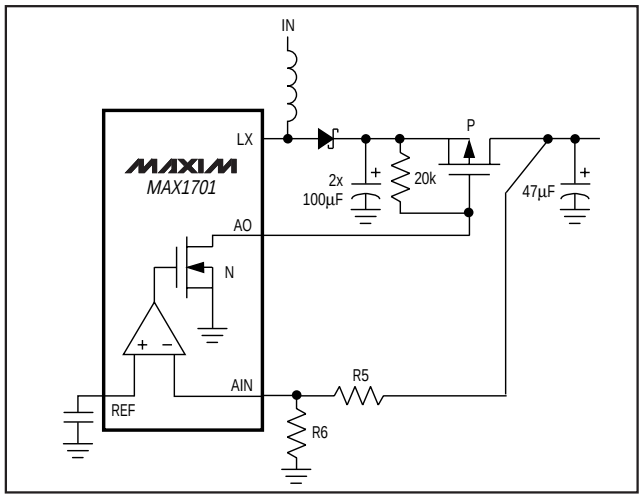


Figure 9. Using Gain Block as a Linear Regulator

Gain Block (MAX1701)

The MAX1701's gain block can function as a third comparator or can be used to build a linear regulator using an external P-channel MOSFET pass device. The gain-block output is a single-stage transconductance amplifier that drives an open-drain N-channel MOSFET. Figure 9 shows the gain block used in a linear regulator. The output of an external P-channel pass element is compared to the internal reference. The difference is amplified and used to drive the gate of the pass element. Use a logic-level PFET such as the Fairchild NDS336P ($R_{DS(ON)}$ = 270mΩ. If the PFET $R_{DS(ON)}$ is less than 250mΩ, the linear regulator output filter capacitance may need to be increased to above 47µF.

Design Procedure

Setting the Output Voltages

Set the output voltage between 2.5V and 5.5V by connecting a resistor voltage-divider to FB from OUT to GND, as shown in Figure 2. The resistor values are then as follows:

$$R1 = R2 (V_{OUT}/V_{FB} - 1)$$

where V_{FB}, the boost-regulator feedback setpoint, is 1.23V. Since the input bias current into FB is less than 20nA, R2 can have a large value (such as 270kΩ or less) without sacrificing accuracy. Connect the resistor voltage-divider as close to the IC as possible, within 0.2in. (5mm) of the FB pin.

Inductor Selection

The MAX1700/MAX1701's high switching frequency allows the use of a small surface-mount inductor. A 10µH inductor should have a saturation-current rating that exceeds the N-channel switch current limit of 1.6A. However, it is generally acceptable to bias the inductor current into saturation by as much as 20%, although this will slightly reduce efficiency. For high efficiency, choose an inductor with a high-frequency core material (such as ferrite) to reduce core losses. To minimize radiated noise, use a toroid, pot core, or shielded bobbin inductor. Connect the inductor from the battery to the LX pin as close to the IC as possible. See Table 4 for a list of component suppliers and Table 5 for suggested components.

Table 4. Component Suppliers

SUPPLIER	PHONE	FAX
AVX	USA: (803) 946-0690 (800) 282-4975	(803) 626-3123
Coilcraft	USA: (847) 639-6400	(847) 639-1469
Matsuo	USA: (714) 969-2491	(714) 960-6492
Motorola	USA: (602) 303-5454	(602) 994-6430
Sanyo	USA: (619) 661-6835 Japan: 81-7-2070-6306	(619) 661-1055 81-7-2070-1174
Sumida	USA: (847) 956-0666 Japan: 81-3-3607-5111	(847) 956-0702 81-3-3607-5144

Table 5. Component Selection Guide

PRODUCTION	INDUCTORS	CAPACITORS	DIODES
Surface Mount	Sumida CDR63B, CD73, CDR73B, CD74B series Coilcraft DO1608, DO3308, DT3316 series	Matsuo 267 series Sprague 595D series AVX TPS series	Motorola MBR0520L
Through Hole	Sumida RCH654 series	Sanyo OS-CON series Nichicon PL series	1N5817

1-Cell to 3-Cell, High-Power (1A), Low-Noise, Step-Up DC-DC Converters

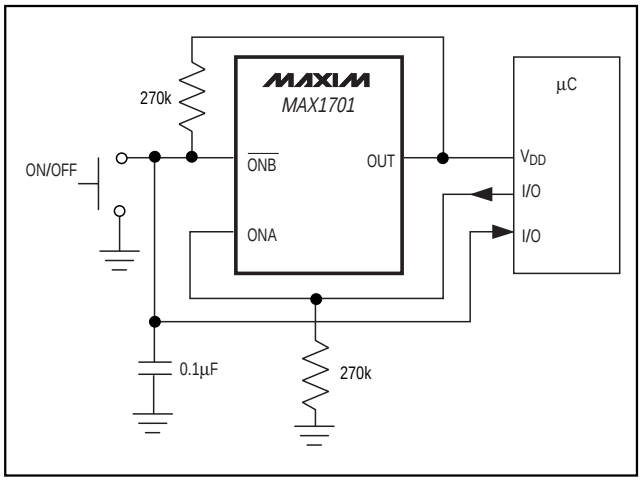


Figure 10. Momentary Pushbutton On/Off Switch

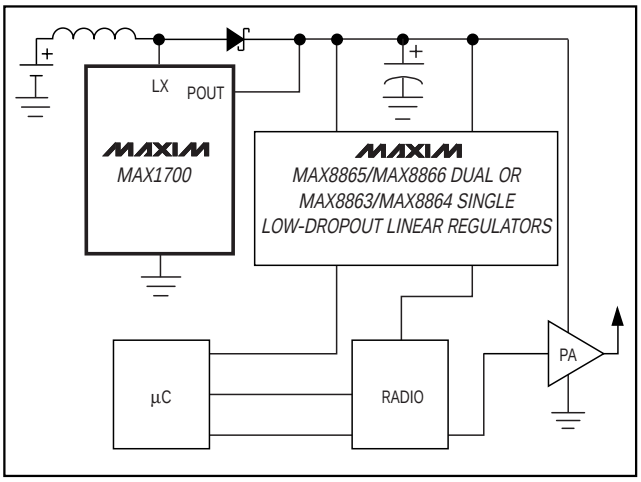


Figure 11. Typical Phone Application

Output Diode

Use a Schottky diode, such as a 1N5817, MBR0520L, or equivalent. The Schottky diode carries current during start-up, and in PFM mode after the synchronous rectifier turns off. Thus, its current rating only needs to be 500mA. Connect the diode between LX and P_{OUT} as close to the IC as possible. Do not use ordinary rectifier diodes since slow switching speeds and long reverse recovery times will compromise efficiency and load regulation.

Input and Output Filter Capacitors

Choose input and output filter capacitors that will service the input and output peak currents with acceptable voltage ripple. Choose input capacitors with working voltage ratings over the maximum input voltage, and output capacitors with working voltage ratings higher than the output.

For full output, two 100µF, 100mΩ, low-ESR tantalum output filter capacitors are recommended. For loads below 250mA, a single 100µF output capacitor will suffice. The input filter capacitor (CIN) reduces peak currents drawn from the input source and reduces input switching noise. The input voltage source impedance determines the required size of the input capacitor. When operating directly from one or two NiCd cells placed close to the MAX1700/MAX1701, use a 22µF, low-ESR input filter capacitor. When operating from a power source placed farther away, or from higher impedance batteries such as alkaline or lithium cells, use one or two 100µF, 100mΩ, low-ESR tantalum capacitors.

Sanyo OS-CON and Panasonic SP/CB-series ceramic capacitors offer the lowest ESR. Low-ESR tantalum capacitors are a good choice and generally offer a good tradeoff between price and performance. Do not exceed the ripple current ratings of tantalum capacitors. Avoid most aluminum-electrolytic capacitors, since their ESR is often too high.

Bypass Capacitors

Two ceramic bypass capacitors are required for proper operation. Bypass REF with a 0.22µF capacitor to GND. Also connect a 0.22µF ceramic capacitor from OUT to GND. Each should be placed as close to their respective pins as possible, within 0.2in. (5mm) of the DC-DC converter IC. See Table 4 for suggested suppliers.

Applications Information

Push-On/Push-Off Control

A momentary pushbutton switch can be used to turn the MAX1700/MAX1701 on and off. In Figure 10, ONA is pulled low and $\overline{ONB}$ is pulled high when the part is off. When the momentary switch is pressed, $\overline{ONB}$ is pulled low and the regulator turns on. The switch must be pressed long enough for the microcontroller to exit reset (200ms) and drive ONA high. A small capacitor is added to help debounce the switch. The controller issues a logic high to ONA, which holds the part on regardless of the switch state. To turn the regulator off, press the switch again, allowing the controller to read the switch status and pull ONA low. When the switch is released, $\overline{ONB}$ is pulled high.

Use in a Typical Wireless Phone Application

The MAX1700/MAX1701 are ideal for use in digital cordless and PCS phones. The power amplifier (PA) is connected directly to the boost-converter output for maximum voltage swing (Figure 11). Low-dropout linear regulators are used for post-regulation to generate

low-noise power for DSP, control, and RF circuitry. Typically, RF phones spend most of their life in standby mode with only short periods in transmit/receive mode. During standby, maximize battery life by setting CLK/SEL = 0; this places the IC in low-power mode (for the lowest quiescent power consumption).

Designing a PC Board

High switching frequencies and large peak currents make PC board layout an important part of design. Poor design can cause excessive EMI and ground-bounce, both of which can cause instability or regulation errors by corrupting the voltage and current feedback signals.

Power components (such as the inductor, converter IC, filter capacitors, and output diode) should be placed as close together as possible, and their traces should be kept short, direct, and wide. A separate low-noise ground plane containing the reference and signal grounds should only connect to the power-ground plane at one point. This minimizes the effect of power-ground currents on the part. Consult the MAX1701 EV kit manual for a layout example.

On multilayer boards, do not connect the ground pins of the power components using vias through an internal ground plane. Instead, place them close together and route them in a star-ground configuration using component-side copper. Then use vias to connect the star ground to the internal ground plane.

Keep the voltage feedback network very close to the IC, within 0.2in. (5mm) of the FB pins. Keep noisy traces, such as from the LX pin, away from the voltage feedback networks. Separate them with grounded copper. Consult the MAX1700 evaluation kit for a full PC board example.

Soft-Start

To implement soft-start, set CLK/SEL low on power-up; this forces low-power operation and reduces the peak switching current to 550mA max. Once the circuit is in regulation and start-up transients have settled, CLK/SEL can be set high for full-power operation.

Intermittent Supply/Battery Connections

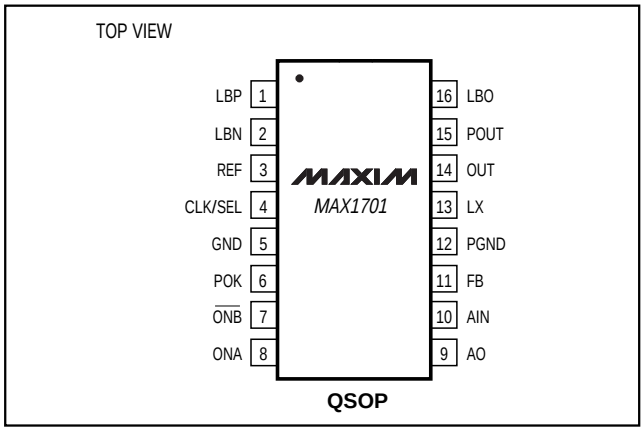
When boosting an input supply connected with a mechanical switch, or a battery connected with spring contacts, input power may sometimes be intermittent as a result of contact bounce. When operating in PFM mode with input voltages greater than 2.5V, restarting after such dropouts may initiate high current pulses that interfere with the MAX1700/MAX1701 internal MOSFET switch control. If contact or switch bounce is anticipated in the design, use one of the following solutions.

1) Connect a capacitor (C_{ONB}) from $\overline{ONB}$ to V_{IN}, a 1MΩ resistor (R_{ONB}) from $\overline{ONB}$ to GND, and tie ONA to GND (Figure 12). This RC network differentiates fast input edges at V_{IN} and momentarily holds the IC off until V_{IN} settles. The appropriate value of C_{ONB} is 10^{-5} times the total output filter capacitance (C_{OUT}), so a C_{OUT} of 200µF results in C_{ONB} = 2nF.

2) Use the system microcontroller to hold the MAX1700/MAX1701 in shut down from the time when power is applied (or reapplied) until the output capacitance (C_{OUT}) has charged to at least the input voltage. Power-on reset times of tens of milliseconds accomplish this.

3) Ensure that the IC operates, or at least powers up, in PWM mode (CLK/SEL = high). Activate PFM mode only after the V_{OUT} has settled and all of the system's power-on reset flags are cleared.

Pin Configurations (continued)



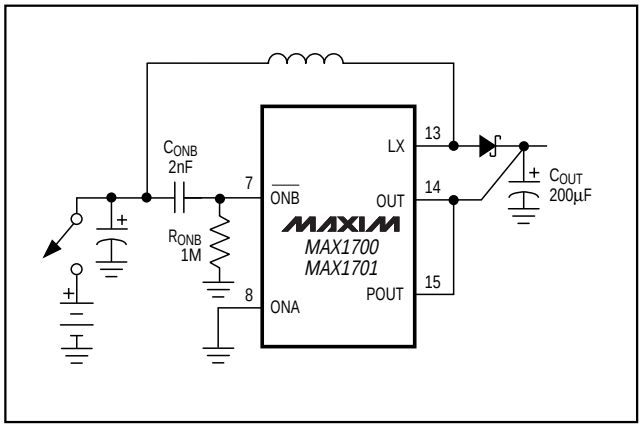


Figure 12. Connecting C_{ONB} and R_{ONB} when Switch or Battery-Contact Bounce Is Anticipated

1-Cell to 3-Cell, High-Power (1A), Low-Noise, Step-Up DC-DC Converters

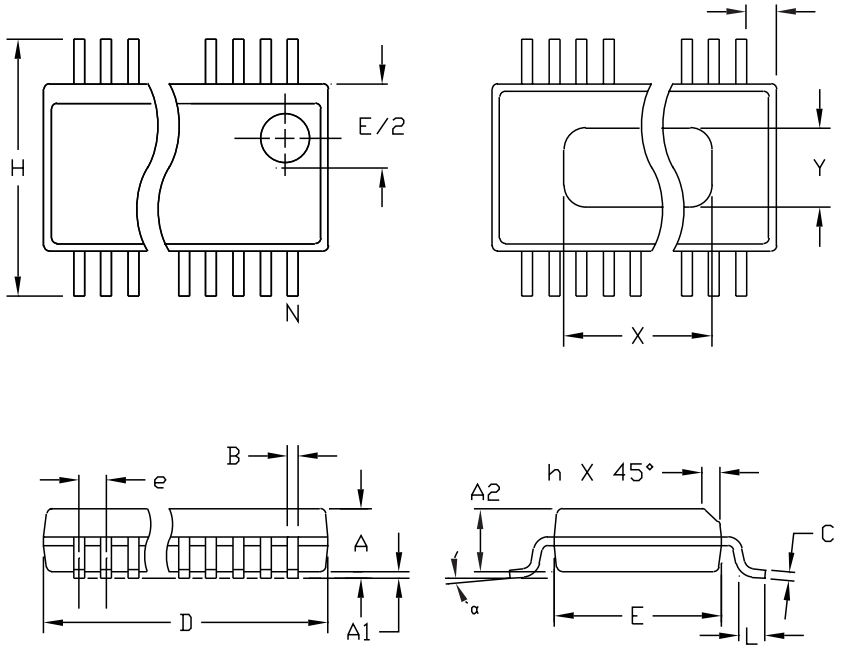
Chip Information

TRANSISTOR COUNT: 531

SUBSTRATE CONNECTED TO GND

Package Information

QSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
X	.107	.123	2.72	3.12		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		
X	.271	.287	6.88	7.29		

NOTES:

1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. HEAT SLUG DIMENSIONS X AND Y APPLY ONLY TO 16 AND 28 LEAD POWER-QSOP PACKAGES.
4. CONTROLLING DIMENSIONS: INCHES.

MAXIM

PROPRIETARY INFORMATION

TITLE:

PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0055	B	1/1