

IRFP4668PbF

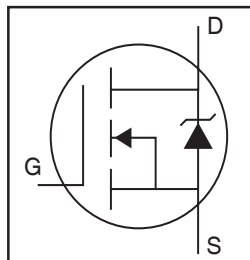
HEXFET® Power MOSFET

Applications

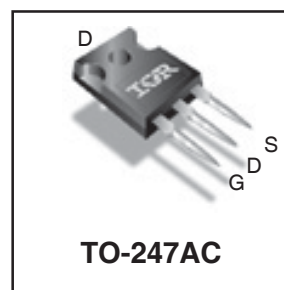
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free



V_{DSS}	200V
$R_{DS(on)}$ typ.	8.0mΩ
	max 9.7mΩ
I_D	130A



G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	130	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	92	
I_{DM}	Pulsed Drain Current ①	520	
P_D @ $T_C = 25^\circ\text{C}$	Maximum Power Dissipation	520	W
	Linear Derating Factor	3.5	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery ③	57	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

Avalanche Characteristics

E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ②	760	mJ
I_{AR}	Avalanche Current ①	See Fig. 14, 15, 22a, 22b,	A
E_{AR}	Repetitive Avalanche Energy ④		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧	—	0.29	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient ⑦⑧	—	40	

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.21	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 5mA$ ①
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	8.0	9.7	m Ω	$V_{GS} = 10V, I_D = 81A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 200V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 200V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
R_G	Internal Gate Resistance	—	1.0	—	Ω	

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	150	—	—	S	$V_{DS} = 50V, I_D = 81A$
Q_g	Total Gate Charge	—	161	241	nC	$I_D = 81A$
Q_{gs}	Gate-to-Source Charge	—	54	—		$V_{DS} = 100V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	52	—		$V_{GS} = 10V$ ④
Q_{sync}	Total Gate Charge Sync. ($Q_g - Q_{gd}$)	—	109	—		$I_D = 81A, V_{DS} = 0V, V_{GS} = 10V$
$t_{d(on)}$	Turn-On Delay Time	—	41	—	ns	$V_{DD} = 130V$
t_r	Rise Time	—	105	—		$I_D = 81A$
$t_{d(off)}$	Turn-Off Delay Time	—	64	—		$R_G = 2.7\Omega$
t_f	Fall Time	—	74	—		$V_{GS} = 10V$ ④
C_{iss}	Input Capacitance	—	10720	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	810	—		$V_{DS} = 50V$
C_{rss}	Reverse Transfer Capacitance	—	160	—		$f = 1.0MHz$
$C_{oss \text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related)⑥	—	630	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 160V$ ⑥
$C_{oss \text{ eff. (TR)}}$	Effective Output Capacitance (Time Related)⑤	—	790	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 160V$ ⑤

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	130	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	520		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 81A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	130	—	ns	$T_J = 25^\circ\text{C}$ $V_R = 100V,$
		—	155	—		$T_J = 125^\circ\text{C}$ $I_F = 81A$
Q_{rr}	Reverse Recovery Charge	—	633	—	nC	$T_J = 25^\circ\text{C}$ $di/dt = 100A/\mu s$ ④
		—	944	—		$T_J = 125^\circ\text{C}$
I_{RRM}	Reverse Recovery Current	—	8.7	—	A	$T_J = 25^\circ\text{C}$
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
 ② Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.23mH$
 $R_G = 25\Omega$, $I_{AS} = 81A$, $V_{GS} = 10V$. Part not recommended for use above this value.
 ③ $I_{SD} \leq 81A$, $di/dt \leq 520A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
 ④ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.

- ⑤ $C_{oss \text{ eff. (TR)}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
 ⑥ $C_{oss \text{ eff. (ER)}}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
 ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
 ⑧ R_{θ} is measured at T_J approximately 90°C .

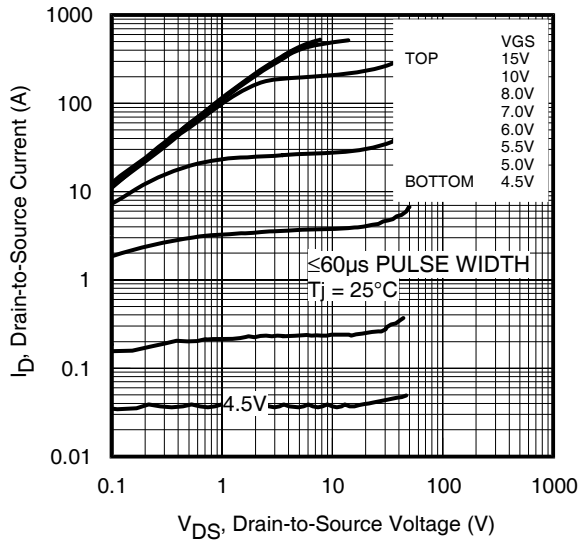


Fig 1. Typical Output Characteristics

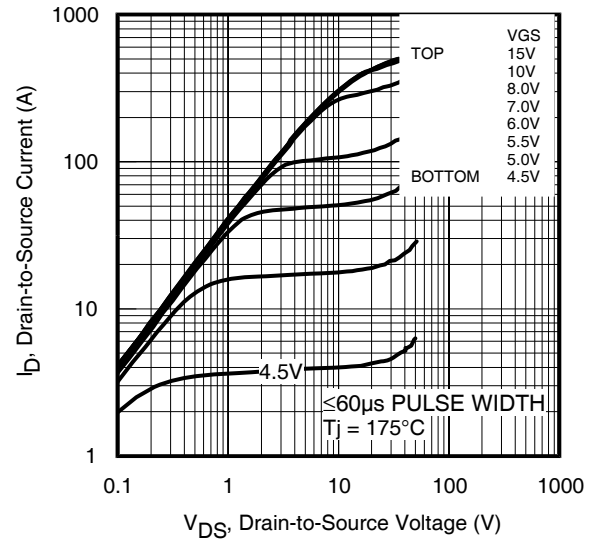


Fig 2. Typical Output Characteristics

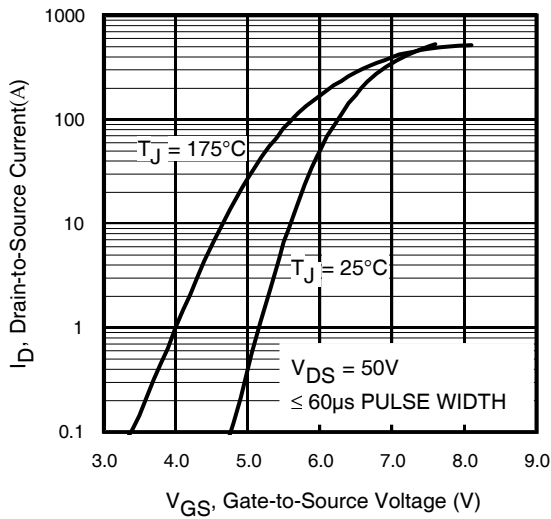


Fig 3. Typical Transfer Characteristics

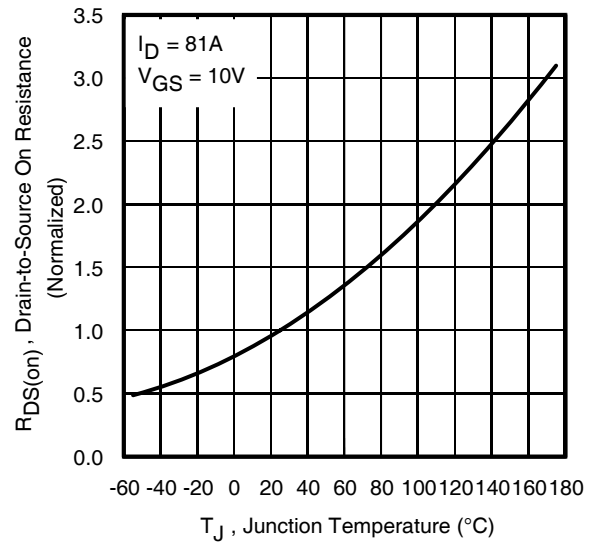


Fig 4. Normalized On-Resistance vs. Temperature

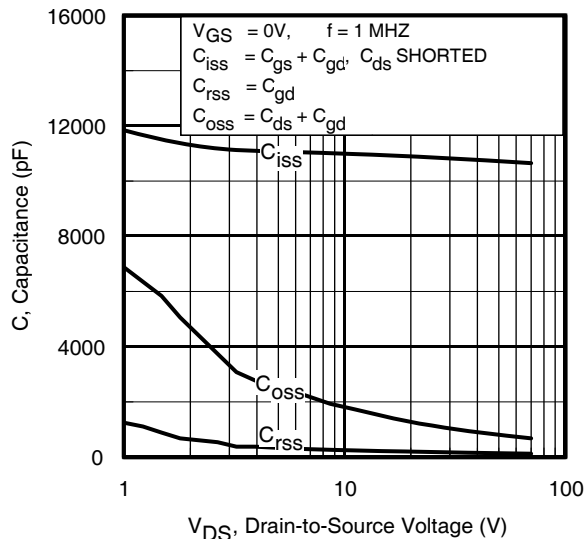


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

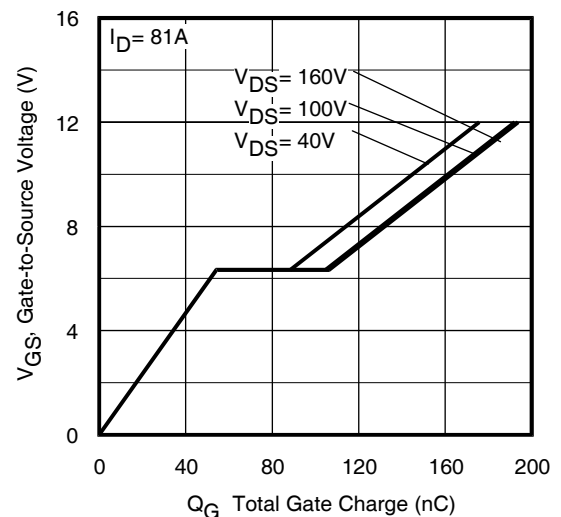


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

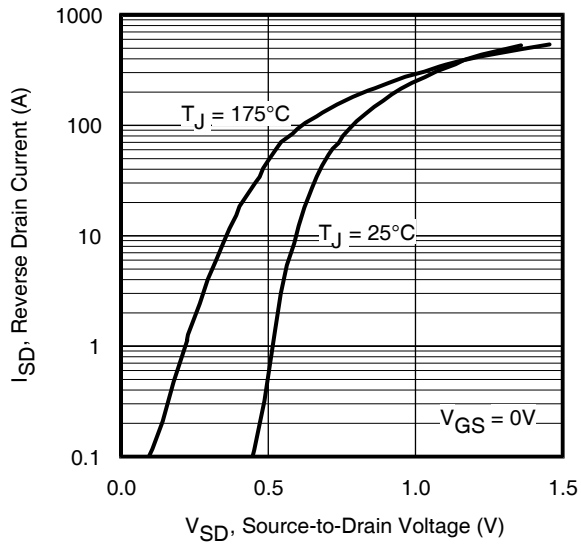


Fig 7. Typical Source-Drain Diode Forward Voltage

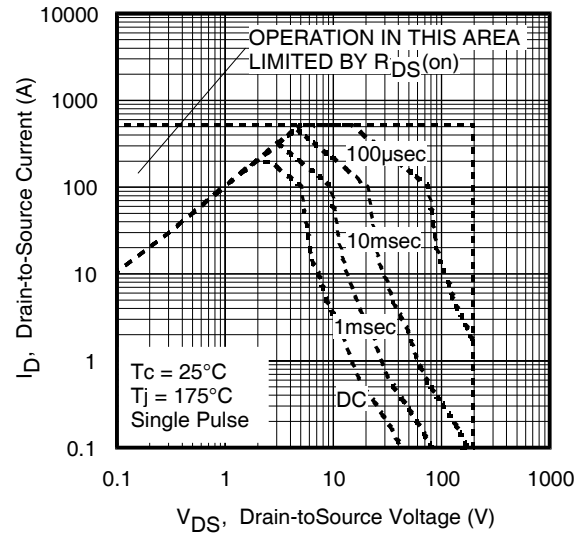


Fig 8. Maximum Safe Operating Area

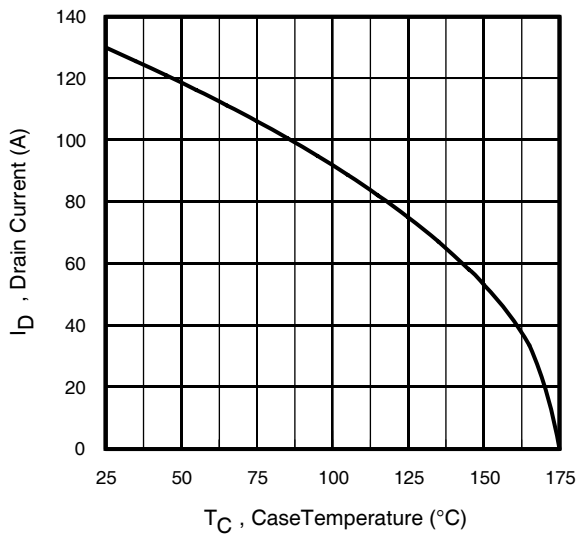


Fig 9. Maximum Drain Current vs. Case Temperature

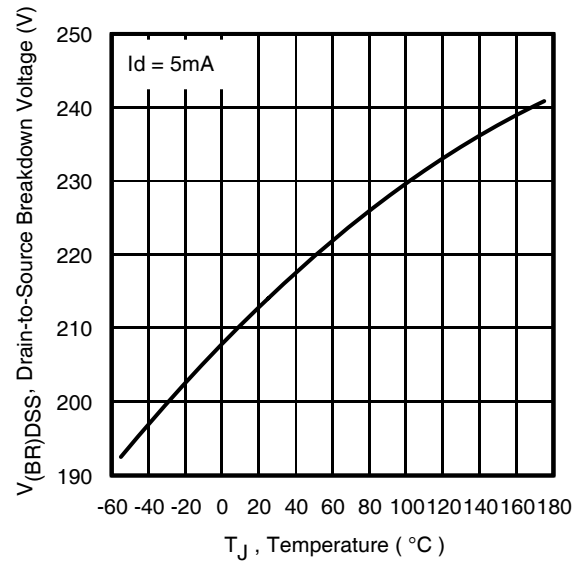


Fig 10. Drain-to-Source Breakdown Voltage

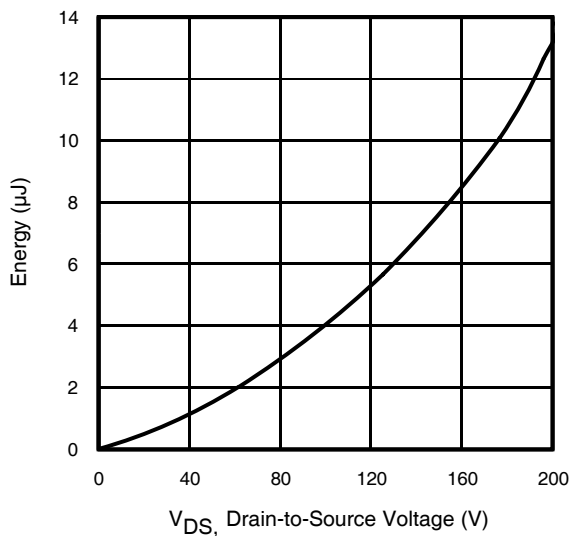


Fig 11. Typical C_{OSS} Stored Energy

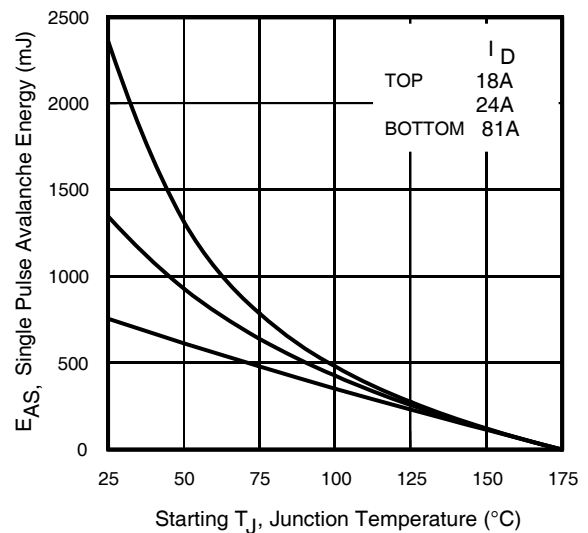


Fig 12. Maximum Avalanche Energy Vs. DrainCurrent

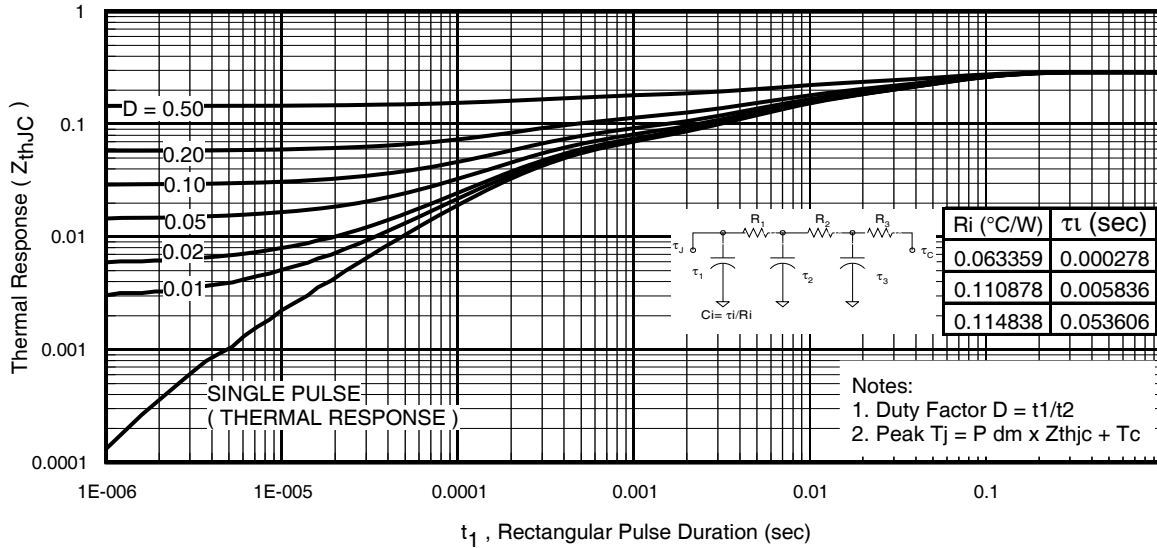


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

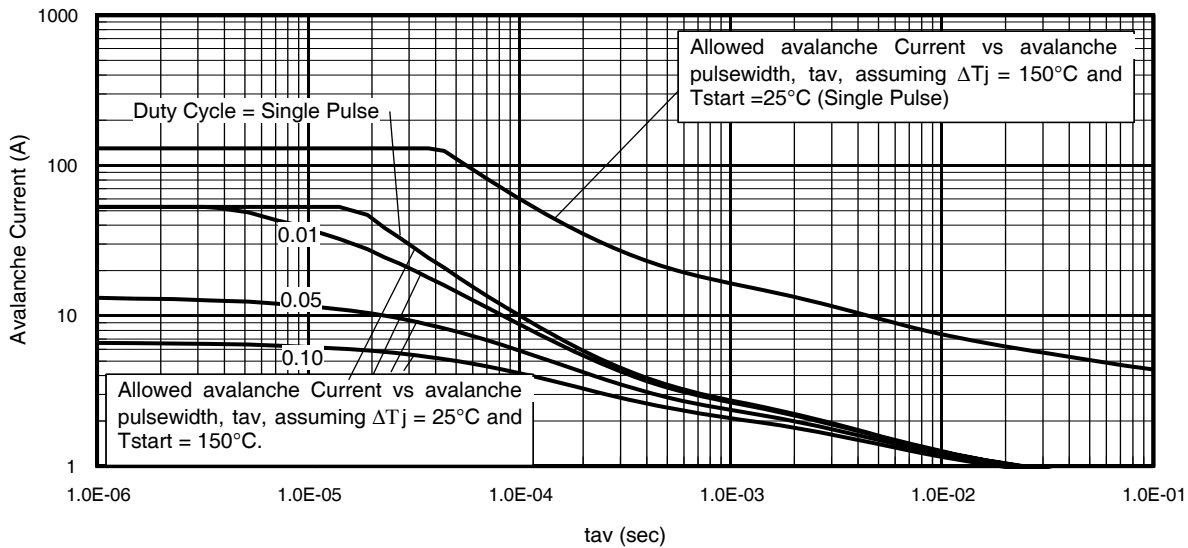
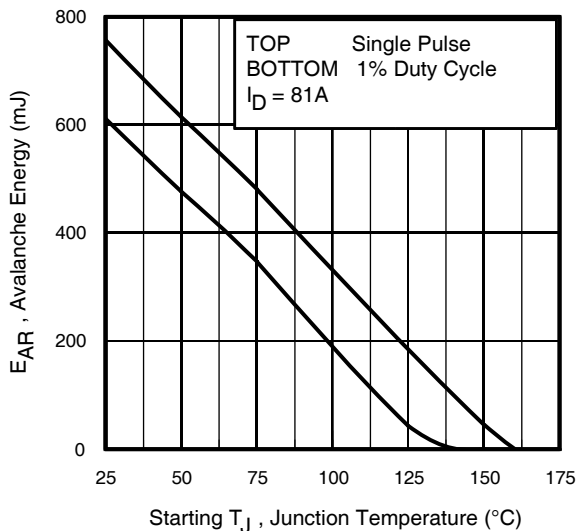


Fig 14. Typical Avalanche Current vs. Pulsewidth



Notes on Repetitive Avalanche Curves, Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 22a, 22b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

Fig 15. Maximum Avalanche Energy vs. Temperature

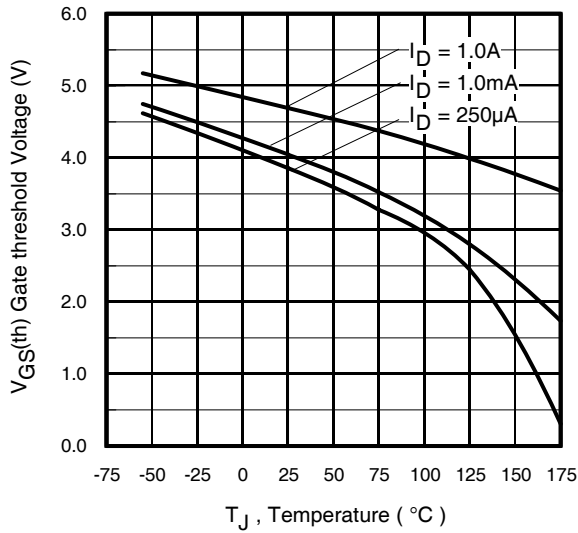


Fig. 16. Threshold Voltage Vs. Temperature

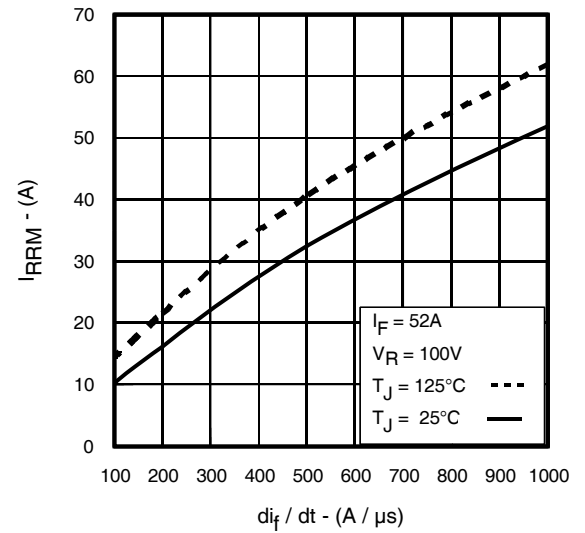


Fig. 17 - Typical Recovery Current vs. di_f/dt

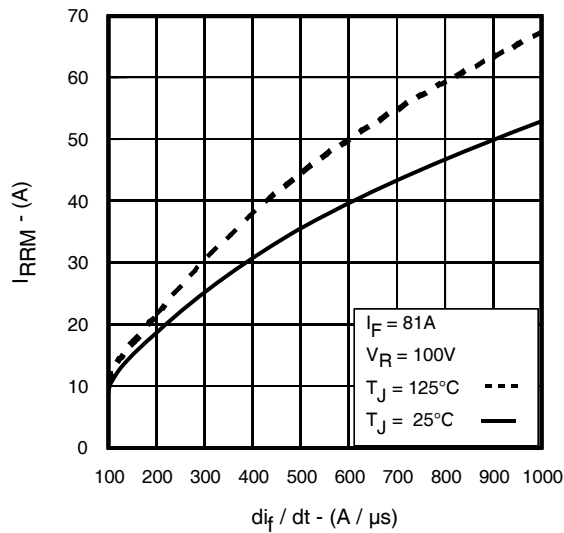


Fig. 18 - Typical Recovery Current vs. di_f/dt

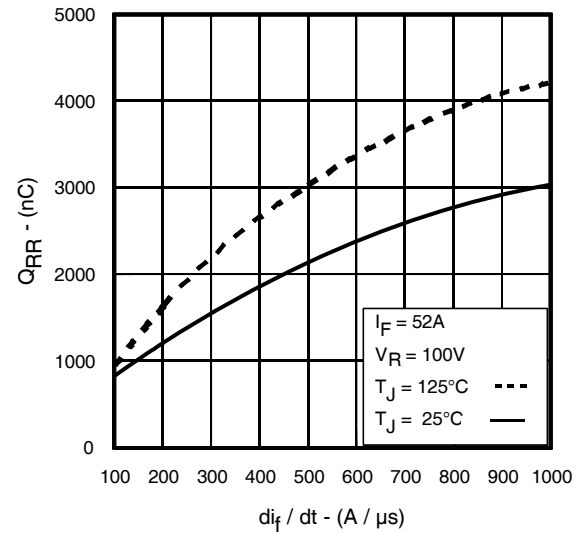


Fig. 19 - Typical Stored Charge vs. di_f/dt

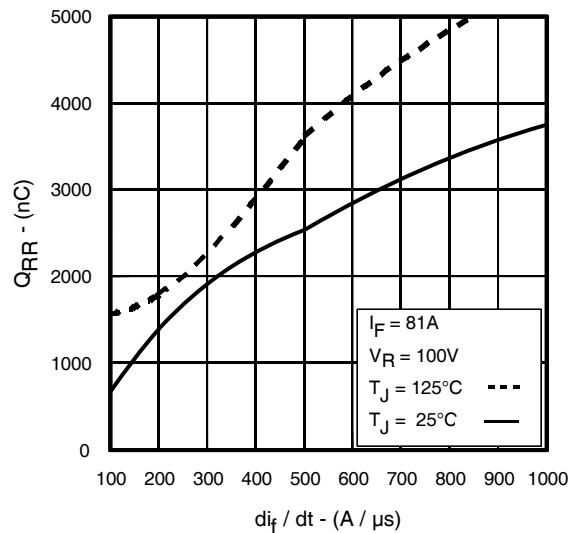
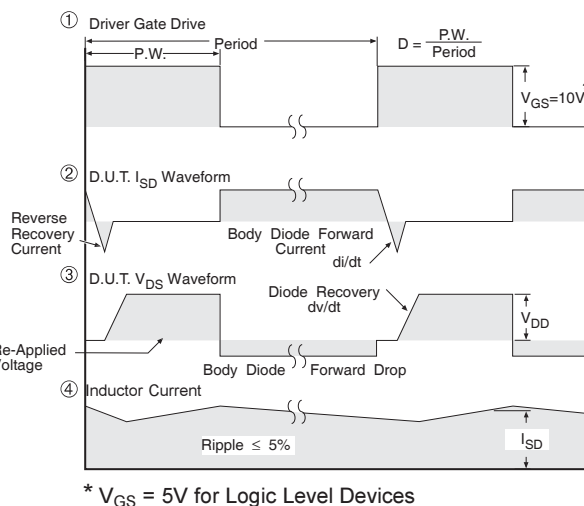


Fig. 20 - Typical Stored Charge vs. di_f/dt



* $V_{GS} = 5V$ for Logic Level Devices

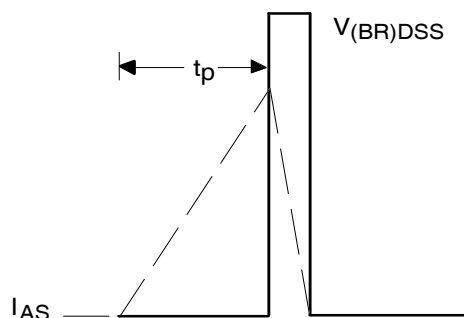


Fig 22b. Unclamped Inductive Waveforms

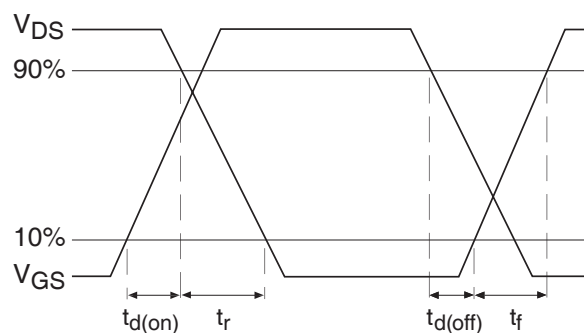


Fig 23b. Switching Time Waveforms

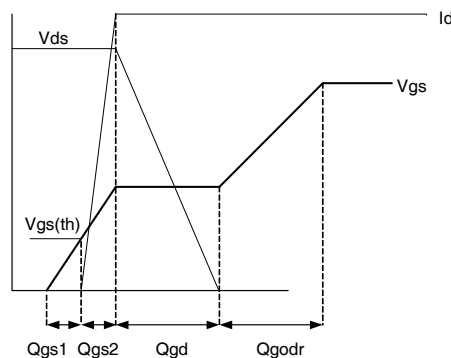


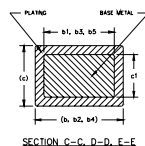
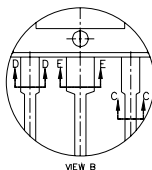
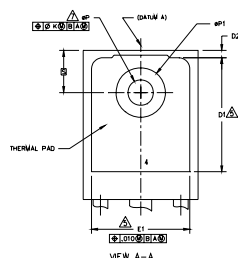
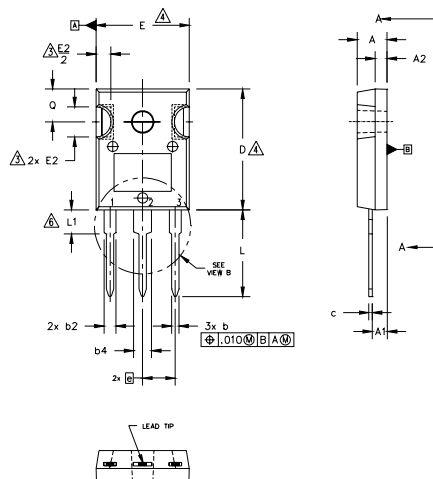
Fig 24b. Gate Charge Waveform

IRFP4668PbF

TO-247AC Package Outline

Dimensions are shown in millimeters (inches)

International
IR Rectifier



NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. ØP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC.

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	
D1	.515	—	13.08	—	4
D2	.020	.053	0.51	1.35	5
E	.602	.625	15.29	15.87	
E1	.530	—	13.46	—	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
Øk	.010		0.25		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
ØP	.140	.144	3.56	3.66	
ØP1	—	.291	—	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

- 1.— GATE
- 2.— DRAIN
- 3.— SOURCE
- 4.— DRAIN

IGBTs, CoPACK

- 1.— GATE
- 2.— COLLECTOR
- 3.— EMITTER
- 4.— COLLECTOR

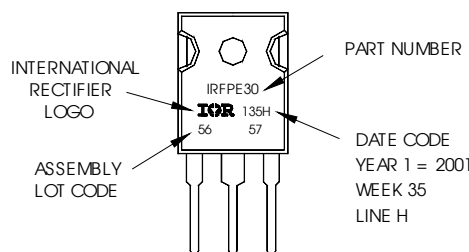
DIODES

- 1.— ANODE/OPEN
- 2.— CATHODE
- 3.— ANODE

TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW35, 2001
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position
indicates "Lead-Free"



TO-247AC packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IR Rectifier

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TAC Fax: (310) 252-7903

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