



# 82541ER Gigabit Ethernet Controller

Networking Silicon

## Datasheet

### Product Features

- PCI Bus
  - PCI revision 2.3, 32-bit, 33/66 MHz
  - Algorithms that optimally use advanced PCI, MWI, MRM, and MRL commands
  - 3.3 V (5 V tolerant PCI signaling)
- MAC Specific
  - Low-latency transmit and receive queues
  - IEEE 802.3x-compliant flow-control support with software-controllable thresholds
  - Caches up to 64 packet descriptors in a single burst
  - Programmable host memory receive buffers (256 B to 16 KB) and cache line size (16 B to 256 B)
  - Wide, optimized internal data path architecture
  - 64 KB configurable Transmit and Receive FIFO buffers
- PHY Specific
  - Integrated for 10/100/1000 Mb/s operation
  - IEEE 802.3ab Auto-Negotiation support
  - IEEE 802.3ab PHY compliance and compatibility
  - State-of-the-art DSP architecture implements digital adaptive equalization, echo cancellation, and cross-talk cancellation
  - Automatic polarity detection
  - Automatic detection of cable lengths and MDI vs. MDI-X cable at all speeds
- Host Off-Loading
  - Transmit and receive IP, TCP, and UDP checksum off-loading capabilities
  - Transmit TCP segmentation
  - Advanced packed filtering
  - Jumbo frame support up to 16 KB
  - Intelligent Interrupt generation (multiple packets per interrupt)
- Manageability
  - Network Device Class Power Management Specification 1.1
  - Compliance with PCI Power Management 1.1 and ACPI 2.0
  - SNMP and RMON statistic counters
  - D0 and D3 power states
- Additional Device
  - Four programmable LED outputs
  - On-chip power control circuitry
  - BIOS LAN Disable pin
  - JTAG (IEEE 1149.1) Test Access Port built in silicon
- Lead-free<sup>a</sup> 196-pin Ball Grid Array (BGA). Devices that are lead-free are marked with a circled “e1” and have the product code: LUxxxxxx.

- a. This device is lead-free. That is, lead has not been intentionally added, but lead may still exist as an impurity at <1000 ppm. The Material Declaration Data Sheet, which includes lead impurity levels and the concentration of other Restriction on Hazardous Substances (RoHS)-banned materials, is available at:  
[ftp://download.intel.com/design/packtech/material\\_content\\_IC\\_Package.pdf#pagemode=bookmarks](ftp://download.intel.com/design/packtech/material_content_IC_Package.pdf#pagemode=bookmarks)  
In addition, this device has been tested and conforms to the same parametric specifications as previous versions of the device.  
For more information regarding lead-free products from Intel Corporation, contact your Intel Field Sales representative

## Revision History

| Date      | Revision | Notes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-----------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Aug 2003  | 2.0      | Non-classified release.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| Mar 2004  | 3.0      | Updated Section 4, "Voltage, Temperature, and Timing Specifications," for the C-0 stepping.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| Oct 2004  | 3.1      | <ul style="list-style-type: none"> <li>Corrected EEMODE signal description.</li> <li>Updated signal names to match design guide and reference schematics.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                   |
| Nov 2004  | 3.2      | <ul style="list-style-type: none"> <li>Added lead free information.</li> <li>Added information about migrating from a 2-layer 0.36 mm wide-trace substrate to a 2-layer 0.32 mm wide-trace substrate. Refer to the section on Package and Pinout Information.</li> <li>Added statement that no changes to existing soldering processes are needed for the 2-layer 0.32 mm wide-trace substrate change in the section describing "Package Information".</li> <li>Corrected pinout discrepancies between sections "Signal Descriptions" and "Package and Pinout Information".</li> </ul> |
| Jan 2005  | 3.3      | <ul style="list-style-type: none"> <li>Added new maximum values for DC supply voltages on 1.2 V and 1.8 V pins. See Table 2, Recommended Operating Conditions and Table 6, DC Characteristics.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                              |
| Feb 2005  | 3.4      | <ul style="list-style-type: none"> <li>Updated Visual Pin Assignment diagram for pinouts F9, F10, E14, F14, and H14.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| Apr 2005  | 3.5      | <ul style="list-style-type: none"> <li>Removed all references to CLK_RUN# signal.</li> <li>Corrected the FLSH_SO/LAN_DISABLE signal definition. If Flash functionality is not used then an external pull-down resistor is required.</li> </ul>                                                                                                                                                                                                                                                                                                                                         |
| July 2005 | 3.6      | <ul style="list-style-type: none"> <li>Added pin C8 description to Table 29 and Table 31.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| Aug 2005  | 3.7      | <ul style="list-style-type: none"> <li>Corrected 25 MHz Clock Input Requirements in Table 13.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| June 2006 | 3.8      | <ul style="list-style-type: none"> <li>Corrected the FLSH_SO/LAN_DISABLE signal definition. If Flash functionality is not used then an external pull-up resistor is required.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                               |
| June 2006 | 3.9      | <ul style="list-style-type: none"> <li>Updated Table 13 "25 MHz Clock Input Requirements".</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| Aug 2006  | 4.0      | <ul style="list-style-type: none"> <li>Updated Table 40 descriptions for pins A10, B10, and C9.</li> <li>Updated pinout descriptions from Tables 25 - 42 to match Figure 13.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                |
| Sept 2006 | 4.1      | <ul style="list-style-type: none"> <li>Removed note "b" from Table 2 and note "a" from Tables 3 and 4. Moved the note following Table 5 before Table 3 "3.3V Supply Voltage Ramp".</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                          |

Information in this document is provided in connection with Intel products. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Intel's Terms and Conditions of Sale for such products, Intel assumes no liability whatsoever, and Intel disclaims any express or implied warranty, relating to sale and/or use of Intel products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right. Intel products are not intended for use in medical, life saving, or life sustaining applications.

Intel may make changes to specifications and product descriptions at any time, without notice.

Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them.

The 82541ER Gigabit Ethernet Controller may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature may be obtained by calling 1-800-548-4725 or by visiting Intel's website at <http://www.intel.com>.

Intel® is a trademark or registered trademark of Intel Corporation or its subsidiaries in the United States and other countries.

Copyright © Intel Corporation, 2006

\*Third-party brands and names are the property of their respective owners.

# Contents

|            |                                                              |           |
|------------|--------------------------------------------------------------|-----------|
| <b>1.0</b> | <b>Introduction .....</b>                                    | <b>1</b>  |
| 1.1        | Document Scope .....                                         | 1         |
| 1.2        | Reference Documents .....                                    | 2         |
| 1.3        | Product Codes .....                                          | 2         |
| 1.4        | Block Diagram .....                                          | 3         |
| <b>2.0</b> | <b>Product Code .....</b>                                    | <b>5</b>  |
| <b>3.0</b> | <b>Signal Descriptions .....</b>                             | <b>7</b>  |
| 3.1        | Signal Type Definitions .....                                | 7         |
| 3.2        | PCI Bus Interface Signals (56) .....                         | 7         |
| 3.2.1      | PCI Address, Data and Control Signals (44) .....             | 8         |
| 3.2.2      | Arbitration Signals (2) .....                                | 9         |
| 3.2.3      | Interrupt Signal (1) .....                                   | 9         |
| 3.2.4      | System Signals (3) .....                                     | 9         |
| 3.2.5      | Error Reporting Signals (2) .....                            | 10        |
| 3.2.6      | Power Management Signals (2) .....                           | 10        |
| 3.3        | EEPROM and Serial FLASH Interface Signals (9) .....          | 10        |
| 3.4        | Miscellaneous Signals .....                                  | 11        |
| 3.4.1      | LED Signals (4) .....                                        | 11        |
| 3.4.2      | Other Signals (4) .....                                      | 11        |
| 3.5        | PHY Signals .....                                            | 11        |
| 3.5.1      | Crystal Signals (2) .....                                    | 11        |
| 3.5.2      | Analog Signals (10) .....                                    | 12        |
| 3.6        | Test Interface Signals (6) .....                             | 12        |
| 3.7        | Power Supply Connections .....                               | 13        |
| 3.7.1      | Digital and Analog Supplies .....                            | 13        |
| 3.7.2      | Grounds, Reserved Pins and No Connects .....                 | 13        |
| 3.7.3      | Voltage Regulation Control Signals (2) .....                 | 13        |
| <b>4.0</b> | <b>Voltage, Temperature, and Timing Specifications .....</b> | <b>15</b> |
| 4.1        | Absolute Maximum Ratings .....                               | 15        |
| 4.2        | Targeted Recommended Operating Conditions .....              | 15        |
| 4.2.1      | General Operating Conditions .....                           | 15        |
| 4.2.2      | Voltage Ramp and Sequencing Recommendations .....            | 16        |
| 4.3        | DC Specifications .....                                      | 18        |
| 4.4        | AC Characteristics .....                                     | 21        |
| 4.5        | Timing Specifications .....                                  | 23        |
| 4.5.1      | PCI Bus Interface .....                                      | 23        |
| 4.5.1.1    | PCI Bus Interface Clock .....                                | 23        |
| 4.5.1.2    | PCI/PCI-X Bus Interface Timing .....                         | 24        |
| 4.5.2      | Link Interface Timing .....                                  | 27        |
| 4.5.3      | EEPROM Interface .....                                       | 27        |
| <b>5.0</b> | <b>Package and Pinout Information .....</b>                  | <b>29</b> |
| 5.1        | Package Information .....                                    | 29        |
| 5.2        | Thermal Specifications .....                                 | 31        |

|     |                              |    |
|-----|------------------------------|----|
| 5.3 | Pinout Information .....     | 32 |
| 5.4 | Visual Pin Assignments ..... | 42 |

## Figures

|    |                                                             |    |
|----|-------------------------------------------------------------|----|
| 1  | 82541ER Block Diagram .....                                 | 3  |
| 2  | AC Test Loads for General Output Pins .....                 | 23 |
| 3  | PCI Clock Timing .....                                      | 23 |
| 4  | PCI Bus Interface Output Timing Measurement .....           | 24 |
| 5  | PCI Bus Interface Input Timing Measurement Conditions ..... | 25 |
| 6  | TVAL (max) Rising Edge Test Load .....                      | 25 |
| 7  | TVAL (max) Falling Edge Test Load .....                     | 26 |
| 8  | TVAL (min) Test Load .....                                  | 26 |
| 9  | TVAL Test Load (PCI 5 V Signaling Environment) .....        | 26 |
| 10 | Link Interface Rise/Fall Timing .....                       | 27 |
| 11 | 82541ER Mechanical Specifications .....                     | 29 |
| 12 | 196 PBGA Package Pad Detail .....                           | 30 |
| 13 | Visual Pin Assignments .....                                | 42 |

## Tables

|    |                                                       |    |
|----|-------------------------------------------------------|----|
| 1  | Absolute Maximum Ratings .....                        | 15 |
| 2  | Recommended Operating Conditions .....                | 15 |
| 3  | 3.3V Supply Voltage Ramp .....                        | 16 |
| 4  | 1.8V Supply Voltage Ramp .....                        | 16 |
| 5  | 1.2V Supply Voltage Ramp .....                        | 17 |
| 6  | DC Characteristics .....                              | 18 |
| 7  | Power Specifications - D0a .....                      | 18 |
| 8  | Power Specifications - D3cold .....                   | 18 |
| 9  | Power Specifications D(r) Uninitialized) .....        | 19 |
| 10 | Power Specifications - Complete Subsystem .....       | 19 |
| 11 | I/O Characteristics .....                             | 20 |
| 12 | AC Characteristics: 3.3 V Interfacing .....           | 21 |
| 13 | 25 MHz Clock Input Requirements .....                 | 21 |
| 14 | Reference Crystal Specification Requirements .....    | 22 |
| 15 | Link Interface Clock Requirements .....               | 22 |
| 16 | EEPROM Interface Clock Requirements .....             | 22 |
| 17 | AC Test Loads for General Output Pins .....           | 22 |
| 18 | PCI Bus Interface Clock Parameters .....              | 23 |
| 19 | PCI Bus Interface Timing Parameters .....             | 24 |
| 20 | PCI Bus Interface Timing Measurement Conditions ..... | 25 |
| 21 | Rise and Fall Times .....                             | 27 |
| 22 | Link Interface Clock Requirements .....               | 27 |
| 23 | Link Interface Clock Requirements .....               | 27 |
| 24 | Thermal Characteristics .....                         | 31 |
| 25 | PCI Address, Data and Control Signals .....           | 32 |
| 26 | PCI Arbitration Signals .....                         | 32 |
| 27 | Interrupt Signals .....                               | 32 |
| 28 | System Signals .....                                  | 32 |
| 29 | Error Reporting Signals .....                         | 33 |
| 30 | Power Management Signals .....                        | 33 |
| 31 | Serial EEPROM Interface Signals .....                 | 33 |

|    |                                         |    |
|----|-----------------------------------------|----|
| 32 | Serial FLASH Interface Signals .....    | 33 |
| 33 | LED Signals.....                        | 33 |
| 34 | Other Signals.....                      | 33 |
| 35 | IEEE Test Signals .....                 | 34 |
| 36 | PHY Signals .....                       | 34 |
| 37 | Test Interface Signals.....             | 34 |
| 38 | Digital Power Signals .....             | 34 |
| 39 | Analog Power Signals .....              | 35 |
| 40 | Grounds and No Connect Signals.....     | 35 |
| 41 | Voltage Regulation Control Signals..... | 35 |
| 42 | Signal Names in Pin Order .....         | 36 |



**Note:** This page is intentionally blank.

## 1.0 Introduction

---

The Intel<sup>®</sup> 82541ER Gigabit Ethernet is a single, compact component with an integrated Gigabit Ethernet Media Access Control (MAC) and physical layer (PHY) functions. For embedded communication and network devices such as web kiosks, and Point-of-Sale terminal designs with critical space constraints, the Intel 82541ER allows for a Gigabit Ethernet implementation in a very small area that is footprint compatible with current generation 10/100 Mbps Fast Ethernet designs.

The Intel<sup>®</sup> 82541ER integrates fourth generation gigabit MAC design with fully integrated, physical layer circuitry to provide a standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE\_TX, and 10BASE-T applications (802.3, 802.3u, and 802.3ab). The controller is capable of transmitting and receiving data at rates of 1000 Mbps, 100 Mbps, or 10 Mbps. In addition to managing MAC and PHY layer functions, the controller provides a 32-bit wide direct Peripheral Component Interconnect (PCI) 2.3 compliant interface capable of operating at 33 or 66 MHz.

The 82541ER Architecture is designed for high performance and low memory latency. Wide internal data paths eliminate performance bottlenecks by efficiently handling large address and data words. The 82541ER controller includes advanced interrupt handling features to limit PCI bus traffic and a PCI interface that maximizes efficient bus usage. The 82541ER uses efficient ring buffer descriptor data structures, with up to 64 packet descriptors cached on chip. A large 64 KByte on-chip packet buffer maintains superior performance as available PCI bandwidth changes. In addition, using hardware acceleration, the controller offloads tasks from the host controller, such as TCP/UDP/IP checksum calculations and TCP segmentation.

The 82541ER is packaged in a 15 mm X 15 mm 196-ball grid array and is pin compatible with the 82559ER/82551ER 10/100 Mbps Fast Ethernet Multifunction PCI/CardBus Controller, 82562EZ/82562EX Platform LAN Connect devices, the 82540EM Gigabit Ethernet Controller and the 82540EP Gigabit Ethernet Controller.

### 1.1 Document Scope

This document contains datasheet specifications for the 82541ER Gigabit Ethernet Controller, including signal descriptions, DC and AC parameters, packaging data, and pinout information.

## **1.2 Reference Documents**

This document assumes that the designer is acquainted with high-speed design and board layout techniques. The following documents provide additional information:

- 82546EZ(EX)/82551ER(IT) & 82541ER Combined Footprint LOM Design Guide. Intel Corporation.
- 82547GI(EI)/82541(PI/GIEI) & 82541ER EEPROM Map and Programming Information Guide. Intel Corporation.
- PCI Local Bus Specification, Revision 2.3. PCI Special Interest Group.
- PCI Bus Power Management Interface Specification, Revision 1.1. PCI Special Interest Group.
- IEEE Standard 802.3, 2003 Edition. Incorporates various IEEE standards previously published separately. Institute of Electrical and Electronics Engineers (IEEE).
- Intel Ethernet Controllers Timing Device Selection Guide. Intel Corporation.
- PCI Mobile Design Guide, Revision 1.1. PCI Special Interest Group.

Software driver developers should contact their local Intel representatives for programming information.

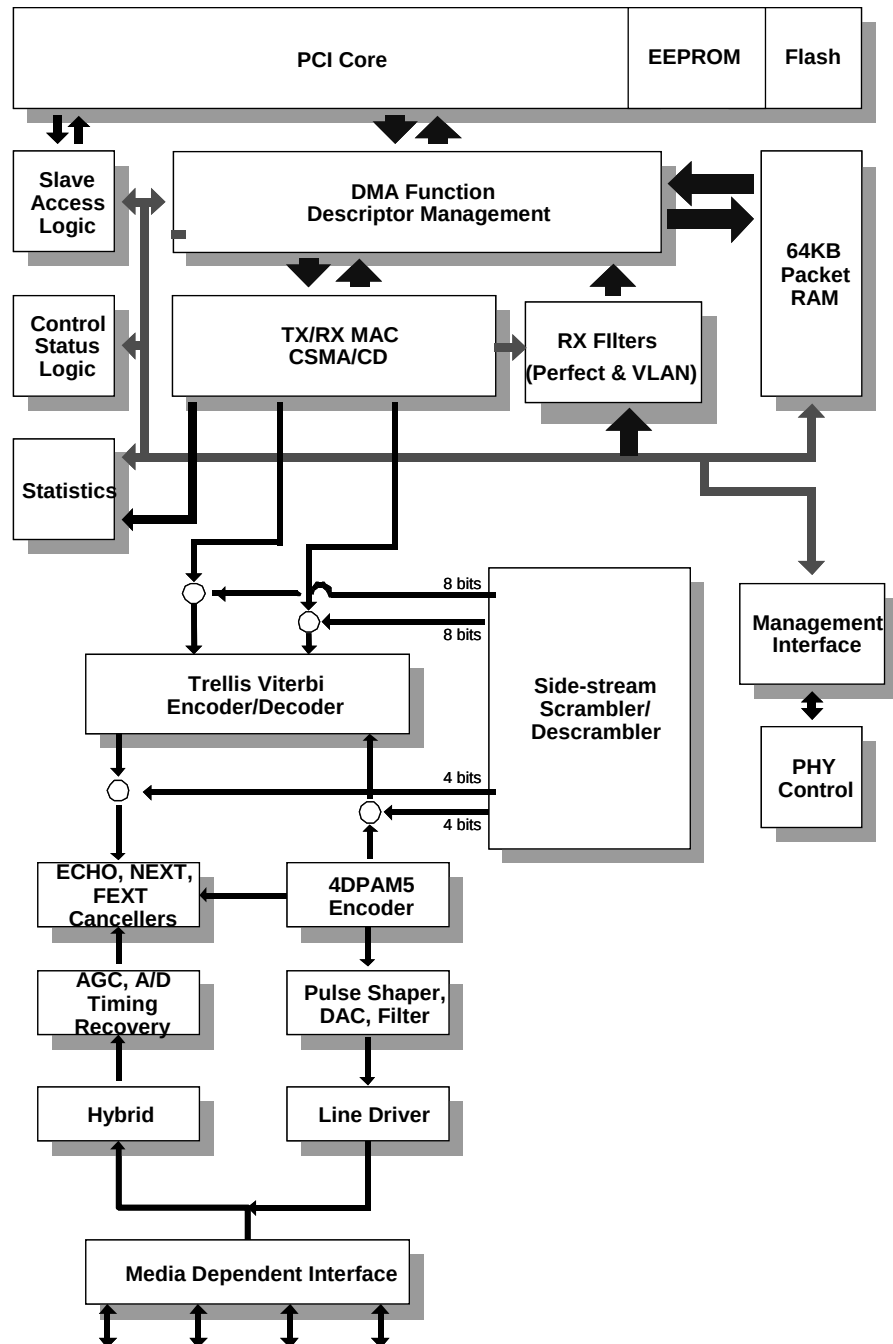
## **1.3 Product Codes**

The product ordering codes are:

- GD82541ER
- LU82541ER



## 1.4 Block Diagram



### Figure 1. 82541ER Block Diagram



**Note:** This page intentionally left blank.

## **2.0      Product Code**

---

The product code for the 82541ER Gigabit Ethernet Controller is: GD82541ER.



**Note:** This page intentionally left blank.

## 3.0 Signal Descriptions

### 3.1 Signal Type Definitions

The signals of the 82541ER controller are electrically defined as follows:

| Name | Definition                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| I    | <b>Input.</b> Standard input only digital signal.                                                                                                                                                                                                                                                                                                                                                                                                                 |
| O    | <b>Output.</b> Standard output only digital signal.                                                                                                                                                                                                                                                                                                                                                                                                               |
| TS   | <b>Tri-state.</b> Bi-directional tri-state digital input/output signal.                                                                                                                                                                                                                                                                                                                                                                                           |
| STS  | <b>Sustained Tri-state.</b> An active low tri-state signal owned and driven by only one agent at a time. The agent that drives an STS pin low must drive it high for at least one clock before letting it float. A new agent cannot start driving an STS signal any sooner than one clock after the previous owner tri-states it. A pullup is required to sustain the inactive state until another agent drives it, and must be provided by the central resource. |
| OD   | <b>Open Drain.</b> Wired-OR with other agents.<br>The signaling agent asserts the OD signal, but the signal is returned to the inactive state by a weak pull-up resistor. The pull-up resistor may require two or three clock periods to fully restore the signal to the de-asserted state.                                                                                                                                                                       |
| A    | <b>Analog.</b> PHY analog data signal.                                                                                                                                                                                                                                                                                                                                                                                                                            |
| P    | <b>Power.</b> Power connection, voltage reference, or other reference connection.                                                                                                                                                                                                                                                                                                                                                                                 |

### 3.2 PCI Bus Interface Signals (56)

When the Reset signal (RST#) is asserted, the 82541ER will not drive any PCI output or bi-directional pins.

### 3.2.1 PCI Address, Data and Control Signals (44)

| Symbol     | Type | Name and Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|------------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| AD[31:0]   | TS   | <p><b>Address and Data.</b> Address and data signals are multiplexed on the same PCI pins. A bus transaction includes an address phase followed by one or more data phases.</p> <p>The address phase is the clock cycle when the Frame signal (FRAME#) is asserted low. During the address phase AD[31:0] contain a physical address (32 bits). For I/O, this is a byte address, and for configuration and memory, a DWORD address. The 82541ER device uses little endian byte ordering.</p> <p>During data phases, AD[7:0] contain the least significant byte (LSB) and AD[31:24] contain the most significant byte (MSB).</p>                                                  |
| C/BE#[3:0] | TS   | <p><b>Bus Command and Byte Enables.</b> Bus command and byte enable signals are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE#[3:0] define the bus command. In the data phase, C/BE#[3:0] are used as byte enables. The byte enables are valid for the entire data phase and determine which byte lanes contain meaningful data.</p> <p>C/BE#[0] applies to byte 0 (LSB) and C/BE#[3] applies to byte 3 (MSB).</p>                                                                                                                                                                                                                           |
| PAR        | TS   | <p><b>Parity.</b> The Parity signal is issued to implement even parity across AD[31:0] and C/BE#[3:0]. PAR is stable and valid one clock after the address phase. During data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted after a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase.</p> <p>When the 82541ER controller is a bus master, it drives PAR for address and write data phases, and as a slave device, drives PAR for read data phases.</p>                                                                                |
| FRAME#     | STS  | <p><b>Cycle Frame.</b> The Frame signal is driven by the 82541ER device to indicate the beginning and length of a bus transaction.</p> <p>While FRAME# is asserted, data transfers continue. FRAME# is de-asserted when the transaction is in the final data phase.</p>                                                                                                                                                                                                                                                                                                                                                                                                          |
| IRDY#      | STS  | <p><b>Initiator Ready.</b> Initiator Ready indicates the ability of the 82541ER controller (as a bus master device) to complete the current data phase of the transaction. IRDY# is used in conjunction with the Target Ready signal (TRDY#). The data phase is completed on any clock when both IRDY# and TRDY# are asserted.</p> <p>During the write cycle, IRDY# indicates that valid data is present on AD[31:0]. For a read cycle, it indicates the master is ready to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together. The 82541ER controller drives IRDY# when acting as a master and samples it when acting as a slave.</p>       |
| TRDY#      | STS  | <p><b>Target Ready.</b> The Target Ready signal indicates the ability of the 82541ER controller (as a selected device) to complete the current data phase of the transaction. TRDY# is used in conjunction with the Initiator Ready signal (IRDY#). A data phase is completed on any clock when both TRDY# and IRDY# are sampled asserted.</p> <p>During a read cycle, TRDY# indicates that valid data is present on AD[31:0]. For a write cycle, it indicates the target is ready to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together. The 82541ER device drives TRDY# when acting as a slave and samples it when acting as a master.</p> |
| STOP#      | STS  | <p><b>Stop.</b> The Stop signal indicates the current target is requesting the master to stop the current transaction. As a slave, the 82541ER controller drives STOP# to request the bus master to stop the transaction. As a master, the 82541ER controller receives STOP# from the slave to stop the current transaction.</p>                                                                                                                                                                                                                                                                                                                                                 |

| Symbol  | Type | Name and Function                                                                                                                                                                                                                                                                    |
|---------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IDSEL#  | I    | <b>Initialization Device Select.</b> The Initialization Device Select signal is used by the 82541ER as a chip select signal during configuration read and write transactions.                                                                                                        |
| DEVSEL# | STS  | <b>Device Select.</b> When the Device Select signal is actively driven by the 82541ER, it signals notifies the bus master that it has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.       |
| VIO     | P    | <b>VIO.</b> The VIO signal is a voltage reference for the PCI interface (3.3 V or 5 V PCI signaling environment). It is used as the clamping voltage.<br><b>Note:</b> VIO should be connected to 3.3V Aux or 5V Aux in order to be compatible with the pull-up clamps specification. |

### 3.2.2 Arbitration Signals (2)

| Symbol | Type | Name and Function                                                                                                                 |
|--------|------|-----------------------------------------------------------------------------------------------------------------------------------|
| REQ#   | TS   | <b>Request Bus.</b> The Request Bus signal is used to request control of the bus from the arbiter. This signal is point-to-point. |
| GNT#   | I    | <b>Grant Bus.</b> The Grant Bus signal notifies the 82541ER that bus access has been granted. This is a point-to-point signal.    |

### 3.2.3 Interrupt Signal (1)

| Symbol | Type | Name and Function                                                                                                                      |
|--------|------|----------------------------------------------------------------------------------------------------------------------------------------|
| INTA#  | TS   | <b>Interrupt A.</b> Interrupt A is used to request an interrupt of the 82541ER. It is an active low, level-triggered interrupt signal. |

### 3.2.4 System Signals (3)

| Symbol | Type | Name and Function                                                                                                                                                                                                                                                                                                              |
|--------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CLK    | I    | <b>PCI Clock.</b> The PCI Clock signal provides timing for all transactions on the PCI bus and is an input to the 82541ER device. All other PCI signals, except the Interrupt A (INTA#) and PCI Reset signal (RST#), are sampled on the rising edge of CLK. All other timing parameters are defined with respect to this edge. |
| M66EN  | I    | <b>66 MHz Enable.</b> M66EN indicates whether the system bus is enabled for 66MHz                                                                                                                                                                                                                                              |
| RST#   | I    | <b>PCI Reset.</b> When the PCI Reset signal is asserted, all PCI output signals are floated and all input signals are ignored.<br>Most of the internal state of the 82541ER is reset on the de-assertion (rising edge) of RST#.                                                                                                |

### 3.2.5 Error Reporting Signals (2)

| Symbol | Type | Name and Function                                                                                                                                                                                                                                                                                                                                                                                         |
|--------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SERR#  | OD   | <b>System Error.</b> The System Error signal is used by the 82541ER controller to report address parity errors. SERR# is open drain and is actively driven for a single PCI clock when reporting the error.                                                                                                                                                                                               |
| PERR#  | STS  | <b>Parity Error.</b> The Parity Error signal is used by the 82541ER controller to report data parity errors during all PCI transactions except by a Special Cycle. PERR# is sustained tri-state and must be driven active by the 82541ER controller two data clocks after a data parity error is detected. The minimum duration of PERR# is one clock for each data phase a data parity error is present. |

### 3.2.6 Power Management Signals (2)

| Symbol       | Type | Name and Function                                                                                                                                                                                                         |
|--------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LAN_PWR_GOOD | I    | <b>Power Good (Power-on Reset).</b> The Power Good signal is used to indicate that stable power is available for the 82541ER. When the signal is low, the 82541ER holds itself in reset state and floats all PCI signals. |
| AUX_PWR      | I    | <b>Auxiliary Power.</b> If the Auxiliary Power signal is high, then auxiliary power is available and the 82541ER device should support the D3cold power state.                                                            |

## 3.3 EEPROM and Serial FLASH Interface Signals (9)

| Symbol                   | Type | Name and Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|--------------------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| EEMODE                   | I    | <b>EEPROM Mode.</b> The EEPROM Mode pin is used to select the interface and source of the EEPROM used to initialize the device. For a Microwire* EEPROM on the standard EEPROM pins, tie this pin to ground with a 100 $\Omega$ pull-down resistor. For a Serial Peripheral Interface (SPI*) EEPROM, leave this pin disconnected.                                                                                                                                                                                               |
| EEDI                     | O    | <b>EEPROM Data Input.</b> The EEPROM Data Input pin is used for output to the memory device.                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| EEDO                     | I    | <b>EEPROM Data Output.</b> The EEPROM Data Output pin is used for input from the memory device. The EEDO includes an internal pull-up resistor.<br>Note: Voltage for EEDO must be less than 0.7 V.                                                                                                                                                                                                                                                                                                                              |
| EECS                     | O    | <b>EEPROM Chip Select.</b> The EEPROM Chip Select signal is used to enable the device.                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| EESK                     | O    | <b>EEPROM Serial Clock.</b> The EEPROM Shift Clock provides the clock rate for the EEPROM interface, which is approximately 1 MHz for Microwire* and 2 MHz for SPI.                                                                                                                                                                                                                                                                                                                                                             |
| FLSH_CE#                 | O    | <b>Flash Chip Enable Output.</b> Used to enable FLASH device.                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| FLSH_SCK                 | O    | <b>Flash Serial Clock Output.</b> The clock rate of the serial FLASH interface is approximately 1 MHz.                                                                                                                                                                                                                                                                                                                                                                                                                          |
| FLSH_SI                  | O    | <b>Flash Serial Data Input.</b> This pin is an output to the memory device.                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| FLSH_SO/<br>LAN_DISABLE# | I    | <b>Flash Serial Data Output / LAN Disable.</b> This pin is an input from the Flash memory. Alternatively, the pin can be used to disable the LAN port from a system General Purpose Input Output (GPIO) port. It has an internal pullup device. If the 82541ER is not using Flash functionality, the pin should be connected to an external pull-up resistor.<br>If this pin is used as LAN_DISABLE#, the device goes to low power state and the LAN port is disabled when this pin is sampled low on rising edge of PCI reset. |



## 3.4 Miscellaneous Signals

### 3.4.1 LED Signals (4)

| Symbol    | Type | Name and Function                                                                                                |
|-----------|------|------------------------------------------------------------------------------------------------------------------|
| LINK_LED# | O    | <b>LED0 / LINK Up.</b> Programmable LED indication. Defaults to indicate link connectivity.                      |
| ACTIVITY# | O    | <b>LED1 / Activity.</b> Programmable LED indication. Defaults to flash to indicate transmit or receive activity. |
| LINK100#  | O    | <b>LED2 / LINK 100.</b> Programmable LED indication. Defaults to indicate link at 100 Mbps.                      |
| LINK1000# | O    | <b>LED3 / LINK 1000.</b> Programmable LED indication. Defaults to indicate link at 1000 Mbps.                    |

### 3.4.2 Other Signals (4)

| Symbol   | Type | Name and Function                                                                                                                                                                                                                                                                                                                                |
|----------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SDP[3:0] | TS   | <b>Software Defined Pin.</b> The Software Defined Pins are reserved and programmable with respect to input and output capability. These default to input signals upon power-up but may be configured differently by the EEPROM. The upper four bits may be mapped to the General Purpose Interrupt bits if they are configured as input signals. |

## 3.5 PHY Signals

### 3.5.1 Crystal Signals (2)

| Symbol | Type | Name and Function                                                                                                                                                           |
|--------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| XTAL1  | I    | <b>Crystal One.</b> The Crystal One pin is a 25 MHz +/- 50 ppm input signal. It should be connected to a crystal, and the other end of the crystal should connect to XTAL2. |
| XTAL2  | O    | <b>Crystal Two.</b> Crystal Two is the output of an internal oscillator circuit used to drive a crystal into oscillation.                                                   |

### 3.5.2 Analog Signals (10)

| Symbol     | Type | Name and Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MDI[0]+/-  | A    | <b>Media Dependent Interface [0].</b><br><b>1000BASE-T:</b> In MDI configuration, MDI[0]+/- corresponds to BI_DA+/-, and in MDI-X configuration, MDI[0]+/- corresponds to BI_DB+/-.<br><b>100BASE_TX:</b> In MDI configuration, MDI[0]+/- is used for the transmit pair, and in MDI-X configuration, MDI[0]+/- is used for the receive pair.<br><b>10BASE-T:</b> In MDI configuration, MDI[0]+/- is used for the transmit pair, and in MDI-X configuration, MDI[0]+/- is used for the receive pair. |
| MDI[1]+/-  | A    | <b>Media Dependent Interface [1].</b><br><b>1000BASE-T:</b> In MDI configuration, MDI[1]+/- corresponds to BI_DB+/-, and in MDI-X configuration, MDI[1]+/- corresponds to BI_DA+/-.<br><b>100BASE_TX:</b> In MDI configuration, MDI[1]+/- is used for the receive pair, and in MDI-X configuration, MDI[1]+/- is used for the transmit pair.<br><b>10BASE-T:</b> In MDI configuration, MDI[1]+/- is used for the receive pair, and in MDI-X configuration, MDI[1]+/- is used for the transmit pair. |
| MDI[2]+/-  | A    | <b>Media Dependent Interface [2].</b><br><b>1000BASE-T:</b> In MDI configuration, MDI[2]+/- corresponds to BI_DC+/-, and in MDI-X configuration, MDI[2]+/- corresponds to BI_DD+/-.<br><b>100BASE_TX:</b> Unused.<br><b>10BASE-T:</b> Unused.                                                                                                                                                                                                                                                       |
| MDI[3]+/-  | A    | <b>Media Dependent Interface [3].</b><br><b>1000BASE-T:</b> In MDI configuration, MDI[3]+/- corresponds to BI_DC+/-, and in MDI-X configuration, MDI[3]+/- corresponds to BI_DD+/-.<br><b>100BASE_TX:</b> Unused.<br><b>10BASE-T:</b> Unused.                                                                                                                                                                                                                                                       |
| IEEE_TEST- | A    | <b>IEEE test pin output minus.</b> Used to gain access to the internal PHY clock for 1000BASE-T IEEE physical layer conformance testing.                                                                                                                                                                                                                                                                                                                                                            |
| IEEE_TEST+ | A    | <b>Analog test pin output plus.</b> Used to gain access to the internal PHY clock for 1000BASE-T IEEE physical layer conformance testing.                                                                                                                                                                                                                                                                                                                                                           |

### 3.6 Test Interface Signals (6)

| Symbol     | Type | Name and Function                                                                                                                                                                                                                    |
|------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TEST       | I    | <b>Test Enable.</b> Enables test mode.<br>Normal mode: connect to VSS.                                                                                                                                                               |
| JTAG_TCK   | I    | <b>JTAG Test Access Port Clock.</b>                                                                                                                                                                                                  |
| JTAG_TDI   | I    | <b>JTAG Test Access Port Data In.</b>                                                                                                                                                                                                |
| JTAG_TDO   | O    | <b>JTAG Test Access Port Data Out.</b>                                                                                                                                                                                               |
| JTAG_TMS   | I    | <b>JTAG Test Access Port Mode Select.</b>                                                                                                                                                                                            |
| JTAG_TRST# | I    | <b>JTAG Test Access Port Reset.</b> This is an active low reset signal for JTAG. To disable the JTAG interface, this signal should be terminated using a 100 $\Omega$ pull-down resistor to ground. It must not be left unconnected. |

## 3.7 Power Supply Connections

### 3.7.1 Digital and Analog Supplies

| Symbol      | Type | Name and Function                                                  |
|-------------|------|--------------------------------------------------------------------|
| 3.3V        | P    | <b>3.3 V I/O Power Supply.</b>                                     |
| Analog_1.8V | P    | <b>1.8V Analog Power Supply.</b>                                   |
| CLKR_1.8V   | P    | <b>1.8V analog power supply for the clock recovery.</b>            |
| XTAL_1.8V   | P    | <b>Input power for the XTAL regulator.</b>                         |
| 1.2V        | P    | <b>1.2V Power supply.</b> This is for analog and digital circuits. |
| Analog_1.2V | P    | <b>1.2V Analog Power Supply.</b>                                   |
| PLL_1.2V    | P    | <b>Input power for the ICS regulator.</b>                          |

### 3.7.2 Grounds, Reserved Pins and No Connects

| Symbol   | Type | Name and Function                                                                                                                                                                                             |
|----------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VSS      | P    | <b>Ground.</b>                                                                                                                                                                                                |
| AVSS     | P    | <b>Shared analog Ground.</b>                                                                                                                                                                                  |
| RSVD_VSS | P    | <b>Reserved Ground.</b> This pin is reserved by Intel and may have factory test functions. For normal operation, connect to ground.                                                                           |
| RSVD_NC  | P    | <b>Reserved No connect.</b> This pin is reserved by Intel and may have factory test functions. For normal operation, do not connect any circuit to these pins. Do not connect pull-up or pull-down resistors. |
| NC       | P    | <b>No Connect.</b> This pin is not connected internally.                                                                                                                                                      |
| RSVD_VCC | P    | <b>Reserved VCC.</b> This pin is reserved by Intel and may have factory test functions. For normal operation, connect to VCC through a 1K pull-up resistor                                                    |

### 3.7.3 Voltage Regulation Control Signals (2)

| Symbol | Type | Name and Function                                                                                                                                                                                                                                                                          |
|--------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CTRL12 | A    | <b>1.2V Control.</b> LDO voltage regulator output to drive external PNP pass transistor. If 1.2V is already present in the system, leave output unconnected. To achieve optimal D3 power consumption, leave the output unconnected and use a high-efficiency external switching regulator. |
| CTRL18 | A    | <b>1.8V Control.</b> LDO voltage regulator output to drive external PNP pass transistor. If 1.8V is already present in the system, leave output unconnected. To achieve optimal D3 power consumption, leave the output unconnected and use a high-efficiency external switching regulator. |

**Note:** This page intentionally left blank.

## 4.0 Voltage, Temperature, and Timing Specifications

### 4.1 Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings<sup>a</sup>

| Symbol    | Parameter                                                                                        | Min       | Max                                 | Unit |
|-----------|--------------------------------------------------------------------------------------------------|-----------|-------------------------------------|------|
| VDD (3.3) | DC supply voltage on 3.3 V pins with respect to VSS                                              | VSS - 0.5 | 4.6                                 | V    |
| VDD (1.8) | DC supply voltage on 1.8 V pins with respect to VSS                                              | VSS - 0.5 | 2.5 or VDD (1.8) + 0.5 <sup>b</sup> | V    |
| VDD (1.2) | DC supply voltage on 1.2V pins with respect to VSS                                               | VSS - 0.5 | 1.7 or VDD (1.2) + 0.5 <sup>c</sup> | V    |
| VDD       | DC supply voltage                                                                                | VSS - 0.5 | 4.6                                 | V    |
| VI / VO   | LVTTTL input voltage                                                                             | VSS - 0.5 | 4.6 <sup>d</sup>                    | V    |
| IO        | Output current                                                                                   |           | 40                                  | mA   |
| TSTG      | Storage temperature range                                                                        | -40       | 125                                 | °C   |
|           | ESD per MIL-STD-883 Test Method 3015, Specification 2001V Latchup Over/Undershoot: 150 mA, 125 C |           | VDD overstress: VDD (3.3) * 7.2     | V    |

- a. Maximum ratings are referenced to ground (VSS). Permanent device damage is likely to occur if the ratings in this table are exceeded. These values should not be used as the limits for normal device operations.
- b. The maximum value is the lesser value of 2.5V or VDD (2.5) + 0.5 V. This specification applies to biasing the device to a steady state for an indefinite duration.
- c. The maximum value is the lesser value of 1.7 V or VDD (2.5) + 0.5 V.
- d. The maximum value must also be less than VIO.

### 4.2 Targeted Recommended Operating Conditions

#### 4.2.1 General Operating Conditions

Table 2. Recommended Operating Conditions (Sheet 1 of 2)<sup>a</sup>

| Symbol    | Parameter                           | Min               | Max               | Unit |
|-----------|-------------------------------------|-------------------|-------------------|------|
| VDD (3.3) | DC supply voltage on 3.3 V pins     | 3.0               | 3.6               | V    |
| VDD (1.8) | DC supply voltage on 1.8 V pins     | 1.71 <sup>b</sup> | 1.89 <sup>c</sup> | V    |
| VDD (1.2) | DC supply voltage on 1.2 V pins     | 1.14 <sup>d</sup> | 1.26 <sup>e</sup> | V    |
| VIO       | PCI bus reference voltage           | 3.0               | 5.25              | V    |
| tR / tF   | Input rise/fall time (normal input) | 0                 | 200               | ns   |

Table 2. Recommended Operating Conditions (Sheet 2 of 2)<sup>a</sup>

| Symbol         | Parameter                             | Min | Max  | Unit |
|----------------|---------------------------------------|-----|------|------|
| tr/ff          | input rise/fall time (Schmitt input)  | 0   | 10   | ms   |
| T <sub>A</sub> | Operating temperature range (ambient) | 0   | 70   | °C   |
| T <sub>J</sub> | Junction temperature                  |     | ≤125 | °C   |

- a. Sustained operation of the device at conditions exceeding these values, even if they are within the absolute maximum rating limits, might result in permanent damage.
- b. The value listed in this table is for external voltage regulation. If the internal voltage regulator is used, the minimum value is 1.67 V.
- c. The value listed in this table is for external voltage regulation. If the internal voltage regulator is used, the maximum value is 1.926 V.
- d. The value listed in this table is for external voltage regulation. If the internal voltage regulator is used, the minimum value is 1.12 V.
- e. The value listed in this table is for external voltage regulation. If the internal voltage regulator is used, the maximum value is 1.284 V.

## 4.2.2 Voltage Ramp and Sequencing Recommendations

**Note:** In any case or time period (greater than 1 ns), the supply voltage should comply with 3.3V > 1.8V > 1.2V. This is important to avoid stress in the ESD protection circuits. After 3.3V reaches 10% of its final value, all voltage rails (1.8V and 1.2V) have 150 ms to reach their final operating values.

Table 3. 3.3V Supply Voltage Ramp

| Parameter         | Description                                           | Min | Max   | Unit |
|-------------------|-------------------------------------------------------|-----|-------|------|
| Rise Time         | Time from 10% to 90% mark                             | 0.1 | 100   | ms   |
| Monotonicity      | Voltage dip allowed in ramp                           |     | 0     | mV   |
| Slope             | Ramp rate at any time between 10% to 90%              |     | 28800 | V/s  |
| Operational Range | Voltage range for normal operating conditions         | 3   | 3.6   | V    |
| Ripple            | Maximum voltage ripple at a bandwidth equal to 50 MHz |     | 70    | mV   |
| Overshoot         | Maximum voltage allowed                               |     | 4     | V    |

Table 4. 1.8V Supply Voltage Ramp

| Symbol            | Parameter                                                          | Min   | Max   | Unit |
|-------------------|--------------------------------------------------------------------|-------|-------|------|
| Rise Time         | Time from 10% to 90% mark                                          | 0.1   | 100   | ms   |
| Monotonicity      | Voltage dip allowed in ramp                                        |       | 0     | mV   |
| Slope             | Ramp rate at any time between 10% to 90%                           |       | 57600 | V/s  |
| Operational Range | Voltage range for normal operating conditions (PNP's) <sup>a</sup> | 1.674 | 1.89  | V    |
| Operational Range | Voltage range for normal operating conditions (PNP's)              | -7    | 5     | %    |
| Operational Range | Voltage range for normal operating conditions (external regulator) | 1.71  | 1.89  | V    |
| Operational Range | Voltage range for normal operating conditions (external regulator) | -5    | 5     | %    |

**Table 4. 1.8V Supply Voltage Ramp**

|                    |                                                                 |     |     |    |
|--------------------|-----------------------------------------------------------------|-----|-----|----|
| Ripple             | Maximum voltage ripple at a bandwidth equal to 50 MHz           |     | 20  | mV |
| Overshoot          | Maximum voltage allowed                                         |     | 2.2 | V  |
| Output Capacitance | Capacitance range when using PNP circuit                        | 4.7 | 20  | μF |
| Input Capacitance  | Capacitance range when using PNP circuit                        | 4.7 | 20  | μF |
| Capacitance ESR    | Equivalent series resistance of output capacitance <sup>b</sup> | 5   | 100 | mΩ |
| Ictrl_18           | Maximum output current rating to CTRL18                         |     | 20  | mA |

- a. Operating with an internal regulator (PNP) supports a wider tolerance output voltage due to process tracking.  
b. Tantalum capacitors must not be used.

**Table 5. 1.2V Supply Voltage Ramp**

| Symbol             | Parameter                                                          | Min   | Max   | Unit |
|--------------------|--------------------------------------------------------------------|-------|-------|------|
| Rise Time          | Time from 10% to 90% mark                                          | 0.025 |       | ms   |
| Monotonicity       | Voltage dip allowed in ramp                                        |       | 0     | mV   |
| Slope              | Ramp rate at any time between 10% to 90%                           |       | 38400 | V/s  |
| Operational Range  | Voltage range for normal operating conditions (PNP's) <sup>a</sup> | 1.116 | 1.26  | V    |
| Operational Range  | Voltage range for normal operating conditions (PNP's)              | -7    | 5     | %    |
| Operational Range  | Voltage range for normal operating conditions (external regulator) | 1.14  | 1.26  | V    |
| Operational Range  | Voltage range for normal operating conditions (external regulator) | -5    | 5     | %    |
| Ripple             | Maximum voltage ripple at a bandwidth equal to 50 MHz              |       | 20    | mV   |
| Overshoot          | Maximum voltage allowed                                            |       | 1.45  | V    |
| Output Capacitance | Capacitance range when using PNP circuit                           | 4.7   | 20    | μF   |
| Input Capacitance  | Capacitance range when using PNP circuit                           | 4.7   | 20    | μF   |
| Capacitance ESR    | Equivalent series resistance of output capacitance <sup>b</sup>    | 5     | 100   | mΩ   |
| Ictrl_12           | Maximum output current rating to CTRL_12                           |       | 20    | mA   |

- a. Operating with an internal regulator (PNP) supports a wider tolerance output voltage due to process tracking.  
b. Tantalum capacitors must not be used.

## 4.3 DC Specifications

**Table 6. DC Characteristics**

| Symbol    | Parameter                       | Condition | Min               | Typ | Max               | Units |
|-----------|---------------------------------|-----------|-------------------|-----|-------------------|-------|
| VDD (3.3) | DC supply voltage on 3.3 V pins |           | 3.00              | 3.3 | 3.60              | V     |
| VDD (1.8) | DC supply voltage on 1.8 V pins |           | 1.71 <sup>a</sup> | 1.8 | 1.89 <sup>b</sup> | V     |
| VDD (1.2) | DC supply voltage on 1.2 V pins |           | 1.14 <sup>c</sup> | 1.2 | 1.26 <sup>d</sup> | V     |

- a. The value listed in this table is for external voltage regulation. If the internal voltage regulator is used, the minimum value is 1.67 V.
- b. The value listed in this table is for external voltage regulation. If the internal voltage regulator is used, the maximum value is 1.926 V.
- c. The value listed in this table is for external voltage regulation. If the internal voltage regulator is used, the minimum value is 1.12 V.
- d. The value listed in this table is for external voltage regulation. If the internal voltage regulator is used, the maximum value is 1.284 V.

**Table 7. Power Specifications - D0a**

|                           | D0a                       |                           |                           |                           |                           |                           |                           |                           |
|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|
|                           | unplugged no link         |                           | @10 Mbps                  |                           | @100 Mbps                 |                           | @ 1000 Mbps               |                           |
|                           | Typ Icc (mA) <sup>a</sup> | Max Icc (mA) <sup>b</sup> | Typ Icc (mA) <sup>a</sup> | Max Icc (mA) <sup>b</sup> | Typ Icc (mA) <sup>a</sup> | Max Icc (mA) <sup>b</sup> | Typ Icc (mA) <sup>a</sup> | Max Icc (mA) <sup>b</sup> |
| 3.3V                      | 3                         | 5                         | 5                         | 10                        | 13                        | 15                        | 30                        | 40                        |
| 1.8V                      | 14                        | 15                        | 85                        | 85                        | 110                       | 115                       | 315                       | 320                       |
| 1.2V                      | 30                        | 35                        | 85                        | 90                        | 90                        | 100                       | 380                       | 400                       |
| <b>Total Device Power</b> | 75 mW                     |                           | 270 mW                    |                           | 355 mW                    |                           | 1.1 W                     | 1.2 W                     |

- a. Typical conditions: operating temperature ( $T_A$ ) = 25 C, nominal voltages, moderate network traffic at full duplex, and PCI 33 MHz system interface.
- b. Maximum conditions: minimum operating temperature ( $T_A$ ) values, maximum voltage values, continuous network traffic at full duplex, and PCI 33 MHz system interface.

**Table 8. Power Specifications - D3cold**

|      | D3cold - wake-up enabled <sup>a</sup> |                           |                           |                           |                           |                           | D3cold-wake disabled      |                           |
|------|---------------------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|
|      | unplugged link                        |                           | @10 Mbps                  |                           | @100 Mbps                 |                           |                           |                           |
|      | Typ Icc (mA) <sup>b</sup>             | Max Icc (mA) <sup>c</sup> | Typ Icc (mA) <sup>a</sup> | Max Icc (mA) <sup>b</sup> | Typ Icc (mA) <sup>a</sup> | Max Icc (mA) <sup>b</sup> | Typ Icc (mA) <sup>a</sup> | Max Icc (mA) <sup>b</sup> |
| 3.3V | 2                                     | 3                         | 2                         | 3                         | 2                         | 3                         | 4                         | 5                         |



**Table 8. Power Specifications - D3cold**

|                    | D3cold - wake-up enabled <sup>a</sup> |                           |                           |                           |                           |                           | D3cold-wake disabled      |                           |
|--------------------|---------------------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|
|                    | unplugged link                        |                           | @10 Mbps                  |                           | @100 Mbps                 |                           |                           |                           |
|                    | Typ Icc (mA) <sup>b</sup>             | Max Icc (mA) <sup>c</sup> | Typ Icc (mA) <sup>a</sup> | Max Icc (mA) <sup>b</sup> | Typ Icc (mA) <sup>a</sup> | Max Icc (mA) <sup>b</sup> | Typ Icc (mA) <sup>a</sup> | Max Icc (mA) <sup>b</sup> |
| 1.8V               | 14                                    | 15                        | 20                        | 25                        | 110                       | 115                       | 1                         | 2                         |
| 1.2V               | 21                                    | 25                        | 30                        | 35                        | 80                        | 85                        | 7                         | 10                        |
| Total Device Power | 60 mW                                 |                           | 80 mW                     |                           | 305 mW                    |                           | 25 mW                     |                           |

- a. The power consumption for 1000 Mbps is not shown since the controller moves to the 10/100 Mbps mode before going into the D3 state to conserve power.
- b. Typical conditions: operating temperature (T<sub>A</sub>) = 25 C, nominal voltages, moderate network traffic at full duplex, and PCI 33 MHz system interface.
- c. Maximum conditions: minimum operating temperature (T<sub>A</sub>) values, maximum voltage values, continuous network traffic at full duplex, and PCI 33 MHz system interface.

**Table 9. Power Specifications D(r) Uninitialized**

|                    | D(r) Uninitialized (FLSH_SO/LAN_DISABLE # = 0) |              |
|--------------------|------------------------------------------------|--------------|
|                    | Typ Icc (mA)                                   | Max Icc (mA) |
| 3.3V               | 5                                              | 10           |
| 1.8V               | 1                                              | 2            |
| 1.2V               | 12                                             | 15           |
| Total Device Power | 35 mW                                          |              |

**Table 10. Power Specifications - Complete Subsystem**

|       | Complete Subsystem (Reference Design) Including Magnetics, LED, Regulator Circuits |                           |                               |                           |                           |                           |                           |                           |                           |                           |
|-------|------------------------------------------------------------------------------------|---------------------------|-------------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|
|       | D3cold - wake disabled                                                             |                           | D3cold wake-enabled @ 10 Mbps |                           | D0 @10 Mbps active        |                           | D0 @100 Mbps active       |                           | D0 @ 1000 Mbps active     |                           |
|       | Typ Icc (mA) <sup>a</sup>                                                          | Max Icc (mA) <sup>b</sup> | Typ Icc (mA) <sup>a</sup>     | Max Icc (mA) <sup>b</sup> | Typ Icc (mA) <sup>a</sup> | Max Icc (mA) <sup>b</sup> | Typ Icc (mA) <sup>a</sup> | Max Icc (mA) <sup>b</sup> | Typ Icc (mA) <sup>a</sup> | Max Icc (mA) <sup>b</sup> |
| 3.3 V | 4                                                                                  | 5                         | 7                             | 10                        |                           |                           | 12                        | 15                        | 33                        | 45                        |

Table 10. Power Specifications - Complete Subsystem

|                        | Complete Subsystem (Reference Design) Including Magnetics, LED, Regulator Circuits |                           |                               |                           |                           |                           |                           |                           |                           |                           |
|------------------------|------------------------------------------------------------------------------------|---------------------------|-------------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|
|                        | D3cold - wake disabled                                                             |                           | D3cold wake-enabled @ 10 Mbps |                           | D0 @10 Mbps active        |                           | D0 @100 Mbps active       |                           | D0 @ 1000 Mbps active     |                           |
|                        | Typ Icc (mA) <sup>a</sup>                                                          | Max Icc (mA) <sup>b</sup> | Typ Icc (mA) <sup>a</sup>     | Max Icc (mA) <sup>b</sup> | Typ Icc (mA) <sup>a</sup> | Max Icc (mA) <sup>b</sup> | Typ Icc (mA) <sup>a</sup> | Max Icc (mA) <sup>b</sup> | Typ Icc (mA) <sup>a</sup> | Max Icc (mA) <sup>b</sup> |
| 1.8 V                  | 1                                                                                  | 7                         | 2                             | 30                        |                           |                           | 35                        | 135                       | 140                       | 410                       |
| 1.2 V                  |                                                                                    | 7                         | 10                            | 30                        |                           |                           | 35                        | 80                        | 85                        | 380                       |
| Subsystem 3.3V Current |                                                                                    | 10                        |                               | 40                        |                           |                           |                           | 120                       |                           | 710                       |

a. Typical conditions: operating temperature ( $T_A$ ) = 25 °C, nominal voltages, moderate network traffic at full duplex, and PCI 33 MHz system interface.

b. Maximum conditions: minimum operating temperature ( $T_A$ ) values, maximum voltage values, continuous network traffic at full duplex, and PCI 33 MHz system interface.

Table 11. I/O Characteristics (Sheet 1 of 2)

| Symbol | Parameter                                      | Condition                                | Min                                | Typ | Max                        | Units   |
|--------|------------------------------------------------|------------------------------------------|------------------------------------|-----|----------------------------|---------|
| VIH    | Input high voltage                             | 3.3 V PCI                                | $0.5 * V_{DD}(3.3)$                |     | $V_{DD}(3.3)$ or VIO       | V       |
| VIL    | Input low voltage                              | 3.3 V PCI <sup>a</sup>                   | VSS                                |     | $0.3 * V_{DD}(3.3)$        | V       |
| IIN    | Input current                                  | $0 < V_{IN} < V_{DD}(3.3)$               | -10                                |     | 10                         | $\mu A$ |
|        | Input with pull-down resistor (50 K $\Omega$ ) | $V_{IN} = V_{DD}(3.3)$                   | 28                                 |     | 191                        |         |
|        | Inputs with pull-up resistor (50 K $\Omega$ )  | $V_{IN} = V_{SS}$                        | -28                                |     | -191                       |         |
| IOL    | Output low current                             | 3.3 V PCI                                |                                    |     | 2.09                       | mA      |
|        |                                                | $0 \leq V_{OUT} \leq 3.6V$               |                                    |     | $100 * V_{OUT}$            |         |
|        |                                                | $0 \leq V_{OUT} \leq 1.3V$               | $48 * V_{OUT}$                     |     |                            |         |
|        |                                                | $1.3V \leq V_{OUT} \leq 3.6V$            | $5.7 * V_{OUT} + 55$               |     |                            |         |
| IOH    | Output high current:                           | $0 \leq (V_{DD} - V_{OUT}) \leq 3.6V$    |                                    |     | $-74 * (V_{DD} - V_{OUT})$ | mA      |
|        |                                                | $0 \leq (V_{DD} - V_{OUT}) \leq 1.2V$    | $-32 * (V_{DD} - V_{OUT})$         |     |                            |         |
|        |                                                | $1.2V \leq (V_{DD} - V_{OUT}) \leq 1.9V$ | $-11 * (V_{DD} - V_{OUT}) - 25.2$  |     |                            |         |
|        |                                                | $1.9V \leq (V_{DD} - V_{OUT}) \leq 3.6V$ | $-1.8 * (V_{DD} - V_{OUT}) - 42.7$ |     |                            |         |
| VOH    | Output high voltage:<br>3.3 V PCI              | IOH = -500 mA                            | $0.9 * V_{DD}(3.3)$                |     |                            | V       |

**Table 11. I/O Characteristics (Sheet 2 of 2) (Continued)**

| Symbol | Parameter                        | Condition                        | Min | Typ | Max            | Units |
|--------|----------------------------------|----------------------------------|-----|-----|----------------|-------|
| VOL    | Output low voltage:<br>3.3 V PCI | IOL = 1500 mA                    |     |     | 0.1 * VDD(3.3) | V     |
| IOZ    | Off-state output leakage current | VO = VDD or VSS                  | -10 |     | 10             | μA    |
| IOS    | Output short circuit current     |                                  |     |     | -250           | mA    |
| CIN    | Input capacitance <sup>b</sup>   | Input and bi-directional buffers |     | 8   |                | pF    |

- a. The maximum VIL is 0.6 V for the following Pins: A13, C5, C8, J4, L7, L12, L13, M8, M12, M13, N10, N11, N13, N14, P9, and P13.  
b. V<sub>DD</sub> (3.3) = 0 V; T<sub>A</sub> = 25 °C; f = 1 Mhz

## 4.4 AC Characteristics

**Table 12. AC Characteristics: 3.3 V Interfacing**

| Symbol | Parameter                   | Min | Typ | Max | Unit |
|--------|-----------------------------|-----|-----|-----|------|
| PCICLK | Clock frequency in PCI mode |     |     | 66  | MHz  |

**Table 13. 25 MHz Clock Input Requirements**

| Symbol | Parameter                                | Specifications |     |     | Units |
|--------|------------------------------------------|----------------|-----|-----|-------|
|        |                                          | Min            | Typ | Max |       |
| f0     | Frequency                                |                | 25  |     | MHz   |
| df0    | Frequency variation                      | -50            |     | +30 | ppm   |
| Dc     | Duty cycle                               | 40             |     | 60  | %     |
| tr     | Rise time                                |                |     | 5   | ns    |
| tf     | Fall time                                |                |     | 5   | ns    |
| Jptp   | Clock jitter (peak-to-peak) <sup>a</sup> |                |     | 250 | ps    |
| Cin    | Input capacitance                        |                | 20  |     | pF    |
| T      | Operating temperature                    |                |     | 70  | ° C   |
| Aptp   | Input clock amplitude (peak-to-peak)     | 1.0            | 1.2 | 1.3 | V     |
| Vcm    | Clock common mode                        |                | 0.6 |     | V     |

- a. Clock jitter is defined according to the recommendations of part 40.6.1.2.5 IEEE 1000BASE-T Standard (at least 10<sup>5</sup> clock edges, filtered by HPF with cut off frequency 5000 Hz).

**Table 14. Reference Crystal Specification Requirements**

| Specification         | Value                     |
|-----------------------|---------------------------|
| Vibrational Mode      | Fundamental               |
| Nominal Frequency     | 25.000 MHz at 25° C       |
| Frequency Tolerance   | ±30 ppm                   |
| Temperature Stability | ±30 ppm at 0° C to 70° C  |
| Calibration Mode      | Parallel                  |
| Load Capacitance      | 20 pF to 24 pF            |
| Shunt Capacitance     | 6 pF maximum              |
| Series Resistance, Rs | 50 W maximum              |
| Drive Level           | 0.5 mW maximum            |
| Aging                 | ±5.0 ppm per year maximum |
| Insulation Resistance | 500 MΩ at DC 100 V        |

**Table 15. Link Interface Clock Requirements**

| Symbol            | Parameter         | Min | Typ | Max | Unit |
|-------------------|-------------------|-----|-----|-----|------|
| fGTX <sup>a</sup> | GTX_CLK frequency |     | 125 |     | MHz  |

a. GTX\_CLK is used externally for test purposes only.

**Table 16. EEPROM Interface Clock Requirements**

| Symbol | Parameter              | Min | Typ | Max | Unit |
|--------|------------------------|-----|-----|-----|------|
| fSK    | Microwire EEPROM Clock |     |     | 1   | MHz  |
|        | SPI EEPROM Clock       |     |     | 2   | MHz  |

**Table 17. AC Test Loads for General Output Pins**

| Symbol | Signal Name | Value | Units |
|--------|-------------|-------|-------|
| CL     | TDO         | 10    | pF    |
| CL     | SDP[3:0]    | 16    | pF    |
| CL     | EEDI, EESK  | 18    | pF    |
| CL     | LED[3:0]    | 20    | pF    |

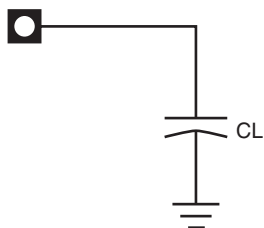


Figure 2. AC Test Loads for General Output Pins

## 4.5 Timing Specifications

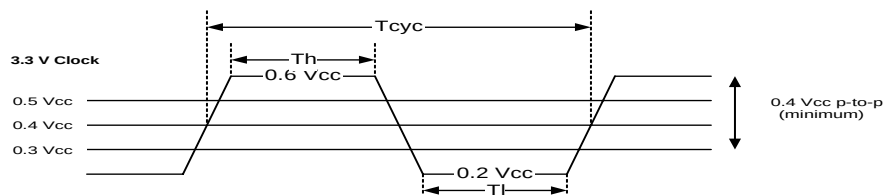
### 4.5.1 PCI Bus Interface

#### 4.5.1.1 PCI Bus Interface Clock

Table 18. PCI Bus Interface Clock Parameters

| Symbol | Parameter <sup>a</sup>      | PCI 66 MHz |     | PCI 33 MHz |     | Units |
|--------|-----------------------------|------------|-----|------------|-----|-------|
|        |                             | Min        | Max | Min        | Max |       |
| TCYC   | CLK cycle time              | 15         | 30  | 30         |     | ns    |
| TH     | CLK high time               | 6          |     | 11         |     | ns    |
| TL     | CLK low time                | 6          |     | 11         |     | ns    |
|        | CLK slew rate               | 1.5        | 4   | 1          | 4   | V/ns  |
|        | RST# slew rate <sup>b</sup> | 50         |     | 50         |     | mV/ns |

- a. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform as shown.
- b. The minimum RST# slew rate applies only to the rising (de-assertion) edge of the reset signal and ensures that system noise cannot render a monotonic signal to appear bouncing in the switching range.



PCI Clock Timing.vsd

Figure 3. PCI Clock Timing

## 4.5.1.2 PCI/PCI-X Bus Interface Timing

Table 19. PCI Bus Interface Timing Parameters

| Symbol    | Parameter                                         | PCI 66MHz |     | PCI 33 MHz |     | Units |
|-----------|---------------------------------------------------|-----------|-----|------------|-----|-------|
|           |                                                   | Min       | Max | Min        | Max |       |
| TVAL      | CLK to signal valid delay: bussed signals         | 2         | 6   | 2          | 11  | ns    |
| TVAL(ptp) | CLK to signal valid delay: point-to-point signals | 2         | 6   | 2          | 12  | ns    |
| TON       | Float to active delay                             | 2         |     | 2          |     | ns    |
| TOFF      | Active to float delay                             |           | 14  |            | 28  | ns    |
| TSU       | Input setup time to CLK: bussed signals           | 3         |     | 7          |     | ns    |
| TSU(ptp)  | Input setup time to CLK: point-to-point signals   | 5         |     | 10, 12     |     | ns    |
| TH        | Input hold time from CLK                          | 0         |     | 0          |     | ns    |

**NOTES:**

1. Output timing measurements are as shown.
2. REQ# and GNT# signals are point-to-point and have different output valid delay and input setup times than bussed signals. GNT# has a setup of 10 ns; REQ# has a setup of 12 ns. All other signals are bussed.
3. Input timing measurements are as shown.

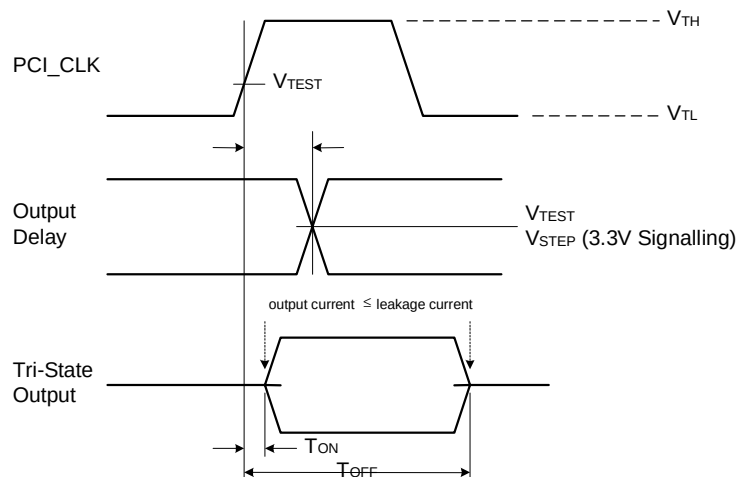


Figure 4. PCI Bus Interface Output Timing Measurement

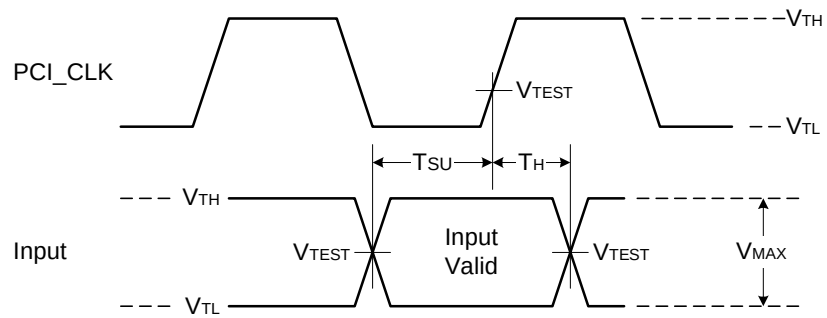


Figure 5. PCI Bus Interface Input Timing Measurement Conditions

Table 20. PCI Bus Interface Timing Measurement Conditions

| Symbol            | Parameter                             | PCI 66 MHz<br>3.3 v   | Unit |
|-------------------|---------------------------------------|-----------------------|------|
| V <sub>TH</sub>   | Input measurement test voltage (high) | 0.6 * V <sub>CC</sub> | V    |
| V <sub>TL</sub>   | Input measurement test voltage (low)  | 0.2 * V <sub>CC</sub> | V    |
| V <sub>TEST</sub> | Output measurement test voltage       | 0.4 * V <sub>CC</sub> | V    |
|                   | Input signal slew rate                | 1.5                   | V/ns |

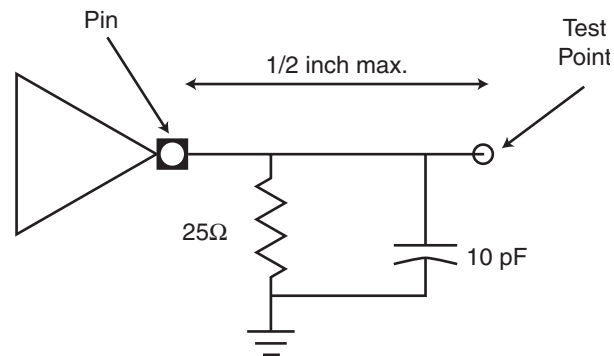


Figure 6. TVAL (max) Rising Edge Test Load

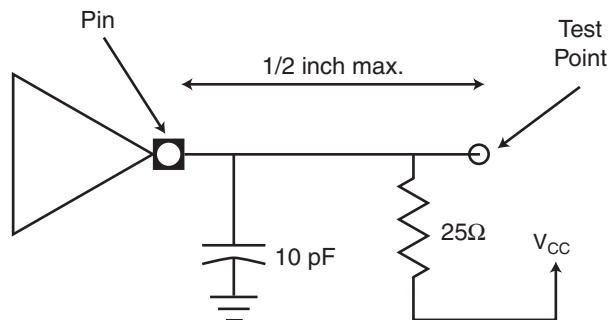


Figure 7. TVAL (max) Falling Edge Test Load

Figure 8. TVAL (min) Test Load

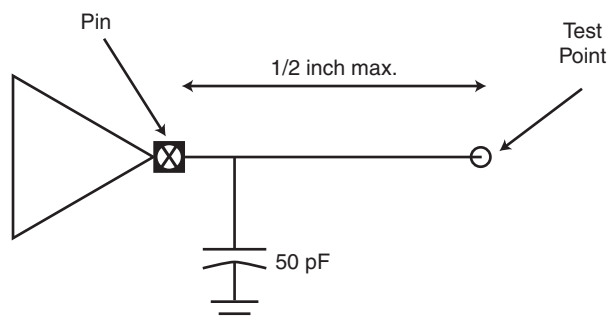


Figure 9. TVAL Test Load (PCI 5 V Signaling Environment)

**NOTE:** Note: 50 pF load used for maximum times. Minimum times are specified with 0 pF load.



## 4.5.2 Link Interface Timing

Table 21. Rise and Fall Times

| Symbol | Parameter       | Condition      | Min | Max | Unit |
|--------|-----------------|----------------|-----|-----|------|
| TR     | Clock rise time | 0.8 V to 2.0 V | 0.7 |     | ns   |
| TF     | Clock fall time | 2.0 V to 0.8 V | 0.7 |     | ns   |
| TR     | Data rise time  | 0.8 to 2.0 V   | 0.7 |     | ns   |
| TF     | Data fall time  | 2.0 V to 0.8 V | 0.7 |     | ns   |

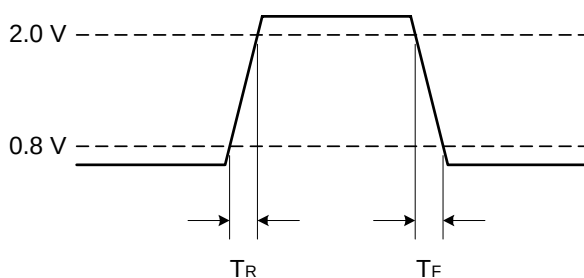


Figure 10. Link Interface Rise/Fall Timing

## 4.5.3 EEPROM Interface

Table 22. Link Interface Clock Requirements

| Symbol | Parameter <sup>a</sup>     | Min | Typ                              | Max | Unit |
|--------|----------------------------|-----|----------------------------------|-----|------|
| TPW    | Microwire EESK pulse width |     | $T_{PERIOD} \times \frac{X}{64}$ |     | ns   |
|        | SPI EESK pulse width       |     | $T_{PERIOD} \times \frac{X}{32}$ |     | ns   |

a. The EEPROM clock is derived from a 125 MHz internal clock.

Table 23. Link Interface Clock Requirements

| Symbol | Parameter <sup>a</sup> | Min    | Typ | Max | Unit |
|--------|------------------------|--------|-----|-----|------|
| TDOS   | EEDO setup time        | TCYC*2 |     |     | ns   |
| TDOH   | EEDO hold time         | 0      |     |     | ns   |

a. The EE\_DO setup and hold time is a function of the PCI bus clock cycle time but is referenced to O\_EE\_SK.



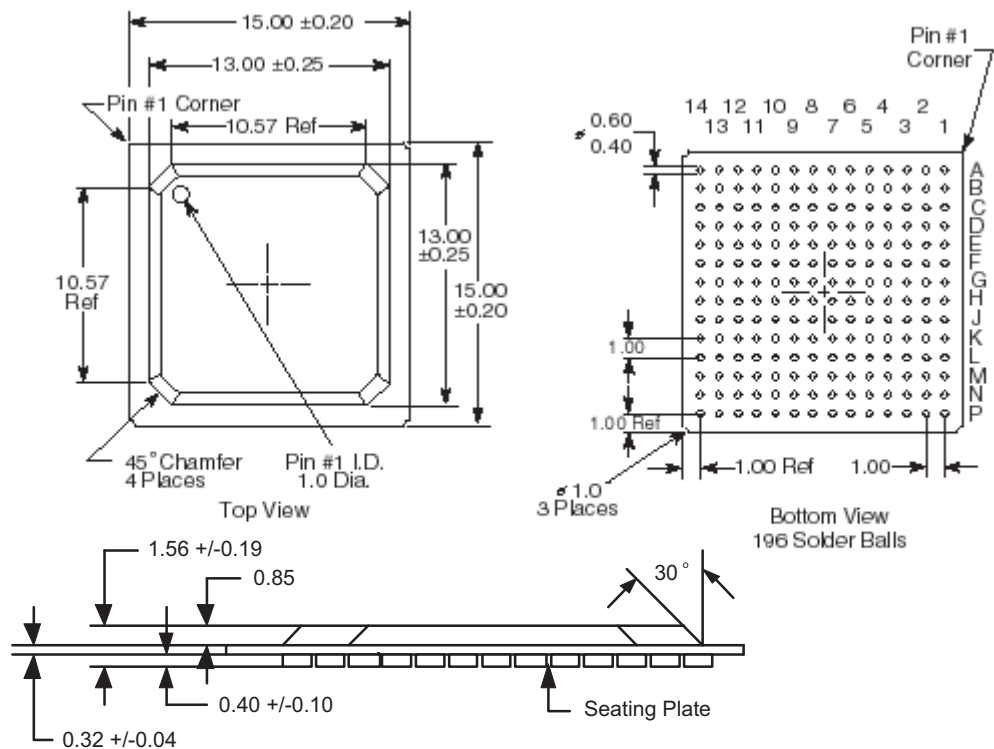
**Note:** This page is intentionally left blank.

## 5.0 Package and Pinout Information

This section describes the device physical characteristics. The pin number-to-signal mapping is indicated beginning with Table 25.

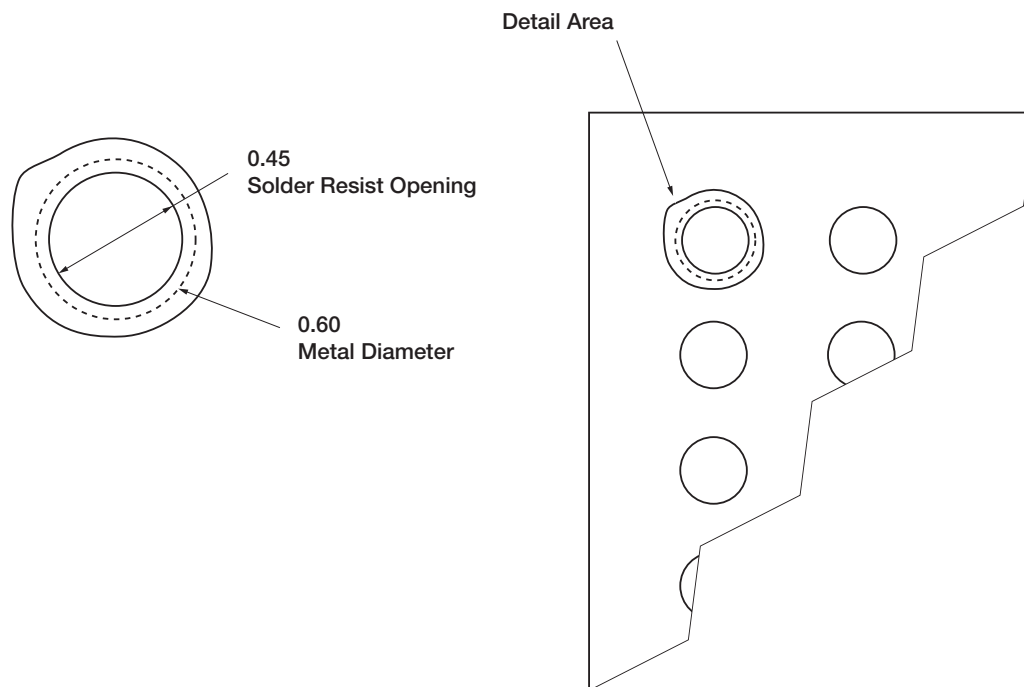
### 5.1 Package Information

The 82541ER device is a 196-lead plastic ball grid array (BGA) measuring 15 mm by 15mm. The package dimensions are detailed below. The nominal ball pitch is 1 mm.



**Figure 11. 82541ER Mechanical Specifications**

**Note:** No changes to existing soldering processes are needed for the 0.32 mm substrate change.



**Figure 12. 196 PBGA Package Pad Detail**

As illustrated in Figure 12, the Ethernet controller package uses solder mask defined pads. The copper area is 0.60 mm and the opening in the solder mask is 0.45mm. The nominal ball sphere diameter is 0.50 mm.

## 5.2 Thermal Specifications

The 82541ER device is specified for operation when the ambient temperature ( $T_A$ ) is within the range of 0° C to 70° C.

$T_C$  (case temperature) is calculated using the equation:

$$T_C = T_A + P (\theta_{JA} - \theta_{JC})$$

$T_J$  (junction temperature) is calculated using the equation:

$$T_J = T_A + P \theta_{JA}$$

$P$  (power consumption) is calculated by using the typical  $I_{CC}$  and nominal  $V_{CC}$ . The preliminary thermal resistances are shown in Table 24.

**Table 24. Thermal Characteristics**

| Symbol        | Parameter                               | Preliminary Value at specified airflow (m/s) |      |      | Units  |
|---------------|-----------------------------------------|----------------------------------------------|------|------|--------|
|               |                                         | 0                                            | 1    | 2    |        |
| $\theta_{JA}$ | Thermal resistance, junction-to-ambient | 29                                           | 25.0 | 23.5 | C/Watt |
| $\theta_{JC}$ | Thermal resistance, junction-to-case    | 11.1                                         | 11.1 | 11.1 | C/Watt |

Thermal resistances are determined empirically with test devices mounted on standard thermal test boards. Real system designs may have different characteristics due to board thickness, arrangement of ground planes, and proximity of other components. The case temperature measurements should be used to assure that the 82541ER device is operating under recommended conditions.

## 5.3 Pinout Information

**Table 25. PCI Address, Data and Control Signals**

| Signal | Pin | Signal | Pin | Signal   | Pin |
|--------|-----|--------|-----|----------|-----|
| AD[0]  | N7  | AD[16] | K1  | C/BE#[0] | M4  |
| AD[1]  | M7  | AD[17] | E3  | C/BE#[1] | L3  |
| AD[2]  | P6  | AD[18] | D1  | C/BE#[2] | F3  |
| AD[3]  | P5  | AD[19] | D2  | C/BE#[3] | C4  |
| AD[4]  | N5  | AD[20] | D3  | PAR      | J1  |
| AD[5]  | M5  | AD[21] | C1  | FRAME#   | F2  |
| AD[6]  | P4  | AD[22] | B1  | IRDY#    | F1  |
| AD[7]  | N4  | AD[23] | B2  | TRDY#    | G3  |
| AD[8]  | P3  | AD[24] | B4  | STOP#    | H1  |
| AD[9]  | N3  | AD[25] | A5  | DEVSEL#  | H3  |
| AD[10] | N2  | AD[26] | B5  | IDSEL    | A4  |
| AD[11] | M1  | AD[27] | B6  | VIO      | G2  |
| AD[12] | M2  | AD[28] | C6  |          |     |
| AD[13] | M3  | AD[29] | C7  |          |     |
| AD[14] | L1  | AD[30] | A8  |          |     |
| AD[15] | L2  | AD[31] | B8  |          |     |

**Table 26. PCI Arbitration Signals**

| Signal | Pin |
|--------|-----|
| REQ#   | C3  |
| GNT#   | J3  |

**Table 27. Interrupt Signals**

| Signal | Pin |
|--------|-----|
| INTA#  | H2  |

**Table 28. System Signals**

| Signal | Pin | Signal | Pin |
|--------|-----|--------|-----|
| CLK    | G1  | RST#   | B9  |
| M66EN  | C2  |        |     |

**Table 29. Error Reporting Signals**

| Signal | Pin | Signal | Pin |
|--------|-----|--------|-----|
| SERR#  | A2  | PERR#  | J2  |

**Table 30. Power Management Signals**

| Signal       | Pin |
|--------------|-----|
| LAN_PWR_GOOD | A9  |
| AUX_PWR      | J12 |

**Table 31. Serial EEPROM Interface Signals**

| Signal | Pin | Signal | Pin | Signal | Pin |
|--------|-----|--------|-----|--------|-----|
| EESK   | M10 | EEDI   | P10 | EECS   | P7  |
| EEDO   | N10 | EEMODE | J4  |        |     |

**Table 32. Serial FLASH Interface Signals**

| Signal               | Pin | Signal  | Pin | Signal   | Pin |
|----------------------|-----|---------|-----|----------|-----|
| FLSH_SCK             | N9  | FLSH_SI | M11 | FLSH_CE# | M9  |
| FLSH_SO/LAN_DISABLE# | P9  |         |     |          |     |

**Table 33. LED Signals**

| Signal    | Pin | Signal    | Pin |
|-----------|-----|-----------|-----|
| LINK_UP#  | A12 | LINK100#  | B11 |
| ACTIVITY# | C11 | LINK1000# | B12 |

**Table 34. Other Signals**

| Signal | Pin | Signal | Pin |
|--------|-----|--------|-----|
| SDP[0] | N14 | SDP[2] | N13 |
| SDP[1] | P13 | SDP[3] | M12 |

Table 35. IEEE Test Signals

| Signal     | Pin | Signal     | Pin |
|------------|-----|------------|-----|
| IEEE_TEST- | D14 | IEEE_TEST+ | B14 |

Table 36. PHY Signals

| Signal  | Pin | Signal  | Pin | Signal | Pin |
|---------|-----|---------|-----|--------|-----|
| MDI[0]- | C14 | MDI[2]- | F14 | XTAL1  | K14 |
| MDI[0]+ | C13 | MDI[2]+ | F13 | XTAL2  | J14 |
| MDI[1]- | E14 | MDI[3]- | H14 |        |     |
| MDI[1]+ | E13 | MDI[3]+ | H13 |        |     |

Table 37. Test Interface Signals

| Signal   | Pin | Signal   | Pin | Signal     | Pin |
|----------|-----|----------|-----|------------|-----|
| JTAG_TCK | L14 | JTAG_TDO | M14 | JTAG_TRST# | L13 |
| JTAG_TDI | M13 | JTAG_TMS | L12 | TEST       | A13 |

Table 38. Digital Power Signals

| Signal | Pin | Signal | Pin | Signal | Pin |
|--------|-----|--------|-----|--------|-----|
| 3.3V   | A3  | 1.2V   | G5  | 1.2V   | J9  |
| 3.3V   | A7  | 1.2V   | G6  | 1.2V   | K10 |
| 3.3V   | A11 | 1.2V   | H5  | 1.2V   | K11 |
| 3.3V   | E1  | 1.2V   | H6  | 1.2V   | K5  |
| 3.3V   | K3  | 1.2V   | H7  | 1.2V   | K6  |
| 3.3V   | K4  | 1.2V   | H8  | 1.2V   | K7  |
| 3.3V   | K13 | 1.2V   | J10 | 1.2V   | K8  |
| 3.3V   | N6  | 1.2V   | J11 | 1.2V   | K9  |
| 3.3V   | N8  | 1.2V   | J5  | 1.2V   | L10 |
| 3.3V   | P2  | 1.2V   | J6  | 1.2V   | L4  |
| 3.3V   | P12 | 1.2V   | J7  | 1.2V   | L5  |
|        |     | 1.2V   | J8  | 1.2V   | L9  |



**Table 39. Analog Power Signals**

| Signal      | Pin | Signal      | Pin | Signal    | Pin |
|-------------|-----|-------------|-----|-----------|-----|
| ANALOG_1.2V | E11 | ANALOG_1.8V | D11 | CLKR_1.8V | D12 |
| ANALOG_1.2V | E12 | ANALOG_1.8V | G12 | XTAL_1.8V | J13 |
| ANALOG_1.2V | G13 | PLL_1.2V    | G4  |           |     |
| ANALOG_1.2V | H11 | PLL_1.2V    | H4  |           |     |

**Table 40. Grounds and No Connect Signals**

| Signal | Pin | Signal | Pin | Signal | Pin | Signal                      | Pin |
|--------|-----|--------|-----|--------|-----|-----------------------------|-----|
| VSS    | B3  | VSS    | F5  | VSS    | M6  | NC                          | L8  |
| VSS    | B7  | VSS    | F6  | VSS    | N1  | NC                          | P1  |
| VSS    | C10 | VSS    | F7  | VSS    | N12 | NC                          | P14 |
| VSS    | D5  | VSS    | F8  | VSS    | P8  | Pull up to VCC <sup>a</sup> | A10 |
| VSS    | D6  | VSS    | F9  | AVSS   | C12 | Pull up to VCC <sup>a</sup> | B10 |
| VSS    | D7  | VSS    | F10 | AVSS   | D13 | Pull up to VCC <sup>a</sup> | C9  |
| VSS    | D8  | VSS    | G7  | AVSS   | F11 | VSS                         | D4  |
| VSS    | E10 | VSS    | G8  | AVSS   | G11 | VSS                         | E4  |
| VSS    | E2  | VSS    | G9  | AVSS   | G14 | NC                          | A6  |
| VSS    | E5  | VSS    | G10 | AVSS   | K12 | NC                          | C5  |
| VSS    | E6  | VSS    | H9  | NC     | A1  | NC                          | F12 |
| VSS    | E7  | VSS    | H10 | NC     | A14 | NC                          | L7  |
| VSS    | E8  | VSS    | K2  | NC     | D9  | NC                          | M8  |
| VSS    | E9  | VSS    | L6  | NC     | D10 | NC                          | N11 |
| VSS    | F4  | VSS    | L11 | NC     | H12 | NC                          | C8  |

a. Use a 1 K  $\Omega$  resistor.

**Table 41. Voltage Regulation Control Signals**

| Signal | Pin | Signal | Pin |
|--------|-----|--------|-----|
| CTRL18 | B13 | CTRL12 | P11 |

Table 42. Signal Names in Pin Order (Sheet 1 of 6)

| Signal Name                 | Pin |
|-----------------------------|-----|
| NC                          | A1  |
| SERR#                       | A2  |
| 3.3V                        | A3  |
| IDSEL                       | A4  |
| AD[25]                      | A5  |
| NC                          | A6  |
| 3.3V                        | A7  |
| AD[30]                      | A8  |
| LAN_PWR_GOOD                | A9  |
| Pull up to VCC <sup>a</sup> | A10 |
| 3.3V                        | A11 |
| LINK_LED#                   | A12 |
| TEST                        | A13 |
| NC                          | A14 |
| AD[22]                      | B1  |
| AD[23]                      | B2  |
| VSS                         | B3  |
| AD[24]                      | B4  |
| AD[26]                      | B5  |
| AD[27]                      | B6  |
| VSS                         | B7  |
| AD[31]                      | B8  |
| RST#                        | B9  |
| Pull up to VCC <sup>a</sup> | B10 |
| LINK100#                    | B11 |
| LINK1000#                   | B12 |
| CTRL18                      | B13 |
| IEEE_TEST+                  | B14 |
| AD[21]                      | C1  |
| M66EN                       | C2  |
| REQ#                        | C3  |
| C/BE#[3]                    | C4  |
| NC                          | C5  |

**Table 42. Signal Names in Pin Order (Sheet 2 of 6) (Continued)**

|                             |     |
|-----------------------------|-----|
| AD[28]                      | C6  |
| AD[29]                      | C7  |
| NC                          | C8  |
| Pull up to VCC <sup>a</sup> | C9  |
| VSS                         | C10 |
| ACTIVITY#                   | C11 |
| AVSS                        | C12 |
| MDI[0]+                     | C13 |
| MDI[0]-                     | C14 |
| AD[18]                      | D1  |
| AD[19]                      | D2  |
| AD[20]                      | D3  |
| VSS                         | D4  |
| VSS                         | D5  |
| VSS                         | D6  |
| VSS                         | D7  |
| VSS                         | D8  |
| NC                          | D9  |
| NC                          | D10 |
| ANALOG_1.8V                 | D11 |
| CLKR_1.8V                   | D12 |
| AVSS                        | D13 |
| IEEE_TEST-                  | D14 |
| 3.3V                        | E1  |
| VSS                         | E2  |
| AD[17]                      | E3  |
| VSS                         | E4  |
| VSS                         | E5  |
| VSS                         | E6  |
| VSS                         | E7  |
| VSS                         | E8  |
| VSS                         | E9  |
| VSS                         | E10 |
| ANALOG_1.2V                 | E11 |
| ANALOG_1.2V                 | E12 |
| MDI[1]+                     | E13 |

Table 42. Signal Names in Pin Order (Sheet 3 of 6) (Continued)

|             |     |
|-------------|-----|
| MDI[1]-     | E14 |
| IRDY#       | F1  |
| FRAME#      | F2  |
| C/BE#[2]    | F3  |
| VSS         | F4  |
| VSS         | F5  |
| VSS         | F6  |
| VSS         | F7  |
| VSS         | F8  |
| VSS         | F9  |
| VSS         | F10 |
| AVSS        | F11 |
| NC          | F12 |
| MDI[2]+     | F13 |
| MDI[2]-     | F14 |
| CLK         | G1  |
| VIO         | G2  |
| TRDY#       | G3  |
| PLL_1.2V    | G4  |
| 1.2V        | G5  |
| 1.2V        | G6  |
| VSS         | G7  |
| VSS         | G8  |
| VSS         | G9  |
| VSS         | G10 |
| AVSS        | G11 |
| ANALOG_1.8V | G12 |
| ANALOG_1.2V | G13 |
| AVSS        | G14 |
| STOP#       | H1  |
| INTA#       | H2  |
| DEVSEL#     | H3  |
| PLL_1.2V    | H4  |
| 1.2V        | H5  |
| 1.2V        | H6  |
| 1.2V        | H7  |

**Table 42. Signal Names in Pin Order (Sheet 4 of 6) (Continued)**

|             |     |
|-------------|-----|
| 1.2V        | H8  |
| VSS         | H9  |
| VSS         | H10 |
| ANALOG_1.2V | H11 |
| NC          | H12 |
| MDI[3]+     | H13 |
| MDI[3]-     | H14 |
| PAR         | J1  |
| PERR#       | J2  |
| GNT#        | J3  |
| EEMODE      | J4  |
| 1.2V        | J5  |
| 1.2V        | J6  |
| 1.2V        | J7  |
| 1.2V        | J8  |
| 1.2V        | J9  |
| 1.2V        | J10 |
| 1.2V        | J11 |
| AUX_PWR     | J12 |
| XTAL_1.8V   | J13 |
| XTAL2       | J14 |
| AD[16]      | K1  |
| VSS         | K2  |
| 3.3V        | K3  |
| 3.3V        | K4  |
| 1.2V        | K5  |
| 1.2V        | K6  |
| 1.2V        | K7  |
| 1.2V        | K8  |
| 1.2V        | K9  |
| 1.2V        | K10 |
| 1.2V        | K11 |
| AVSS        | K12 |
| 3.3V        | K13 |
| XTAL1       | K14 |
| AD[14]      | L1  |

Table 42. Signal Names in Pin Order (Sheet 5 of 6) (Continued)

|            |     |
|------------|-----|
| AD[15]     | L2  |
| C/BE#[1]   | L3  |
| 1.2V       | L4  |
| 1.2V       | L5  |
| VSS        | L6  |
| NC         | L7  |
| NC         | L8  |
| 1.2V       | L9  |
| 1.2V       | L10 |
| VSS        | L11 |
| JTAG_TMS   | L12 |
| JTAG_TRST# | L13 |
| JTAG_TCK   | L14 |
| AD[11]     | M1  |
| AD[12]     | M2  |
| AD[13]     | M3  |
| C/BE#[0]#  | M4  |
| AD[5]      | M5  |
| VSS        | M6  |
| AD[1]      | M7  |
| NC         | M8  |
| FLSH_CE#   | M9  |
| EESK       | M10 |
| FLSH_SI    | M11 |
| SDP[3]     | M12 |
| JTAG_TDI   | M13 |
| JTAG_TDO   | M14 |
| VSS        | N1  |
| AD[10]     | N2  |
| AD[9]      | N3  |
| AD[7]      | N4  |
| AD[4]      | N5  |
| 3.3V       | N6  |
| AD[0]      | N7  |
| 3.3V       | N8  |
| FLSH_SCK   | N9  |

**Table 42. Signal Names in Pin Order (Sheet 6 of 6) (Continued)**

|         |     |
|---------|-----|
| EEDO    | N10 |
| NC      | N11 |
| VSS     | N12 |
| SDP[2]  | N13 |
| SDP[0]  | N14 |
| NC      | P1  |
| 3.3V    | P2  |
| AD[8]   | P3  |
| AD[6]   | P4  |
| AD[3]   | P5  |
| AD[2]   | P6  |
| EECS    | P7  |
| VSS     | P8  |
| FLSH_SO | P9  |
| EEDI    | P10 |
| CTRL12  | P11 |
| 3.3V    | P12 |
| SDP[1]  | P13 |
| NC      | P14 |

a. Use a 1 K  $\Omega$  resistor.

## 5.4 Visual Pin Assignments

|    | A              | B              | C              | D           | E           | F        | G           | H           | J         | K      | L          | M        | N        | P       |
|----|----------------|----------------|----------------|-------------|-------------|----------|-------------|-------------|-----------|--------|------------|----------|----------|---------|
| 1  | NC             | AD[22]         | AD[21]         | AD[18]      | 3.3V        | IRDY#    | CLK         | STOP#       | PAR       | AD[16] | AD[14]     | AD[11]   | VSS      | NC      |
| 2  | SERR#          | AD[23]         | M66EN          | AD[19]      | VSS         | FRAME#   | VIO         | INTA#       | PERR#     | VSS    | AD[15]     | AD[12]   | AD[10]   | 3.3V    |
| 3  | 3.3V           | VSS            | REQ#           | AD[20]      | AD[17]      | C/BE#[2] | TRDY#       | DVSEL#      | GNT#      | 3.3V   | C/B3#[1]   | AD[13]   | AD[9]    | AD[8]   |
| 4  | IDSEL          | AD[24]         | C/BE#[3]       | VSS         | VSS         | VSS      | PLL_1.2V    | PLL_1.2V    | EEMODE    | 3.3V   | 1.2V       | C/BE#[0] | AD[7]    | AD[6]   |
| 5  | AD[25]         | AD[26]         | NC             | VSS         | VSS         | VSS      | 1.2V        | 1.2V        | 1.2V      | 1.2V   | 1.2V       | AD[5]    | AD[4]    | AD[3]   |
| 6  | NC             | AD[27]         | AD[28]         | VSS         | VSS         | VSS      | 1.2V        | 1.2V        | 1.2V      | 1.2V   | VSS        | VSS      | 3.3V     | AD[2]   |
| 7  | 3.3V           | VSS            | AD[29]         | VSS         | VSS         | VSS      | VSS         | 1.2V        | 1.2V      | 1.2V   | NC         | AD[1]    | AD[0]    | EECS    |
| 8  | AD[30]         | AD[31]         | NC             | VSS         | VSS         | VSS      | VSS         | 1.2V        | 1.2V      | 1.2V   | NC         | NC       | 3.3V     | VSS     |
| 9  | LAN_PWR_GOOD   | RST#           | Pull Up To VCC | NC          | VSS         | VSS      | VSS         | VSS         | 1.2V      | 1.2V   | 1.2V       | FLSH_CE# | FLSH_SCK | FLSH_SO |
| 10 | Pull Up To VCC | Pull Up To VCC | VSS            | NC          | VSS         | VSS      | VSS         | VSS         | 1.2V      | 1.2V   | 1.2V       | EESK     | EEDO     | EEDI    |
| 11 | 3.3V           | LINK100#       | ACTIVITY#      | ANALOG_1.8V | ANALOG_1.2V | AVSS     | AVSS        | ANALOG_1.2V | 1.2V      | 1.2V   | VSS        | FLSH_SI  | NC       | CTRL12  |
| 12 | LINK_LED#      | LINK1000#      | AVSS           | CLKR_1.8V   | ANALOG_1.2V | NC       | ANALOG_1.8V | NC          | AUX_PWR   | AVSS   | JTAG_TMS   | SDP[3]   | VSS      | 3.3V    |
| 13 | TEST           | CTRL18         | MDI[0]+        | AVSS        | MDI[1]+     | MDI[2]+  | ANALOG_1.2V | MDI[3]+     | XTAL_1.8V | 3.3V   | JTAG_TRST# | JTAG_TDI | SDP[2]   | SDP[1]  |
| 14 | NC             | IEEE_TEST+     | MDI[0]-        | IEEE_TEST-  | MDI[1]-     | MDI[2]-  | AVSS        | MDI[3]-     | XTAL2     | XTAL1  | JTAG_TCK   | JTAG_TDO | SDP[0]   | NC      |

**Pins A10, B-10, and C9 - Use 1K ohm resistors.**

**Figure 13. Visual Pin Assignments**